

Fast CMOS Multilevel Pipeline Registers

Product Features:

- PI29FCT520T and PI29FCT521T are pinout and function compatible with IDT29FCT520/521, QS29FCT520/521 and AMD's Am29520/521
- Four 8-bit high-speed registers
- Hold, Transfer, and load instructions
- Dual two-level or single four-level pipeline operation
- TTL input and output levels, reducing problematic "ground bounce"
- High output drive
I_{OL} = 48 mA
- Extremely low static power (1 mW, typ.)
- Industrial operating temperature range: -40°C to +85°C
- FCT (2xxxT) has a 25Ω series resistor.
- Packages available:
 - 24-pin 300 mil wide plastic DIP (P24)
 - 24-pin 150 mil wide plastic QSOP (Q24)
 - 24-pin 150 mil wide plastic TQSOP (R24)
 - 24-pin 300 mil wide plastic SOIC (S24)

Product Description:

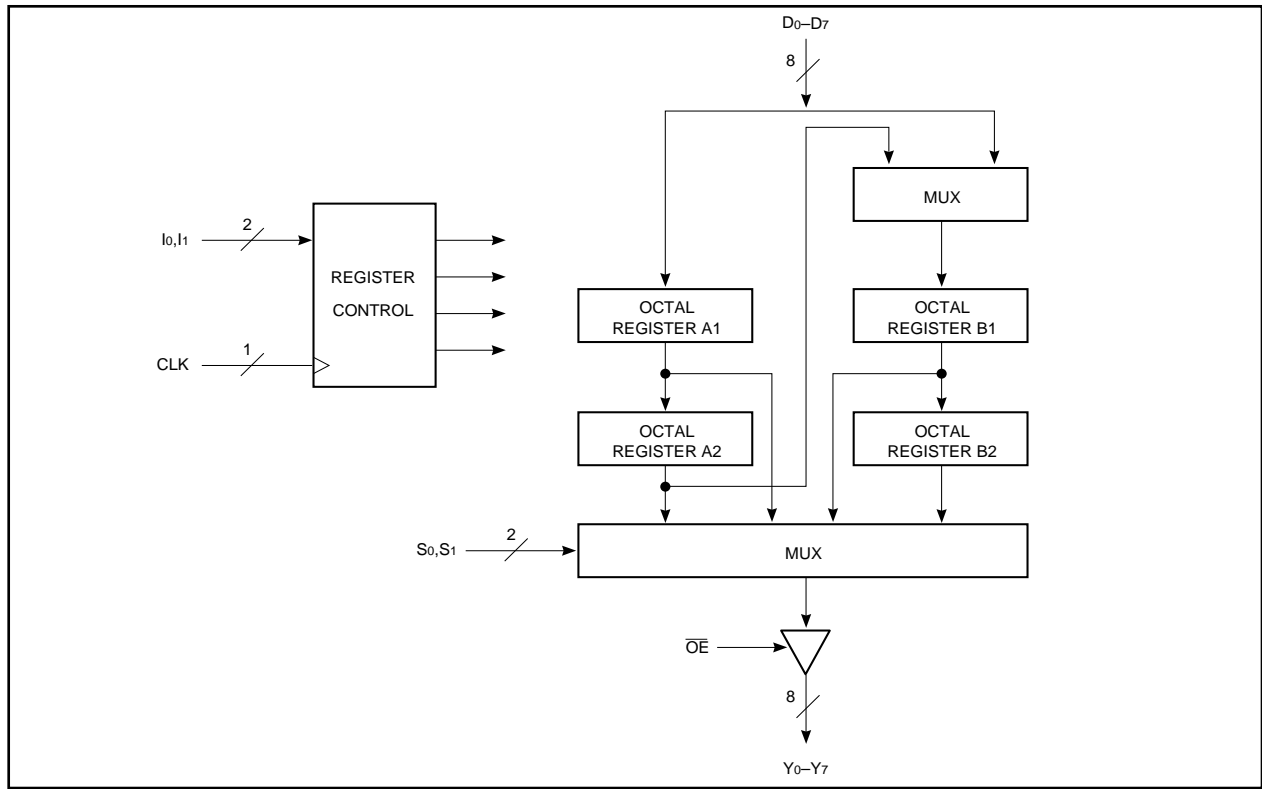
Pericom Semiconductor's PI29FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI29FCT520T/2520T and PI29FCT521T are multilevel pipeline registers containing four 8-bit positive triggered registers which can be configured as a dual 2-level or a single 4-level pipeline. These products are designed for use as temporary storage or for storage delays in pipelined systems.

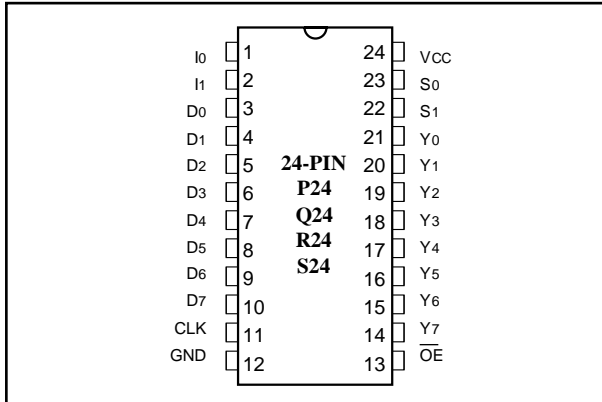
The PI29FCT521T differs from the PI29FCT520T/2520T only in the way data is loaded into and between registers in the dual 2-level operation. When data is entered into the first level (I = 2 or I = 1) of the PI29FCT520T/2520T, the existing data in the first level is moved to the second level. In the PI29FCT521T, these instructions simply overwrite the data in the first level. Transfer of data to the second level is achieved using the 4-level shift instruction (I = 0) causing the first level to change. In either part, I = 3 shift instruction puts the registers on hold.

Device models available upon request.

Logic Block Diagram



Product Pin Configuration



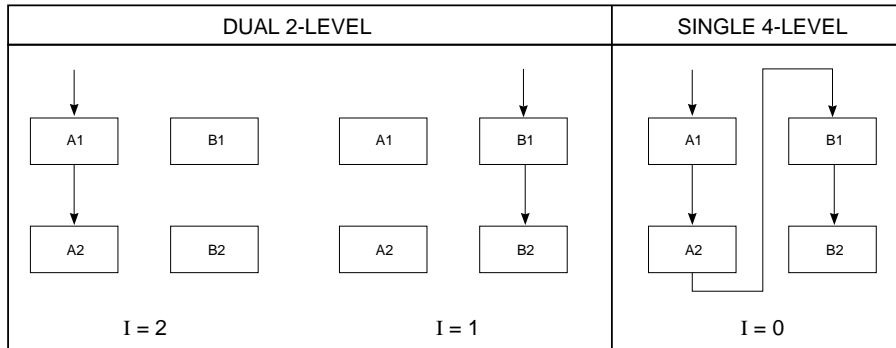
Product Pin Description

Pin Name	Description
\overline{OE}	Output Enable Input (Active LOW) for 3-State Output Port
CLK	Clock Input. Enter data into registers on LOW-to-HIGH transistions
I0,I1	Instruction Inputs
S0,S1	Multiplexer Select. Inputs either register A1, A2, B1, or B2 data to be avaiable at the output ports
Dx	Register Inputs
Yx	Register Outputs
GND	Ground
Vcc	Power

Register Selection

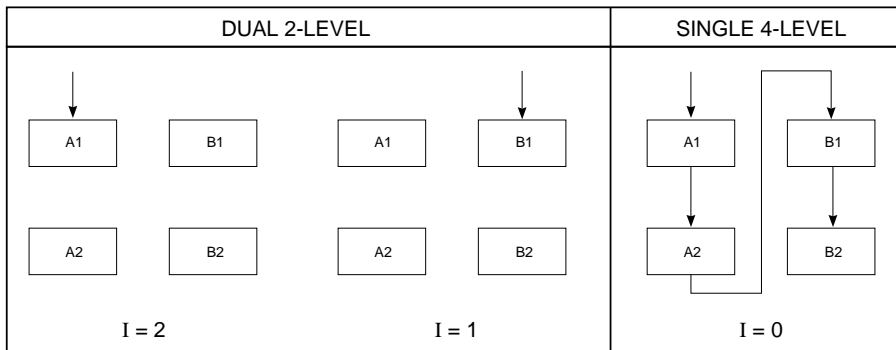
S1	S0	Register
0	0	B2
0	1	B1
1	0	A2
1	1	A1

PI29FCT520/T2520T Data Loading



NOTE: I = 3 FOR HOLD

PI29FCT521T Data Loading



NOTE: I = 3 FOR HOLD

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = MIN., V _{IN} = V _{IH} OR V _{IL} I _{OH} = -15.0 mA	2.4	3.0		V
V _{OL}	Output LOW Voltage	V _{CC} = MIN., V _{IN} = V _{IH} OR V _{IL} I _{OL} = 48 mA		0.3	0.50	V
			I _{OL} = 12 mA (25Ω series)		0.3	0.50
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I _{IH}	Input HIGH Current	V _{CC} = MAX., V _{IN} = V _{CC}			1	μA
I _{IL}	Input LOW Current	V _{CC} = MAX., V _{IN} = GND			-1	μA
I _{OZH}	High Impedance	V _{CC} = MAX., V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current	V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = MIN., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = MAX. ⁽³⁾ , V _{OUT} = GND	-60	-120		mA
I _{OFF}	Power Down Disable	V _{CC} = GND, V _{OUT} = 4.5V	—	—	100	μA
V _H	Input Hysteresis			200		mV

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.0	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open \overline{OE} = GND One Input Toggling 50% Duty Cycle	V _{IN} = GND V _{IN} = V _{CC}		0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁵⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle \overline{OE} = GND One Bit Toggling f _I = 5 MHz 50% Duty Cycle	V _{IN} = GND V _{IN} = V _{CC}		1.5	3.5 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.0	5.5 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle \overline{OE} = GND Eight Bits Toggling f _I = 5 MHz 50% Duty Cycle	V _{IN} = GND V _{IN} = V _{CC}		3.8	7.3 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		6.0	16.3 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V, control inputs only); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply characteristics.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_I = Input Frequency
 N_I = Number of Inputs at f_I
 All currents are in milliamperes and all frequencies are in megahertz.

PI29FCT520T/2520T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	FCT520AT/2520AT		FCT520BT/2520BT		Unit
			Com.		Com.		
			Min	Max	Min	Max	
tPLH tPHL	Propagation Delay CLK to Yx	CL = 50 pF RL = 500Ω	2.0	14.0	2.0	7.5	ns
tPLH tPHL	Propagation Delay S0 or S1 to Yx		2.0	13.0	2.0	7.5	ns
tsu	Setup Time HIGH or LOW Dx to CLK		5.0	—	2.5	—	ns
th	Hold Time HIGH or LOW Dx to CLK		2.0	—	2.0	—	ns
tsu	Setup Time HIGH or LOW I0 or I1 to CLK		5.0	—	4.0	—	ns
th	Hold Time HIGH or LOW I0 or I1 to CLK		2.0	—	2.0	—	ns
tpZH tpZL	Output Enable Time OE to Yx		1.5	12.0	1.5	7.0	ns
tpHZ tpLZ	Output Disable Time ⁽³⁾ OE to Yx		1.5	15.0	1.5	7.5	ns
tw	Clock Pulse Width ⁽³⁾ HIGH or LOW		7.0	—	5.5	—	ns

PI29FCT521T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	FCT521AT		FCT521BT		Unit
			Com.		Com.		
			Min	Max	Min	Max	
tPLH tPHL	Propagation Delay CLK to Yx	CL = 50 pF RL = 500Ω	2.0	14.0	2.0	7.5	ns
tPLH tPHL	Propagation Delay S0 or S1 to Yx		2.0	13.0	2.0	7.5	ns
tsu	Setup Time HIGH or LOW Dx to CLK		5.0	—	2.5	—	ns
th	Hold Time HIGH or LOW Dx to CLK		2.0	—	2.0	—	ns
tsu	Setup Time HIGH or LOW I0 or I1 to CLK		5.0	—	4.0	—	ns
th	Hold Time HIGH or LOW I0 or I1 to CLK		2.0	—	2.0	—	ns
tpZH tpZL	Output Enable Time OE to Yx		1.5	12.0	1.5	7.0	ns
tpHZ tpLZ	Output Disable Time ⁽³⁾ OE to Yx		1.5	15.0	1.5	7.5	ns
tw	Clock Pulse Width ⁽³⁾ HIGH or LOW		7.0	—	5.5	—	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

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