

1.8V, 25-bit (1:1) or 14-bit (1:2) JEDEC-Compliant Data Register

Features

- Operating frequency: DC to 500 MHz
- Supports DDRII SDRAM
- Two operations modes: 25 bit (1:1) and 14 bit (1:2)
- 1.8V operation
- Fully JEDEC-compliant
- 96-ball VFBGA

Functional Description

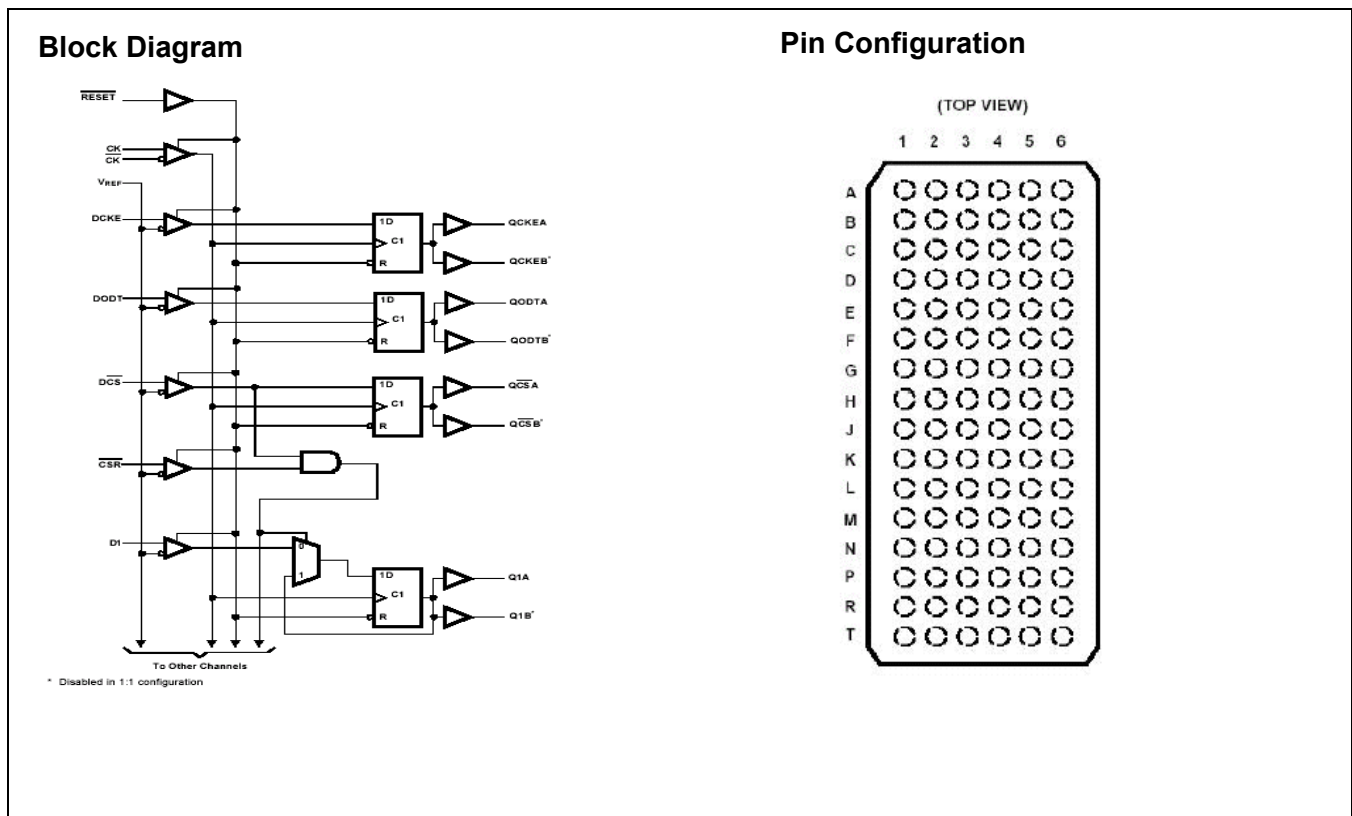
All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8-V CMOS drivers that have been optimized to drive the DDR-II DIMM load. The CY2SSTU32864 operates from a differential clock (CK and CK#). Data are registered at the crossing of CK going high, and CK# going low.

The C0 input controls the pinout configuration of the 1:2 pinout from A configuration (when low) to B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high). C0 = 1 and C1 = 0 is not allowed and either it does or it doesn't defaults to the C0 = C1 = 0 state.

The device monitors both DCS# and CSR# inputs and will gate the Qn outputs from changing states when both DCS# and CSR# inputs are high. If either DCS# or CSR# input is low, the Qn outputs will function normally. The RESET input has priority over the DCS# and CSR# control and will force the outputs low. If the DCS#-control functionality is not desired, the CSR# input can be hardwired to ground, in which case the set-up time requirement for DCS# would be the same as for the other D data inputs.

The device supports low-power standby operation. When the reset input (RESET#) is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (VREF) inputs are allowed. In addition, when RESET# is low, all registers are reset and all outputs are forced low. The LVCMOS RESET# and Cn inputs must always be held at a valid logic high or low level. To ensure defined outputs from the register before a stable clock has been supplied, RESET# must be held in the low state during power-up.

In the DDR-II RDIMM application, RESET# is specified to be completely asynchronous with respect to CK and CK#. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers.



Pin Definition

Pin Name	Pin Number (C0=0, C1=0)	Pin Number (C0=0, C1=1)	Pin Number (C0=1, C1=1)	Description
GND	B3, B4, D3, D4, F3, F4, H3, H4, K3, K4, M3, M4, P3, P4	B3, B4, D3, D4, F3, F4, H3, H4, K3, K4, M3, M4, P3, P4	B3, B4, D3, D4, F3, F4, H3, H4, K3, K4, M3, M4, P3, P4	Ground
VDD	A4, C3, C4, E3, E4, G3, G4, J3, J4, L3, L4, N3, N4, R3, R4, T4	A4, C3, C4, E3, E4, G3, G4, J3, J4, L3, L4, N3, N4, R3, R4, T4	A4, C3, C4, E3, E4, G3, G4, J3, J4, L3, L4, N3, N4, R3, R4, T4	Power Supply Voltage
VREF	A3, T3	A3, T3	A3, T3	Input Reference Voltage
ZOH	J5	J5	J5	Reserved
ZOL	J6	J6	J6	Reserved
CK	H1	H1	H1	Positive Master Clock
CK#	J1	J1	J1	Negative Master Clock
C0	G6	G6	G6	Configuration control input
C1	G5	G5	G5	Configuration control input
RESET#	G2	G2	G2	Asynchronous reset – resets registers and disables Vref data and clock differential input receivers
CSR#	J2	J2	J2	Chip Select – Disables D1-D24 when both CSR# and DCS# are High (VDD)
DCS#	H2	H2	H2	Chip Select – Disables D1-D24 when both CSR# and DCS# are High (VDD)
D1			A1	Data input – clocked in on the crossing points of CK and CK#
D2-3	B1, C1	B1, C1	B1, C1	Data input – clocked in on the crossing points of CK and CK#
D4			D1	Data input – clocked in on the crossing points of CK and CK#
D5, 6, 8, 9, 10	E1, F1, K1, L1, M1	E1, F1, K1, L1, M1	E1, F1, K1, L1, M1	Data input – clocked in on the crossing points of CK and CK#
D11	N1	N1		Data input – clocked in on the crossing points of CK and CK#
D12, 13	P1, R1	P1, R1	P1, R1	Data input – clocked in on the crossing points of CK and CK#
D14	T1	T1		Data input – clocked in on the crossing points of CK and CK#
D15-25	B2, C2, E2, F2, K2, L2, M2, N2, P2, R2, T2			Data input – clocked in on the crossing points of CK and CK#
DODT	D1	D1	N1	The outputs of this register bit will not be suspended by the DCS# and CSR# Control
DCKE	A1	A1	T1	The outputs of this register bit will not be suspended by the DCS# and CSR# Control
Q1A			A5	Data Outputs that are suspended by the DCS# and CSR# control
Q2A-3A	B5, C5	B5, C5	B5, C5	Data Outputs that are suspended by the DCS# and CSR# control
Q4A			D5	Data Outputs that are suspended by the DCS# and CSR# control
Q5A, 6A, 8A, 9A, 10A	E5, F5, K5, L5, M5	E5, F5, K5, L5, M5	E5, F5, K5, L5, M5	Data Outputs that are suspended by the DCS# and CSR# control
Q11A	N5	N5		

Pin Definition (Continued)

Q12A, Q13A	P5, R5	P5, R5	P5, R5	
Q14A	T5	T5		Data Outputs that are suspended by the DCS# and CSR# control
Q1B			A6	Data Outputs that are suspended by the DCS# and CSR# control
Q2B-3B		B6, C6	B6, C6	Data Outputs that are suspended by the DCS# and CSR# control
Q4B			D6	Data Outputs that are suspended by the DCS# and CSR# control
Q5B, 6B, 8B, 9B, 10B,		E6, F6, K6, L6, M6	E6, F6, K6, L6, M6	Data Outputs that are suspended by the DCS# and CSR# control
Q11B		N6		Data Outputs that are suspended by the DCS# and CSR# control
Q12B, 13B		P6, R6	P6, R6	Data Outputs that are suspended by the DCS# and CSR# control
Q14B		T6		Data Outputs that are suspended by the DCS# and CSR# control
Q15-25	B6, C6, E6, F6, K6, L6, M6, N6, P6, R6, T6			Data Outputs that are suspended by the DCS# and CSR# control
QCSA#	H5	H5	H5	Data outputs that will not be suspended by the DCS# and CSR# control
QCSB#		H6	H6	Data outputs that will not be suspended by the DCS# and CSR# control
QODTA	D5	D5	N5	Data outputs that will not be suspended by the DCS# and CSR# control
QODTB		D6	N6	Data outputs that will not be suspended by the DCS# and CSR# control
QCKEA	A5	A5	T5	Data outputs that will not be suspended by the DCS# and CSR# control
QCKEB		A6	T6	Data outputs that will not be suspended by the DCS# and CSR# control
NC	A2, A6, D2, D6, G1, H6	A2, B2, C2, D2, E2, F2, G1, K2, L2, M2, N2, P2, R2, T2	A2, B2, C2, D2, E2, F2, G1, K2, L2, M2, N2, P2, R2, T2	No Connect Pins

Table 1. Flip Flop Function Table

Inputs						Outputs		
RESET#	DCS#	CSR#	CK	CK#	Dn, DODT, DCKE	Qn	QCS#	QODT, QCKE
H	L	L			L	L	L	L
H	L	L			H	H	L	H
H	L	L	L or H	L or H	X	Q0	Q0	Q0
H	L	H			L	L	L	L
H	L	H			H	H	L	H
H	L	H	L or H	L or H	X	Q0	Q0	Q0
H	H	L			L	L	H	L
H	H	L			H	H	H	H
H	H	L	L or H	L or H	X	Q0	Q0	Q0
H	H	H			L	Q0	H	L
H	H	H			H	Q0	H	H
H	H	H	L or H	L or H	X	Q0	Q0	Q0
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	L	L	L

Recommended Operating Conditions

Parameter	Description	Condition	Min.	Max.	Unit
T _A (Ind.)	Ambient Operating Temp		-40	85	C
T _A (Com.)	Ambient Operating Temp		0	70	C
V _{DD}	Operating Voltage		1.7	1.9	V

Absolute Maximum Conditions ^[1]

Parameter	Description	Condition	Min.	Max.	Unit
V _{IN}	Input Voltage Range ^[2,3]		-0.5	V _{DD} + 0.5	V
V _{OUT}	Output Voltage Range ^[2,3]		-0.5	V _{DD} + 0.5	V
T _S	Storage Temperature		-65	150	C
V _{CC}	Supply Voltage Range		-0.5	2.5	V
I _{IK}	Input Clamp Current	V _O < 0 or V _O > V _{DD}	-50	50	mA
I _{OK}	Output Clamp Current	V _O < 0 or V _O > V _{DD}	-50	50	mA
I _O	Continuous Output Current	V _O = 0 to V _{DD}	-50	50	mA
	Continuous Current through V _{DD} /GND		-100	100	mA

DC Electrical Specifications

Parameter	Description	Conditions	Min.	Max.	Unit
V _{IX}	Input Differential Crossing Voltage CK, CK#		0.675	1.125	V
I _{DD}	Static Standby Power Supply Current	RESET# = G _{ND} , IO = 0, V _{DD} = 1.9V		100	μA
	Static Operating Power Supply Current	RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , IO = 0, V _{DD} = 1.9V		40	mA
I _{DD}	Power Supply Current Dynamic Operating Clock Only	RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , CK, CK# switching 50% duty cycle, V _{DD} = 1.8V	28 (typical)		μA/MHz
	Dynamic Operating per each Data Input	RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , CK, CK# switching 50% duty cycle, V _{DD} = 1.8V, 1 IO switching 1:1 configuration	18 (typical)		μA/MHz
		RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , CK, CK# switching 50% duty cycle, V _{DD} = 1.8V, 1 IO switching 1:2 configuration	36 (typical)		μA/MHz
	Low Power Active Mode, CLK only	RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , CK, CK# switching 50% duty cycle, V _{DD} = 1.8V, CS Enabled	27 (typical)		μA/MHz
	Low Power Active Mode per each Data Input	RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , CK, CK# switching 50% duty cycle, V _{DD} = 1.8V, 1 IO switching 1:1 configuration, CS Enabled	2 (typical)		μA/MHz
RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , CK, CK# switching 50% duty cycle, V _{DD} = 1.8V, 1 IO switching 1:2 configuration; CS Enabled		2 (typical)		μA/MHz	
V _{ID}	Input Differential Voltage	CK, CK#	600	-	mV
V _{REF}	Voltage Reference		0.49*V _{DD}	0.51*V _{DD}	V
V _{TT}	Terminating Voltage		V _{REF} -40mV	V _{REF} +40mV	V

Notes:

- Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stresses ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- This value is limited to 2.5V (max.)

DC Electrical Specifications (Continued)

Parameter	Description	Conditions	Min.	Max.	Unit
V_I	Input Voltage		0	V_{DD}	V
I_I	Input Current	$V_I = V_{DD}$ or GND	-5	5	μ A
V_{IL}	AC Input Low Voltage	Data Inputs	-	$V_{REF}-250$ mV	V
	DC Input Low Voltage	Data Inputs	-	$V_{REF}-125$ mV	V
V_{IH}	AC Input High Voltage	Data Inputs	$V_{REF}+250$ mV	-	V
	DC Input High Voltage	Data Inputs	$V_{REF}+125$ mV	-	V
V_{OL}	Output Low Voltage	$I_{OL} = 100\mu$ A, $V_{CC} = 1.7$ V to 1.9V	-	0.2	V
		$I_{OL} = 6$ mA, $V_{CC} = 1.7$ V	-	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = -100$ μ A, $V_{CC} = 1.7$ V to 1.9V	$V_{DD}-0.2$	-	V
		$I_{OH} = -6$ mA, $V_{CC} = 1.7$ V	1.2	-	V
I_{OH}	Output High Current		-	-8	mA
I_{OL}	Output Low Current		-	8	mA

AC Electrical Specifications

Parameter	Description	Conditions	Min.	Max.	Unit
S_{LR}	Slew Rate Rising	dv/dt_r (20 to 80%)	1	4	V/ns
	Slew Rate Falling	dv/dt_f (20 to 80%)	1	4	V/ns
$dv/dt \Delta$	Delta between Rising/Falling Rates		-	1	V/ns
C_{IN}	C_i (Data)	$V_I = V_{REF} \pm 250$ mV	2.5	3.5	pF
	C_i (CK and CK#)	$V_{IX} = 0.9$ V, $V_{ID} = 600$ mV	2	3	pF
	C_i (RESET#)	$V_I = V_{DD}$ or V_{DD}	2.5		pF

AC Timing Specifications

Parameter	Description	Conditions	Min.	Max.	Unit
F_{CLK}	Clock Frequency		-	500	MHz
T_W		CK,CK# H or L	1	-	ns
$T_{ACT}^{[4,5]}$	Differential Input Active time		-	10	ns
$T_{INACT}^{[4,5]}$	Differential Input Inactive time		-	15	ns
T_{SU}	Set up Time	DCS# before crossing CK,CK#, CSR = H, CK going high	0.7	-	ns
		DCS# before crossing CK,CK#, CSR = L, CK going high	0.5	-	ns
		CSR, ODT, CKE and data before crossing CK,CK#, CK going high	0.5	-	ns
T_H	Hold Time	DCS#, CSRT#, ODT, CKE and data after crossing CK,CK#, CK going high	0.5	-	ns
T_{PDM}	Propagation Delay without switching	From CK, CK# to Q	2.15 (typical)		ns
T_{PDMS}	Propagation Delay with switching	From CK, CK# to Q - simultaneous switching	2.35 (typical)		ns
T_{rPLH}	Propagation Delay from Low to High	RESET# to Q		3	ns
T_{rPHL}	Propagation Delay from High to Low	RESET# Start to Q Low		3	ns

Notes:

- Data and V_{REF} inputs must be low a minimum time of T_{ACT} max, after RESET# is taken high.
- Data, V_{REF} and clock inputs must be held at valid levels (not floating) a minimum time of T_{INACT} max after RESET# is taken low.

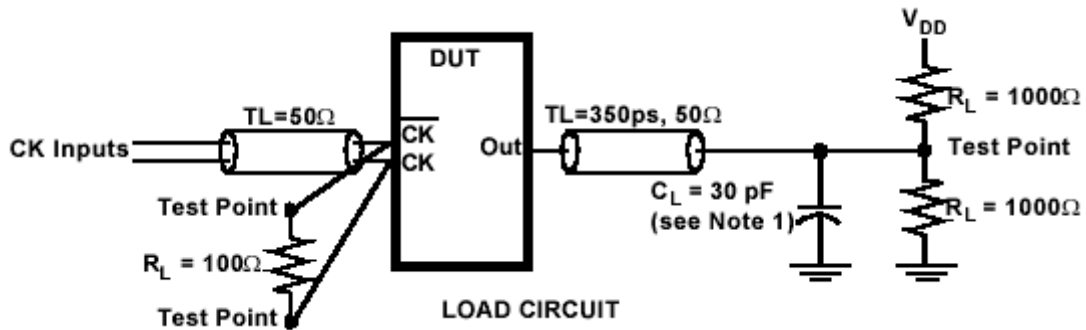


Figure 1. Test Load for Timing Measurements #1

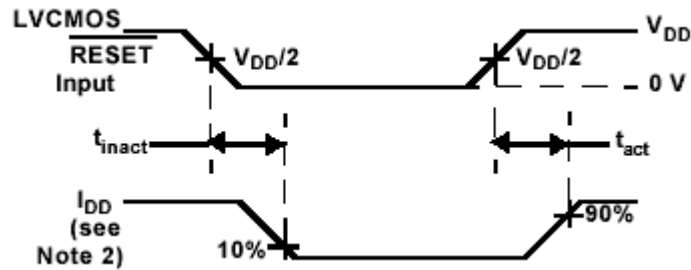


Figure 2. Voltage and Current Inputs Active and Inactive Times

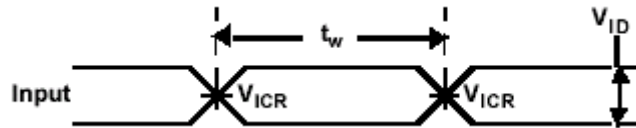


Figure 3. Pulse Duration

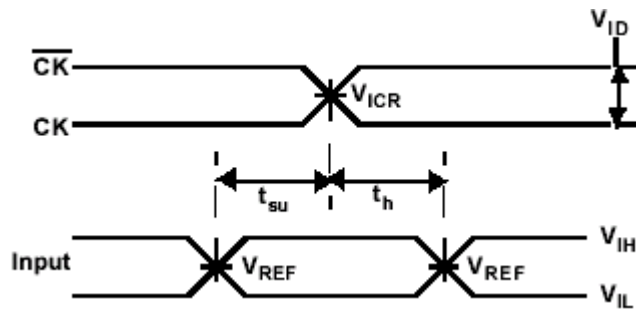


Figure 4. Set up and Hold Times

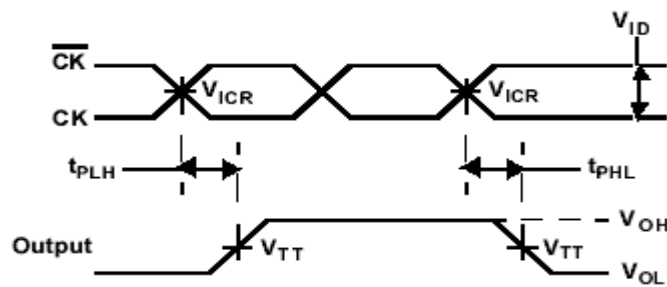


Figure 5. Propagation Delay

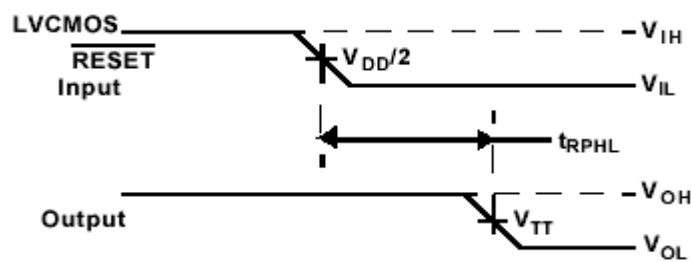
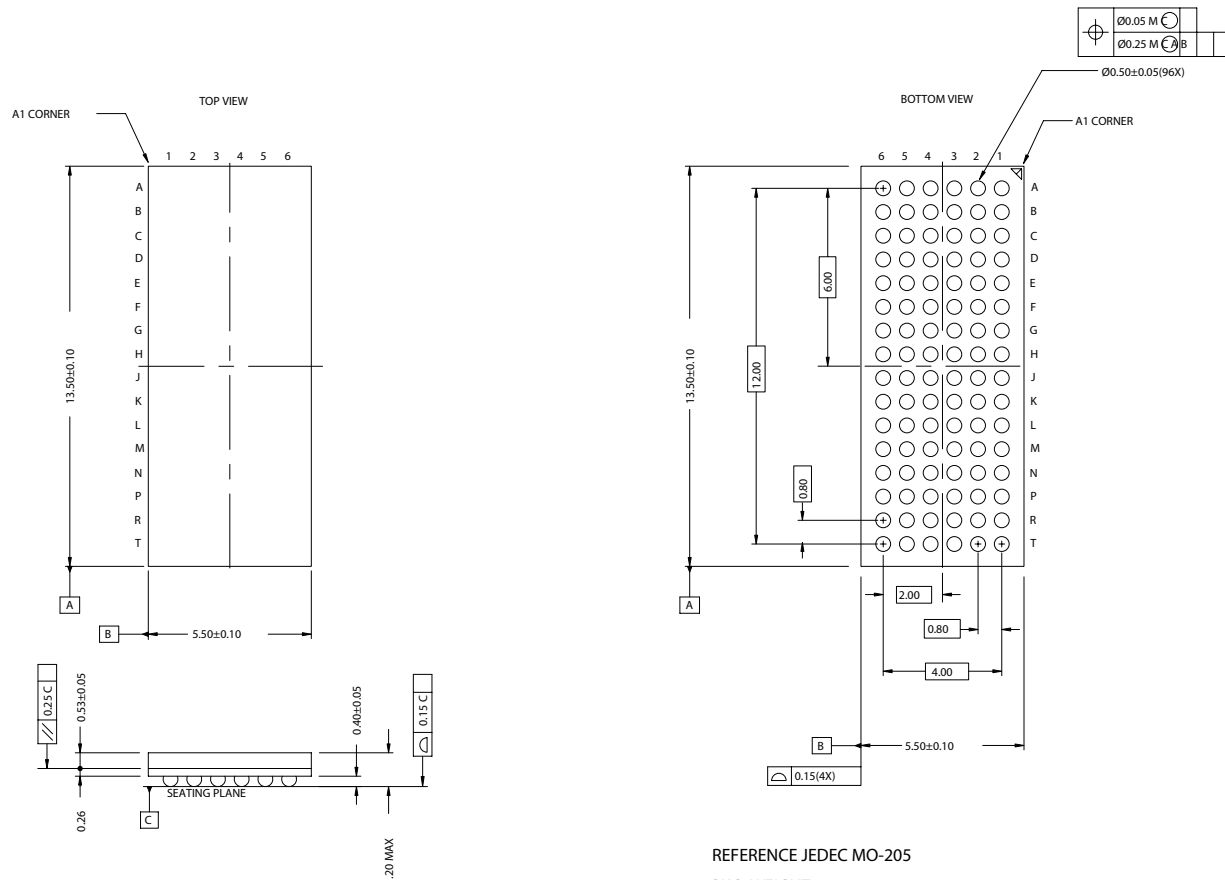


Figure 6. Propagation Delay after RESET#

Ordering Information

Part Number	Package Type	Product Flow
CY2SSTU32864BVXC	96-pin VFBGA	Commercial, 0° to 70°C
CY2SSTU32864BVXCT	96-pin VFBGA– Tape and Reel	Commercial, 0° to 70°C
CY2SSTU32864BVXI	96-pin VFBGA	Industrial, –40° to 85°C
CY2SSTU32864BVXIT	96-pin VFBGA– Tape and Reel	Industrial, –40° to 85°C

Package Drawing and Dimensions
96 FBGA (5.5 x 13.5 x 1.4 mm) BA96A


51-85202-*A

Document History Page

Document Title: CY2SSTU32864 1.8V, 25-bit (1:1) or 14-bit (1:2) JEDEC-Compliant Data Register Document #: 38-07576 Rev. *A				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	129199	09/09/03	RGL	New Data Sheet
*A	224102	See ECN	RGL	Added more information to complete the DS