



13-BIT TO 26-BIT REGISTERED BUFFER WITH SSTL I/O

IDT74SSTVN16859

FEATURES:

- 1:2 registered output buffer
- 2.3V to 2.7V operation for PC1600, PC2100, and PC2700
- 2.5V to 2.7V operation for PC3200
- Single bit propagation delay, TSSOP : 2.2ns, VFQFPN : 1.8ns
- SSTL_2 Class I style data inputs/outputs
- Differential CLK input
- $\overline{\text{RESET}}$ control compatible with LVCMOS levels
- Latch-up performance exceeds 100mA
- ESD >2000V per MIL-STD-883, Method 3015; >200V using machine model (C = 200pF, R = 0)
- Available in 56 pin VFQFPN and 64 pin TSSOP packages

APPLICATIONS:

- Ideally suited for stacked DIMM DDR registered applications
- Along with CSPT857C/D, Zero Delay PLL Clock buffer, provides complete solution for DDR1 DIMMs

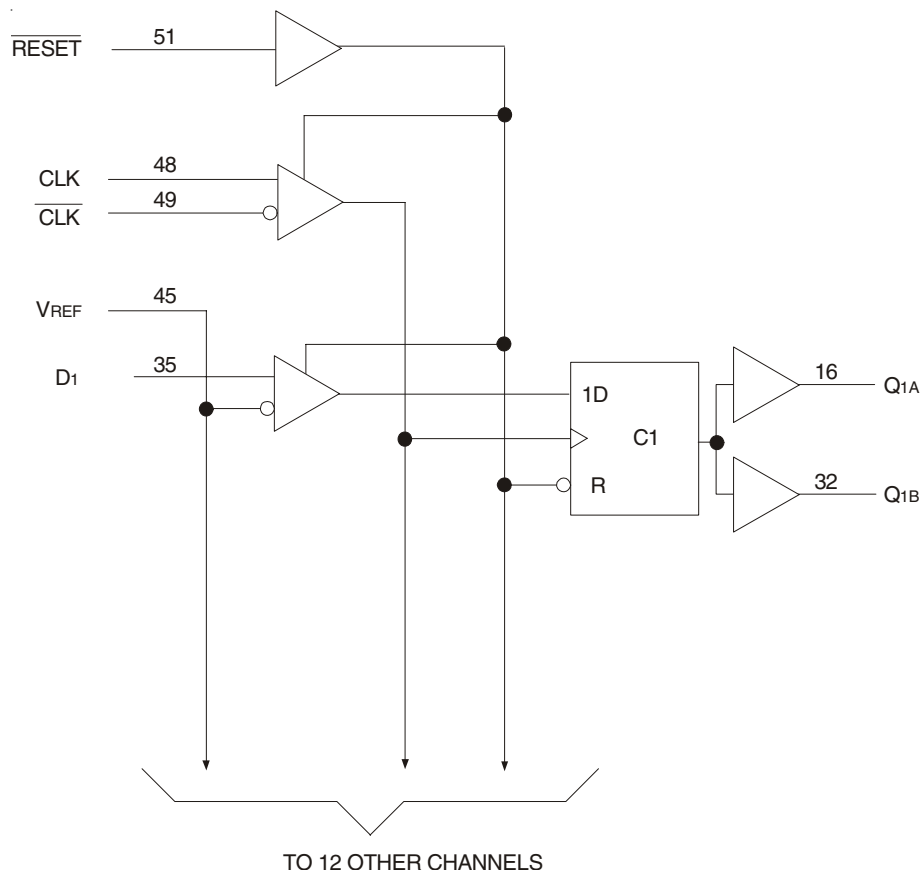
DESCRIPTION:

The SSTVN16859 is a 13-bit to 26-bit registered buffer designed for 2.3V-2.7V V_{DD} for PC1600 - PC2700 and 2.5V-2.7V V_{DD} for PC3200, and supports low standby operation. All data inputs and outputs are SSTL_2 level compatible with JEDEC standard for SSTL_2.

$\overline{\text{RESET}}$ is an LVCMOS input since it must operate predictably during the power-up phase. $\overline{\text{RESET}}$, which can be operated independent of CLK and $\overline{\text{CLK}}$, must be held in the low state during power-up in order to ensure predictable outputs (low state) before a stable clock has been applied.

$\overline{\text{RESET}}$, when in the low state, will disable all input receivers, reset all registers, and force all outputs to a low state, before a stable clock has been applied. With inputs held low and a stable clock applied, outputs will remain low during the Low-to-High transition of $\overline{\text{RESET}}$.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

| Pin Names | Description |
|---------------------------|---|
| Q1 - Q13 | Data Output |
| GND | Ground |
| V _{DDQ} | Output-stage drain power voltage |
| V _{DD} | Logic power voltage |
| $\overline{\text{RESET}}$ | Asynchronous reset input - resets registers and disables data and clock differential input receivers |
| V _{REF} | Input reference voltage |
| CLK | Positive master clock input |
| $\overline{\text{CLK}}$ | Negative master clock input |
| D1 - D13 | Data Input - clocked in on the crossing of the rising edge of CLK and the falling edge of $\overline{\text{CLK}}$ |
| Center PAD | Ground (MLF package only) |

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR PC1600 - PC2700

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: T_A = 0°C to +70°C, V_{DD} = 2.5V ±0.2V, V_{DDQ} = 2.5V ±0.2V

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|------------------|--|--|-----------------------|------|------|-------------------------|
| V _{IK} | Control Inputs | V _{DD} = 2.3V, I _I = -18mA | — | — | -1.2 | V |
| V _{OH} | | V _{DD} = 2.3V to 2.7V, I _{OH} = -100μA | V _{DD} - 0.2 | — | — | V |
| | | V _{DD} = 2.3V, I _{OH} = -8mA | 1.95 | — | — | |
| V _{OL} | | V _{DD} = 2.3V to 2.7V, I _{OL} = 100μA | — | — | 0.2 | V |
| | | V _{DD} = 2.3V, I _{OL} = 8mA | — | — | 0.35 | |
| I _I | All Inputs | V _{DD} = 2.7V, V _I = V _{DD} or GND | — | — | ±5 | μA |
| I _{DD} | Static Standby | I _O = 0, V _{DD} = 2.7V, $\overline{\text{RESET}}$ = GND | — | — | 0.01 | mA |
| | Static Operating | I _O = 0, V _{DD} = 2.7V, $\overline{\text{RESET}}$ = V _{DD} , V _I = V _{IH} (AC) or V _{IL} (AC) | — | — | 20 | |
| I _{DDQ} | Dynamic Operating (Clock Only) | I _O = 0, V _{DD} = 2.7V, $\overline{\text{RESET}}$ = V _{DD} , V _I = V _{IH} (AC) or V _{IL} (AC), CLK and $\overline{\text{CLK}}$ Switching 50% Duty Cycle. | — | 6 | — | μA/Clock MHz |
| | Dynamic Operating (Per Each Data Input) ⁽¹⁾ | I _O = 0, V _{DD} = 2.7V, $\overline{\text{RESET}}$ = V _{DD} , V _I = V _{IH} (AC) or V _{IL} (AC), CLK and $\overline{\text{CLK}}$ Switching 50% Duty Cycle. One Data Input Switching at Half Clock Frequency, 50% Duty Cycle. | — | 43 | — | μA/Clock MHz/Data Input |
| C _I | Data Inputs | V _{DD} = 2.5V, V _I = V _{REF} ± 310mV | 2 | — | 3 | pF |
| | CLK and $\overline{\text{CLK}}$ | V _{ICR} = 1.25V, V _I (PP) = 360mV | 2 | — | 3 | |
| | $\overline{\text{RESET}}$ | V _I = V _{DD} or GND | 2 | — | 3 | |

NOTE:

- Power dissipation levels will allow operation at DDR333 speeds without excessive die temperature.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR PC3200

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = 2.6\text{V} \pm 0.1\text{V}$, $V_{DDQ} = 2.6\text{V} \pm 0.1\text{V}$

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-----------|--|--|----------------|------|---------|--------------------------------|
| V_{IK} | Control Inputs | $V_{DD} = 2.5\text{V}$, $I_i = -18\text{mA}$ | — | — | -1.2 | V |
| V_{OH} | | $V_{DD} = 2.5\text{V}$ to 2.7V , $I_{OH} = -100\mu\text{A}$ | $V_{DD} - 0.2$ | — | — | V |
| | | $V_{DD} = 2.5\text{V}$, $I_{OH} = -8\text{mA}$ | 1.95 | — | — | |
| V_{OL} | | $V_{DD} = 2.5\text{V}$ to 2.7V , $I_{OL} = 100\mu\text{A}$ | — | — | 0.2 | V |
| | | $V_{DD} = 2.5\text{V}$, $I_{OL} = 8\text{mA}$ | — | — | 0.35 | |
| I_i | All Inputs | $V_{DD} = 2.7\text{V}$, $V_i = V_{DD}$ or GND | — | — | ± 5 | μA |
| I_{DD} | Static Standby | $I_o = 0$, $V_{DD} = 2.7\text{V}$, $\overline{\text{RESET}} = \text{GND}$ | — | — | 0.01 | mA |
| | Static Operating | $I_o = 0$, $V_{DD} = 2.7\text{V}$, $\overline{\text{RESET}} = V_{DD}$, $V_i = V_{IH}(\text{AC})$ or $V_{IL}(\text{AC})$ | — | — | 20 | |
| I_{DDQ} | Dynamic Operating (Clock Only) | $I_o = 0$, $V_{DD} = 2.7\text{V}$, $\overline{\text{RESET}} = V_{DD}$, $V_i = V_{IH}(\text{AC})$ or $V_{IL}(\text{AC})$, CLK and $\overline{\text{CLK}}$ Switching 50% Duty Cycle. | — | 6 | — | $\mu\text{A}/\text{Clock MHz}$ |
| | Dynamic Operating (Per Each Data Input) ⁽¹⁾ | $I_o = 0$, $V_{DD} = 2.7\text{V}$, $\overline{\text{RESET}} = V_{DD}$, $V_i = V_{IH}(\text{AC})$ or $V_{IL}(\text{AC})$, CLK and $\overline{\text{CLK}}$ Switching 50% Duty Cycle. One Data Input Switching at Half Clock Frequency, 50% Duty Cycle. | — | 43 | — | |
| C_i | Data Inputs | $V_{DD} = 2.6\text{V}$, $V_i = V_{REF} \pm 310\text{mV}$ | 2 | — | 3 | pF |
| | CLK and $\overline{\text{CLK}}$ | $V_{ICR} = 1.3\text{V}$, $V_i(\text{PP}) = 360\text{mV}$ | 2 | — | 3 | |
| | $\overline{\text{RESET}}$ | $V_i = V_{DD}$ or GND | 2 | — | 3 | |

NOTE:

- Power dissipation levels will allow operation at DDR400 speeds without excessive die temperature.

OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$ (1)

| Symbol | Parameter | | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|------------------|---|------------------------------|--------------------------|---------------------|--------------------------|------------------|
| V_{DD} | Supply Voltage | | V_{DDQ} | — | 2.7 | V |
| V_{DDQ} | Output Supply Voltage | PC1600 - PC12700 | 2.3 | 2.5 | 2.7 | V |
| | | PC3200 | 2.5 | 2.6 | 2.7 | |
| V_{REF} | Reference Voltage ($V_{REF} = V_{DDQ}/2$) | PC1600 - PC2700 | 1.15 | 1.25 | 1.35 | V |
| | | PC3200 | 1.25 | 1.3 | 1.35 | |
| V_{TT} | Termination Voltage | | $V_{REF} - 40\text{mV}$ | V_{REF} | $V_{REF} + 40\text{mV}$ | V |
| V_i | Input Voltage | | 0 | — | V_{DD} | V |
| V_{IH} | AC High-Level Input Voltage | Data Inputs | $V_{REF} + 310\text{mV}$ | — | — | V |
| V_{IL} | AC Low-Level Input Voltage | Data Inputs | — | — | $V_{REF} - 310\text{mV}$ | V |
| V_{IH} | DC High-Level Input Voltage | Data Inputs | $V_{REF} + 150\text{mV}$ | — | — | V |
| V_{IL} | DC Low-Level Input Voltage | Data Inputs | — | — | $V_{REF} - 150\text{mV}$ | V |
| V_{IH} | High-Level Input Voltage | $\overline{\text{RESET}}$ | 1.7 | — | — | V |
| V_{IL} | Low-Level Input Voltage | $\overline{\text{RESET}}$ | — | — | 0.7 | V |
| V_{ICR} | Common-Mode Input Range | CLK, $\overline{\text{CLK}}$ | 0.97 | — | 1.53 | V |
| $V_i(\text{PP})$ | Peak-to-Peak Input Voltage | CLK, $\overline{\text{CLK}}$ | 360 | — | — | mV |
| I_{OH} | High-Level Output Current | | — | — | -16 | mA |
| I_{OL} | Low-Level Output Current | | — | — | 16 | mA |
| T_A | Operating Free-Air Temperature | | 0 | — | +70 | $^\circ\text{C}$ |

NOTE:

- The $\overline{\text{RESET}}$ input of the device must be held at V_{DD} or GND to ensure proper device operation.

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

| Symbol | Parameter | PC1600-PC2700 | | PC3200 | | Unit |
|--------------------|--|---|------|--------|------|------|
| | | Min. | Max. | Min. | Max. | |
| CLOCK | Clock Frequency | — | 200 | — | 220 | MHz |
| t _w | Pulse Duration, CLK, $\overline{\text{CLK}}$ HIGH or LOW | 2.5 | — | 2.5 | — | ns |
| t _{ACT} | Differential Inputs Active Time ⁽¹⁾ | — | 22 | — | 22 | ns |
| t _{INACT} | Differential Inputs Inactive Time ⁽²⁾ | — | 22 | — | 22 | ns |
| t _{SU} | Setup Time, Fast Slew Rate ^(3,5) Data Before CLK \uparrow , CLK \downarrow | 0.65 | — | 0.65 | — | ns |
| | | Setup Time, Slow Slew Rate ^(4,5) | 0.75 | — | 0.75 | — |
| t _H | Hold Time, Fast Slew Rate ^(3,5) Data Before CLK \uparrow , CLK \downarrow | 0.75 | — | 0.65 | — | ns |
| | | Hold Time, Slow Slew Rate ^(2,5) | 0.9 | — | 0.8 | — |

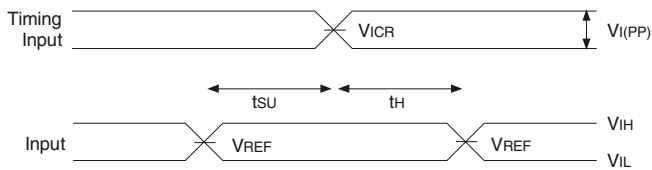
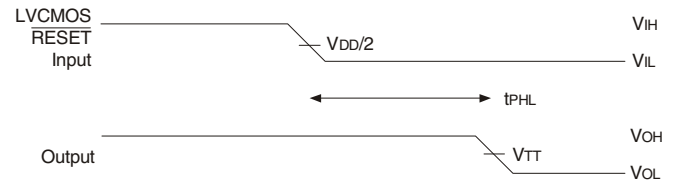
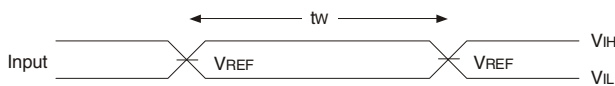
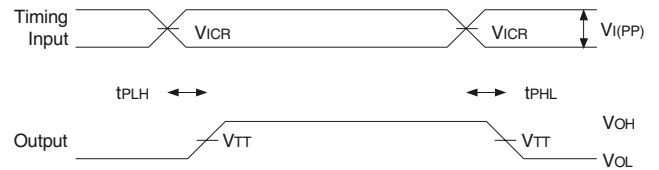
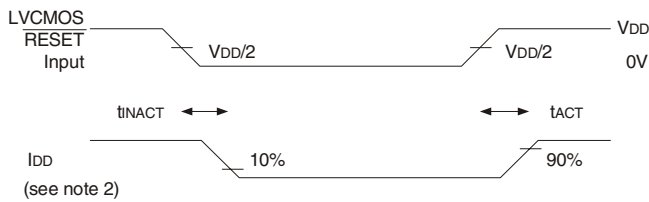
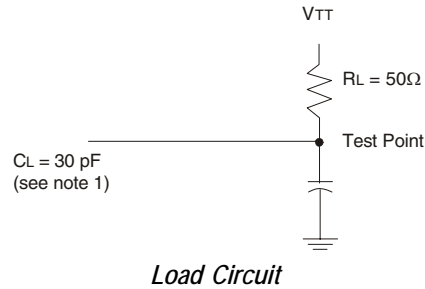
NOTES:

1. Data inputs must be low a minimum time of t_{ACT} max., after $\overline{\text{RESET}}$ is taken HIGH.
2. Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{INACT} max., after $\overline{\text{RESET}}$ is taken LOW.
3. For data signal input slew rate is $\geq 1\text{V/ns}$.
4. For data signal input slew rate is $\geq 0.5\text{V/ns}$ and $< 1\text{V/ns}$.
5. CLK, $\overline{\text{CLK}}$ signal input slew rates are $\geq 1\text{V/ns}$.

SWITCHING CHARACTERISTICS OVER RECOMMENDED FREE-AIR OPERATING RANGE (UNLESS OTHERWISE NOTED)

| Symbol | Parameter | Package | PC1600-PC2700 | | PC3200 | | Unit |
|--------------------|---|---------------|---------------|------|--------|---------|------|
| | | | Min. | Max. | Min. | Max. | |
| f _{MAX} | | TSSOP, VFQFPN | 200 | — | 220 | — | MHz |
| t _{PDM} | CLK and $\overline{\text{CLK}}$ to Q | TSSOP | 1.1 | 2.4 | 1.1 | 2.2 | ns |
| | | VFQFPN | 1.1 | 2.2 | 1.1 | 1.8 | |
| t _{PDMSS} | CLK and $\overline{\text{CLK}}$ to Q (simultaneous switching) | TSSOP | — | 2.7 | — | 2.5 | ns |
| | | VFQFPN | — | 2.5 | — | ((TBD)) | |
| t _{PHL} | $\overline{\text{RESET}}$ to Q | TSSOP, VFQFPN | — | 5 | — | 5 | ns |

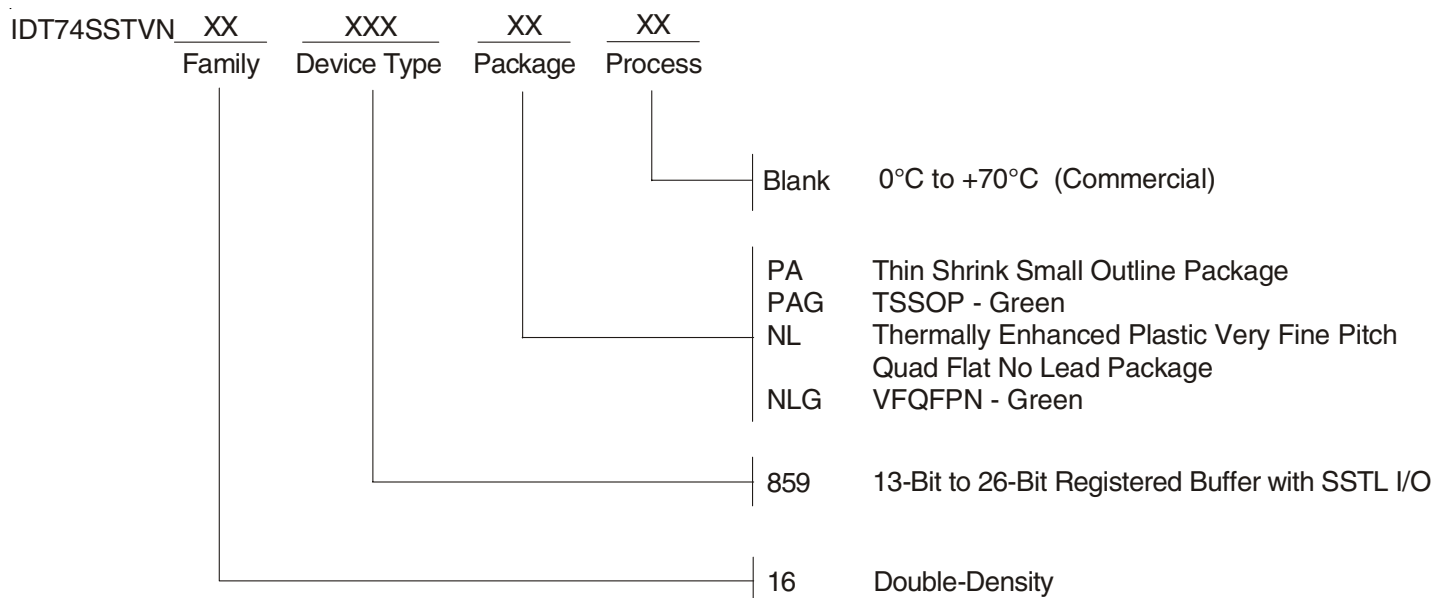
TEST CIRCUITS AND WAVEFORMS
FOR PC1600 - PC2700, $V_{DD} = 2.5V \pm 0.2V$
FOR PC3200, $V_{DD} = 2.6V \pm 0.1V$



NOTES:

1. C_L includes probe and jig capacitance.
2. I_{DD} tested with clock and data inputs held at V_{DD} or GND, and $I_o = 0mA$.
3. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10MHz$, $Z_o = 50\Omega$, input slew rate = $1 V/ns \pm 20\%$ (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5. $V_{TT} = V_{REF} = V_{DD}/2$
6. $V_{IH} = V_{REF} + 310mV$ (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVC MOS input.
7. $V_{IL} = V_{REF} - 310mV$ (AC voltage levels) for differential inputs. $V_{IL} = GND$ for LVC MOS input.
8. t_{PDM} is t_{PD} with one output switching. t_{PDMSS} is t_{PD} with all outputs switching.

ORDERING INFORMATION



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