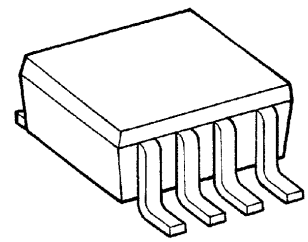
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7WH123FU, TC7WH123FK

MONOSTABLE MULTIVIBRATOR

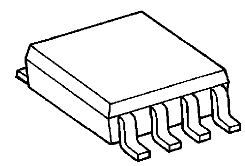
The TC74WH123 is high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C^2MOS technology.
There are two trigger inputs, $\overline{A}$ input (Negative edge), and B input (Positive edge). These inputs are valid for a slow rise/fall time signal (tr = tf = 1sec.) as they are schmitt trigger inputs. This device may also be triggered by using $\overline{CLR}$ input (Positive edge).
After triggering, the output stays in a MONOSTABLE state for a time period determined by the external resistor and capacitor (Rx, Cx). A low level at the $\overline{CLR}$ input breaks this state.
Limits for Cx and Rx are :
External capacitor, Cx ······· No limit
External resistor, Rx ··········· V_{CC} = 2.0V more than 5kΩ
V_{CC} ≧ 3.0V more than 1kΩ
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

TC7WH123FU



SSOP8-P-0.65

TC7WH123FK



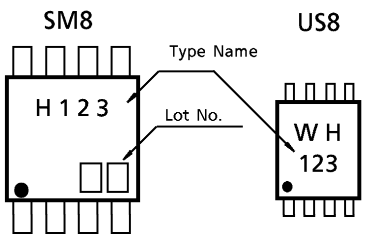
SSOP8-P-0.50A

Weight
SSOP8-P-0.65 : 0.02g (Typ.)
SSOP8-P-0.50A : 0.01g (Typ.)

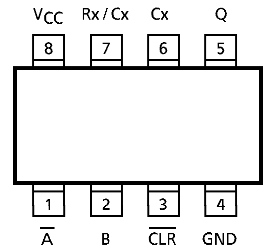
FEATURES

- High Speed ·························· t_{pd} = 8.1ns (Typ.) at V_{CC} = 5V
- Low Power Dissipation
  - Standby State ························ I_{CC} = 2μA (Max.) at Ta = 25°C
  - Active State ·························· I_{CC} = 600μA (Max.) at V_{CC} = 5V
- High Noise Immunity ··············· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays ······ $t_{pLH} \doteqdot t_{pHL}$
- Wide Operation Voltage Range ··· V_{CC} (opr) = 2~5.5V

MARKING



PIN ASSIGNMENT (TOP VIEW)

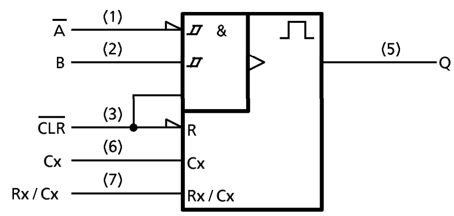


TRUTH TABLE

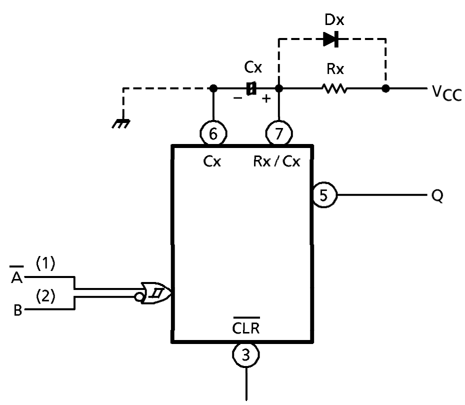
INPUTS			OUTPUTS	NOTE
$\overline{A}$	B	$\overline{CLR}$	Q	
↓	H	H	⎍	OUTPUT ENABLE
×	L	H	L	INHIBIT
H	×	H	L	INHIBIT
L	↑	H	⎍	OUTPUT ENABLE
L	H	↑	⎍	OUTPUT ENABLE
×	×	L	L	RESET

× : Don't Care

LOGIC DIAGRAM



BLOCK DIAGRAM



(Note 1) Cx, Rx, Dx are external

Capacitor, Resistor, and Diode, respectively.

(Note 2) External clamping diode, Dx ;

The external capacitor is charged to V_{CC} level in the wait state, i.e. when no trigger is applied.
If the supply voltage is turned off, Cx is discharges mainly through the internal (parasitic) diode. If Cx is sufficiently large and V_{CC} drops rapidly, there will be some possibility of damaging the IC through in rush current or latch-up. If the capacitance of the supply voltage filter is large enough and V_{CC} drops slowly, the in rush current is automatically limited and damage to the IC is avoided.
The maximum value of forward current through the parasitic diode is ±20mA.
In the case of a large Cx, the limit of fall time of the supply voltage is determined as follows:

$$t_r \geqq (V_{CC} - 0.7) \cdot Cx / 20mA$$

(t_r is the time between the supply voltage turn off and the supply voltage reaching 0.4 V_{CC}.)

In the even a system does not satisfy the above condition, an external clamping diode (Dx) is needed to protect the IC from rush current.

FUNCTIONAL DESCRIPTION

(1) Stand-by State

The external capacitor (Cx) is fully charged to V_{CC} in the stand-by state. That means, before triggering, the Q_P and Q_N transistors which are connected to the Rx / Cx node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies turn off. The total supply current is only leakage current.

(2) Trigger operation

Trigger operation is effective in any of the following three cases. First, the condition where the $\overline{A}$ input is low, and the B input has a rising signal ; second, where the B input is high, and the $\overline{A}$ input has a falling signal ; and third, where the $\overline{A}$ input is low and the B input is high, and the $\overline{CLR}$ input has a rising signal.
After a trigger becomes effective, comparators C1 and C2 start operating, and Q_N is turned on.
The external capacitor discharges through Q_N. The voltage level at the Rx / Cx node drops. If the Rx / Cx voltage level falls to the internal reference voltage Vref L, the output of C1 becomes low.
The flip-flop is then reset and Q_N turns off. At that moment C1 stops but C2 continues operating.
After Q_N turns off, the voltage at the Rx / Cx node starts rising at a rate determined by the time constant of external capacitor Cx and resistor Rx.
Upon triggering, output Q becomes high, following some delay time of the internal F / F and gates. It stays high even if the voltage of Rx / Cx changes from falling to rising. When Rx / C x reaches the internal reference voltage Vref H, the output of C2 becomes low, the output Q goes low and C2 stops its operation. That means, after triggering, when the voltage level of the Rx / Cx node reaches Vref H, the IC returns to its MONOSTABLE state.
With large values of Cx and Rx, and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse, tw (OUT), is as follows :

tw (OUT) = 1.0 Cx Rx

(3) Retrigger operation

When a new trigger is applied to either input $\overline{A}$ or B while in the MONOSTABLE state, it is effective only if the IC is charging Cx. The voltage level of the Rx / Cx node then falls to Vref L level again. Therefore the Q output stays high if the next trigger comes in before the time period set by Cx and Rx.
If the new trigger is very close to previous trigger, such as an occurrence during the discharge cycle, it will have no effect.
The minimum time for a trigger to be effective 2nd trigger, trr (Min.), depends on V_{CC} and Cx.

(4) Reset operation

In normal operation, the $\overline{CLR}$ input is held high. If $\overline{CLR}$ is low, a trigger has no effect because the Q output is held low and the trigger control F / F is reset. Also, Q_P turns on and Cx is charged rapidly to V_{CC}.
This means if $\overline{CLR}$ is set low, the IC goes into a wait state.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~7	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} / Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	300 (SM8)	mW
		200 (US8)	
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature (10 s)	T_L	260	°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~100 (V_{CC} = 3.3 ± 0.3V)	ns / V
		0~20 (V_{CC} = 5 ± 0.5V)	
External Capacitor	Cx	No Limitation*	F
External Resistor	Rx	≧5k (V_{CC} = 2.0V)* ≧1k (V_{CC} ≧ 3.0V)*	Ω

* The maximum allowable values of Cx and Rx are a function of leakage of capacitor Cx, the leakage of TC74VHC123A / 221A, and leakage due to board layout and surface resistance.
Susceptibility to externally induced noise signals may occur for Rx > 1MΩ.

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
Input Voltage	"H" Level	V_{IH}			2.0	1.5	—	—	1.5	—	V
					3.0~5.5	V_{CC} ×0.7	—	—	V_{CC} ×0.7	—	
	"L" Level	V_{IL}			2.0	—	—	0.5	—	0.5	
					3.0~5.5	—	—	V_{CC} ×0.3	—	V_{CC} ×0.3	
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	2.0	1.9	2.0	—	1.9	—	V
					3.0	2.9	3.0	—	2.9	—	
					4.5	4.4	4.5	—	4.4	—	
				I_{OH} = −4mA	3.0	2.58	—	—	2.48	—	
				I_{OH} = −8mA	4.5	3.94	—	—	3.80	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	2.0	—	0	0.1	—	0.1	
					3.0	—	0	0.1	—	0.1	
					4.5	—	0	0.1	—	0.1	
				I_{OL} = 4mA	3.0	—	—	0.36	—	0.44	
				I_{OL} = 8mA	4.5	—	—	0.36	—	0.44	
Control Input Current		I_{IN}	V_{IN} = 5.5V or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Rx / Cx Terminal Off-State Current		I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.25	—	±0.25	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	2.0	—	20.0	μA
		I_{CC}	V_{IN} = V_{CC} or GND, Rx / Cx = 0.5V_{CC}		3.0	—	160	250	—	280	
					4.5	—	380	500	—	650	
					5.5	—	560	750	—	975	

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C TYP.	Ta = 25°C LIMIT	Ta = −40~85°C LIMIT	UNIT
Minimum Pulse Width	t_W (L) t_W (H)		3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum Clear Width ($\overline{CLR}$)	t_W (L)		3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum Retrigger Time	t_{rr}	Rx = 1kΩ Cx = 100pF	3.3 ± 0.3	60	—	—	ns
			5.0 ± 0.5	39	—	—	
		Rx = 1kΩ Cx = 0.01μF	3.3 ± 0.3	1.5	—	—	
			5.0 ± 0.5	1.2	—	—	μs

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	CL (pF)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
Propagation Delay Time (A, B-Q)	t_{pLH} t_{pHL}		3.3 ± 0.3	15	—	13.4	20.6	1.0	24.0	ns
				50	—	15.9	24.1	1.0	27.5	
			5.0 ± 0.5	15	—	8.1	12.0	1.0	14.0	
				50	—	9.6	14.0	1.0	16.0	
Propagation Delay Time ($\overline{CLR}$ trigger-Q)	t_{pLH} t_{pHL}		3.3 ± 0.3	15	—	14.5	22.4	1.0	26.0	
				50	—	17.0	25.9	1.0	29.5	
			5.0 ± 0.5	15	—	8.7	12.9	1.0	15.0	
				50	—	10.2	14.9	1.0	17.0	
Propagation Delay Time ($\overline{CLR}$-Q)	t_{pLH} tpHL		3.3 ± 0.3	15	—	10.3	15.8	1.0	18.5	
				50	—	12.8	19.3	1.0	22.0	
			5.0 ± 0.5	15	—	6.3	9.4	1.0	11.0	
				50	—	7.8	11.4	1.0	13.0	
Output Pulse Width	t_{wOUT}	Cx = 28pF Rx = 2kΩ	3.3 ± 0.3	50	—	160	240	—	300	
			5.0 ± 0.5		—	133	200	—	240	
		Cx = 0.01μF Rx = 10kΩ	3.3 ± 0.3	50	90	100	110	90	110	μs
			5.0 ± 0.5		90	100	110	90	110	
		Cx = 0.1μF Rx = 10kΩ	3.3 ± 0.3	50	0.9	1.0	1.1	0.9	1.1	ms
			5.0 ± 0.5		0.9	1.0	1.1	0.9	1.1	
Input Capacitance	C_{IN}					4	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 1)			—	73	—	—	—	

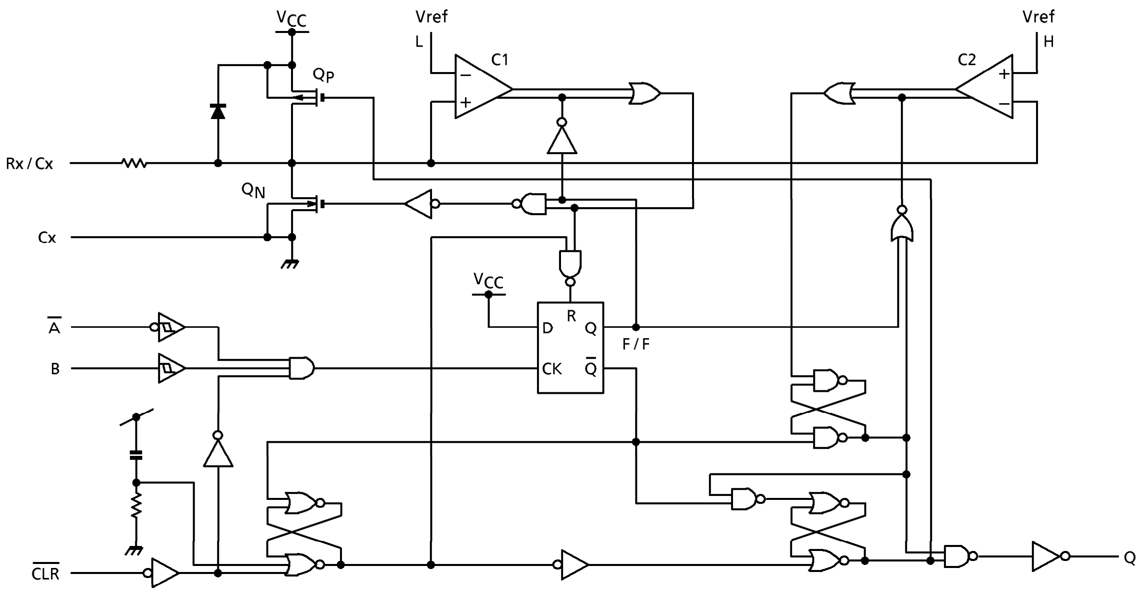
(Note 1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :

$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot Duty / 100 + I_{CC} / 2$ (per circuit)

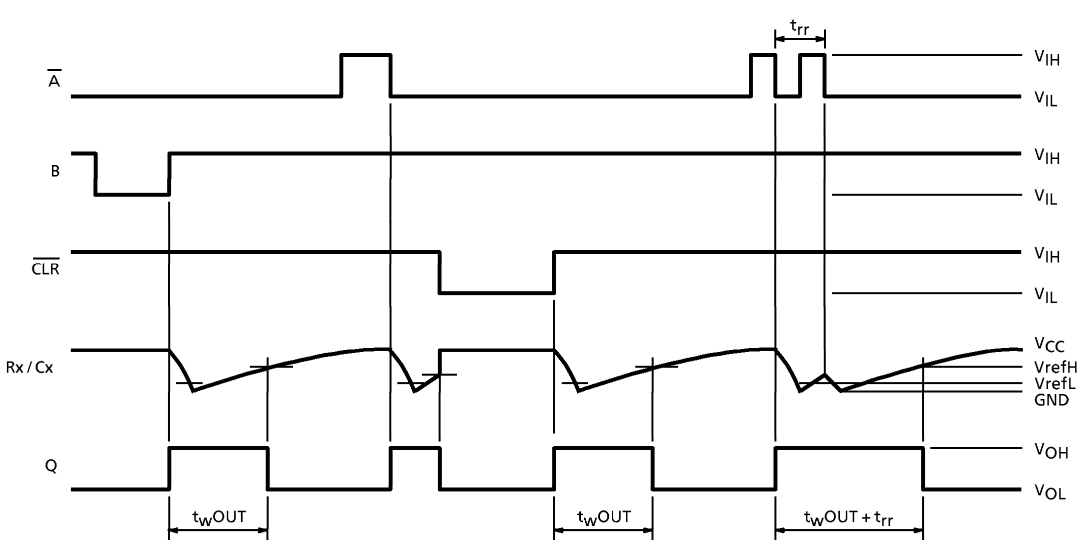
(I_{CC}' : Active Supply Current)

(Duty : %)

IEC LOGIC SYMBOL

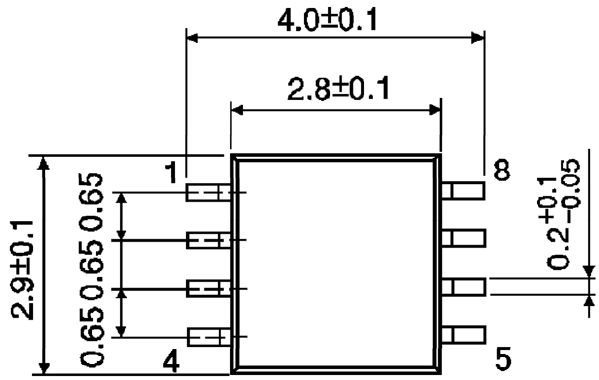


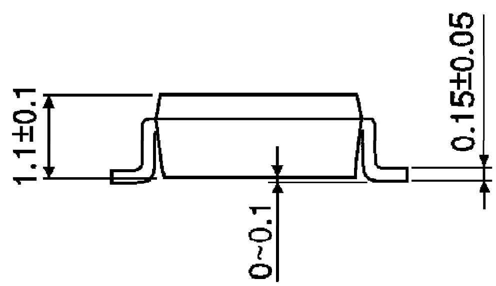
Timing Chart



PACKAGE DIMENSIONS

SSOP8-P-0.65 Unit : mm

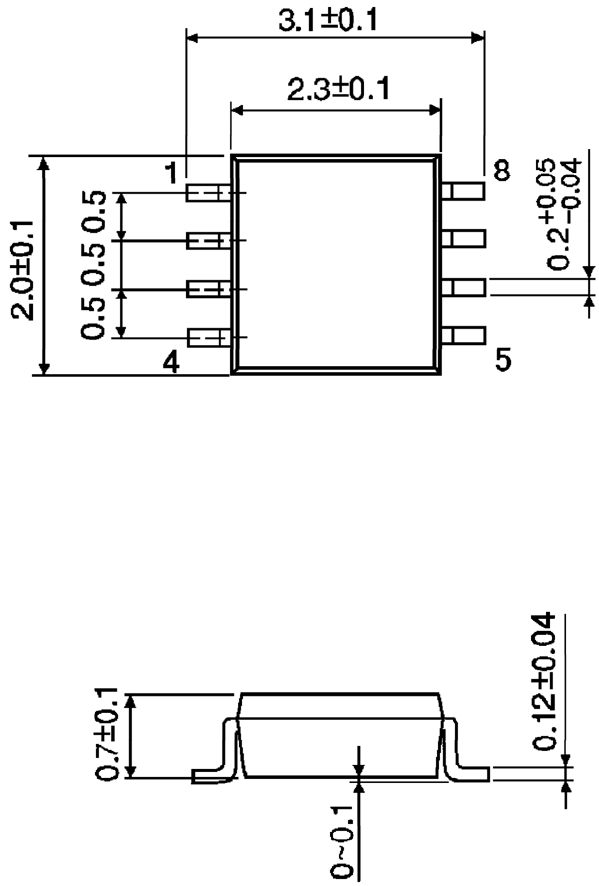




Weight : 0.02g (Typ.)

PACKAGE DIMENSIONS

SSOP8-P-0.50A Unit : mm



Weight : 0.01g (Typ.)

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