		REVISIONS		
LTR	DESCRIPTION		DATE	APPROVED
A	Change to military drawing format. Change from a suggested source drawing to an approved source drawing. Add CAGE 34335 and device type 02. Add case outline letters K, L, X, and 3. Change drawing CAGE to 67268.		15 Jan. 1988	M. A. Frye
B	Updated boilerplate. Removed programming specifics from drawing. Separated source bulletin from body of drawing. - glg		01 Aug 2000	Raymond Monnin
C	Correction to marking paragraph 3.5, updated boilerplate paragraphs. ksr		02 Mar 2005	Raymond Monnin

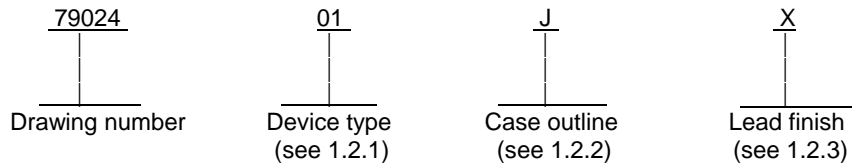THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268

REV																		
SHEET																		
REV																		
SHEET																		

REV STATUS		REV	C	C	C	C	C	C	C	C	C	C			
OF SHEETS		SHEET	1	2	3	4	5	6	7	8	9	10			

PMIC N/A	PREPARED BY Rick C. Officer	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
STANDARD MICROCIRCUIT DRAWING	CHECKED BY Charles Reusing	http://www.dscc.dla.mil
THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	APPROVED BY Michael A. Frye	MICROCIRCUITS, MEMORY, DIGITAL, 8192 BIT, SWITCHABLE, SCHOTTKY, BIPOLAR PROM WITH TRI-STATE OUTPUT, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 13 August 1979	
AMSC N/A	REVISION LEVEL C	SIZE A	CAGE CODE **14933**	**79024**
		SHEET 1 OF 10		

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5962-E198-05

1. SCOPE

1.1 <u>Scope</u>. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 <u>Part or Identifying Number (PIN)</u>. The complete PIN shall be as shown in the following example:

<u>79024</u>	<u>01</u>	<u>J</u>	<u>X</u>
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 <u>Device type(s)</u>. The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit	Access time
01	<u>1/</u>	1K x 8-bit power switched bipolar PROM	90 ns
02	<u>1/</u>	1K x 8-bit power switched bipolar PROM	75 ns

1.2.2 <u>Case outline(s)</u>. The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	dual-in-line package
K	GDFP2-F24 or CDFP3-F24	24	flat package
L	GDIP3-T24 or CDIP4-T24	24	dual-in-line package
X	CQCC1-N32	32	rectangular chip carrier package
3	CQCC1-N28	28	square leadless chip carrier package

1.2.3 <u>Lead finish</u>. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 <u>Absolute maximum ratings</u>.

Supply voltage range .... -0.5 V dc to +7.0 V dc
Address/enable Input voltages .... -0.5 V dc to +5.5 V dc
Address/enable Input current .... -30 mA dc to +5.5 mA dc
Storage temperature range .... -65°C to +150°C
Lead temperature (soldering, 10 seconds) .... +300°C
Thermal resistance, junction-to-case (Θ_{JC}) .... See MIL-STD-1835

1.4 <u>Recommended operating conditions</u>.

Case operating temperature range (T_C) .... -55°C to +125°C
Supply voltage range (V_{CC}) .... 4.5 V dc to 5.5 V dc

2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103.

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DEPARTMENT OF DEFENSE SPECIFICATION

    MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

    MIL-STD-883   -   Test Method Standard Microcircuits.
    MIL-STD-1835 -   Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

    MIL-HDBK-103 -   List of Standard Microcircuit Drawings.
    MIL-HDBK-780 -   Standard Microcircuit Drawings.

  (Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

   2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

   3. REQUIREMENTS

   3.1 Item requirements The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturer's approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

   3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

   3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

   3.2.2 Unprogrammed devices. Testing to the applicable truth table, or alternate testing as specified in 4.3.1d, shall be used for unprogrammed devices for contracts involving no altered item drawing. When testing is required per 4.3 herein, the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

   3.2.3 Programmed devices. The truth table for programmed devices shall be specified by an altered item drawing.

   3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

   3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

   3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

   3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

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TABLE I. <u>Electrical performance characteristics</u>.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	$V_{IL} = 0.8\ V$, $V_{IH} = 2.0\ V$ $I_{OH} = -2.0\ mA$, $V_{CC} = 4.5\ V$	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	$V_{IL} = 0.8\ V$, $V_{IH} = 2.0\ V$ $I_{OL} = 16\ mA$, $V_{CC} = 4.5\ V$	1, 2, 3	All		0.5	V
Low level input voltage	V_{IL}	$V_{CC} = 5.5\ V$	1, 2, 3	All		0.8	V
Input clamp voltage	V_{IC}	$V_{CC} = 4.5\ V$, $I_{IN} = -18\ mA$, Ambient temperature = 25°C	1, 2, 3	All		0.8	V
Input threshold voltage	V_{IH}	$V_{CC} = 4.5\ V$	1, 2, 3	All	2.0		V
Address/enable input	I_{IH}	$V_{IH} = 5.5\ V$	1, 2, 3	All		40	µA
Address/enable input	I_{IL}	$V_{IN} = 0.45\ V$	1, 2, 3	All	-1.0	-250	µA
Output short-circuit current 1/ 2/	I_{OS}	$V_{OUT} = 0.2\ V$ 1/	1, 2, 3	All	-12	–100	mA
Output disable current	I_{OHE}	$V_{CC} = 5.5\ V$, $V_{OUT} = 2.4\ V$	1, 2, 3	All		40	µA
Output disable current	I_{OLE}	$V_{OL} = 0.45\ V$, $V_{OUT} = 5.5\ V$ 2/	1, 2, 3	All		-40	µA
Supply current	I_{CC}	$V_{CC} = 5.5\ V$ Disabled	1, 2, 3	All		80	mA
		All inputs grounded Enabled				185	
Input capacitance	C_{IN}	$V_{IN} = 2.0\ V\ dc$; f = 1 MHz Ambient temperature = 25°C	4	All		8	pF
Address access time	t_{AVQV}	See figure 2 and 3	9, 10, 11	01		90	ns
				02		75	
Chip power-down delay to tri-state	t_{GVQZ}	See figure 2 and 3	9, 10, 11	All		50	ns
Chip power-up access time	t_{GVQV}	See figure 2 and 3	9, 10, 11	01		115	ns
				02		225	

1/ Not more than one output shall be shorted at a time for a maximum duration of one second.
2/ Device is in the three state.

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3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, Appendix A.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing..

3.9 Verification and review. DSCC, DSCC's agent and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

  a. Burn-in test (method 1015 of MIL-STD-883).

    (1) Test condition C, D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

    (2) T_A = +125°C, minimum.

  b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.
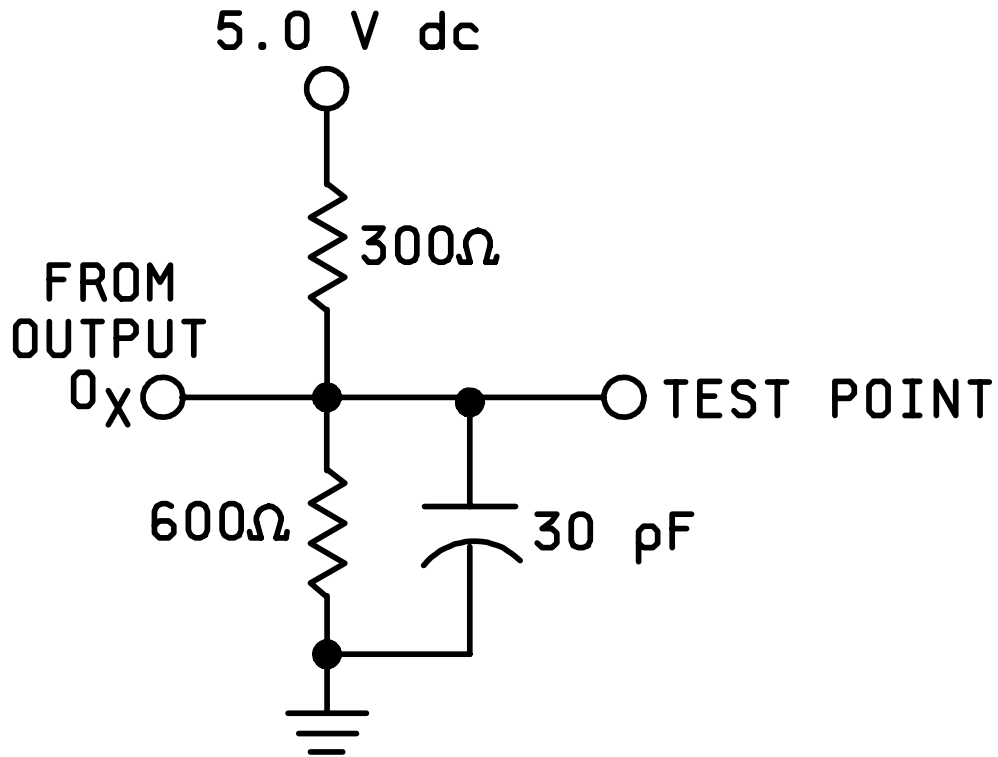
  a. Tests shall be as specified in table II herein.

  b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

  c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

  d. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9. 10, and 11. Either of two techniques is acceptable:

    (1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing per the sampling plan specified in MIL-STD-883, method 5005.

    (2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming. If more than 2 devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than 2 total devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

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Device Types		All		
Case Outlines	J, K, L		X	3
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Symbol
1	A7	1	NC	NC
2	A6	2	NC	A7
3	A5	3	A7	A6
4	A4	4	A6	A5
5	A3	5	A5	A4
6	A2	6	A4	A3
7	A1	7	A3	A2
8	A0	8	A2	A1
9	Q0	9	A1	A0
10	Q1	10	A0	NC
11	Q2	11	NC	Q0
12	VSS	12	Q0	Q1
13	Q3	13	Q1	Q2
14	Q4	14	Q2	VSS
15	Q5	15	NC	NC
16	Q6	16	VSS	Q3
17	Q7	17	Q3	Q4
18	E4	18	NC	Q5
19	E3	19	Q4	Q6
20	$\overline{E2}$	20	Q5	Q7
21	$\overline{E1}$	21	Q6	NC
22	A9	22	Q7	E4
23	A8	23	NC	E3
24	VCC	24	E4	$\overline{E2}$
25	- - -	25	E3	$\overline{E1}$
26	- - -	26	$\overline{E2}$	A9
27	- - -	27	NC	A8
28	- - -	28	$\overline{E1}$	VCC
29	- - -	29	A9	- - -
30	- - -	30	A8	- - -
31	- - -	31	NC	- - -
32	- - -	32	VCC	- - -

FIGURE 1. <u>Terminal connections</u>.

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Device type 01
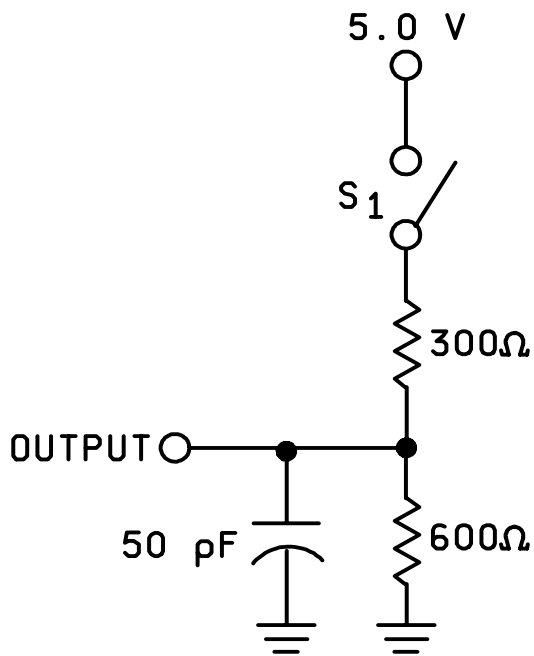

5.0 V dc

300Ω

FROM
OUTPUT
0ₓ

600Ω

30 pF

TEST POINT

NOTES:
1. The tolerance for all load components is ±5 percent.
2. The load capacitance includes the test jig and probe capacitances.
3. All device test loads should be located within two inches of device output pin.
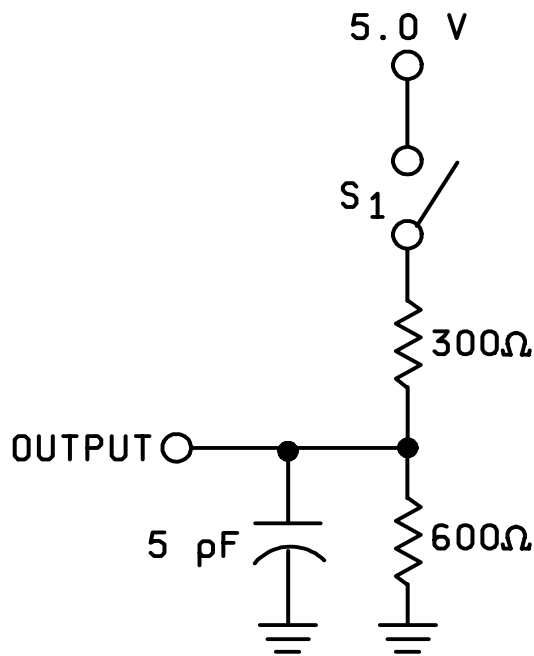4. Use this circuit or equivalent to test the outputs.

FIGURE 2. AC test load circuit.

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Device type 02

Output load for all switching tests except t_{GVQZ}.

Output load for t_{GVQZ}.

NOTES:
1. All device test loads should be located within two inches of device output pin.
2. S_1 is open for output data high to high-Z and high-Z to output data high tests.
    S_1 is closed for all other switching tests.
3. The load capacitance includes all stray and fixture capacitance.

FIGURE 2. AC test load circuit - continued.

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ADDRESSES — V_{IH} / V_{IL} — 1.5 V

OUTPUTS — V_{OH} / V_{OL} — 1.5 V

t_{AVQV}

E_3, E_4
POWER DOWNS
$\overline{E}_1$, $\overline{E}_2$ — 1.5 V — 1.5 V — V_{IH} / V_{IL}

OUTPUTS — TS

t_{GVQV} t_{GVQZ}

FIGURE 3. Switching time definitions.

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TABLE II. Electrical test requirements. 1/ 2/

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

    *   PDA applies to subgroup 1.

4.3.2 Groups C and D inspections.

    a. End-point electrical parameters shall be as specified in table II herein.

    b. Steady-state life test conditions, method 1005 of MIL-STD-883.

    (1) Test condition C, D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

    (2) T_A = +125°C, minimum.

    (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone 614-692-0547.

6.6 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02 Mar 2005

Approved sources of supply for SMD 79024 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
7902401JA	0C7V7 3/	R29633 29633DMB
	3/	HM-7681P-8
7902402JA	0C7V7 3/	R29633 AM27PS181/BJA
7902402KA	0C7V7 3/	R29633 AM27PS181/BKA
79024023A	0C7V7 3/	R29633 AM27PS181/B3A
7902402XA	0C7V7 3/	R29633 AM27PS181/BUA
7902402LA	0C7V7 3/	R29633 AM27PS181/BLA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No longer available from an approved source.

Vendor CAGE
 number

Vendor name
and address

0C7V7

QP Semiconductor.
2945 Oakmead Village Court
Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.