| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Boilerplate update, part of 5 year review. ksr | 06-12-05 | Raymond Monnin |

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

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| REV | | | | | | | | | | | | | | | | | | | | |
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| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV STATUS | | | | REV | | | A | A | A | A | A | A | A | A | A | A | | | | |
| OF SHEETS | | | | SHEET | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | | | | |

PMIC N/A

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DRAWING APPROVAL DATE
92-09-11

REVISION LEVEL
A

**DEFENSE SUPPLY CENTER COLUMBUS**
**COLUMBUS, OHIO 43218-3990**
**http://www.dscc.dla.mil**

# STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

# MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 4K X 8 UVEPROM, MONOLITHIC SILICON

| SIZE | CAGE CODE | |
|---|---|---|
| A | **67268** | **5962-90658** |

SHEET 1 OF 10

DSCC FORM 2233
APR 97

5962-E013-07

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

| 5962-90658 | 01 | J | A |
|---|---|---|---|
| Drawing number | Device type (see 1.2.1) | Case outline (see 1.2.2) | Lead finish (see 1.2.3) |

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function | Acess time |
|---|---|---|---|
| 01 | 57C43C-70 | 4K x 8-bit UVEPROM | 70 ns |
| 02 | 57C43C-55 | 4K x 8-bit UVEPROM | 55 ns |
| 03 | 57C43C-45 | 4K x 8-bit UVEPROM | 45 ns |
| 04 | 57C43C-35 | 4K x 8-bit UVEPROM | 35 ns |

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| J | GDIP1-T24 or CDIP2-T24 | 24 | Dual-in-line 1/ |
| K | GDFP2-F24 or CDFP3-F24 | 24 | Flat pack 1/ |
| L | GDIP3-T24 or CDIP4-T24 | 24 | Dual-in-line 1/ |
| 3 | CQCC1-N28 | 28 | Square leadless chip carrier 1/ |

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Voltage range on any pin with respect to ground ..... -0.6 V dc to +7.0 V dc
$V_{pp}$ range with respect to ground ..... -0.6 V dc to +14.0 V dc
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation ($P_D$) ..... 1 W
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case ($\theta_{JC}$) ..... See MIL-STD-1835
Junction temperature ($T_J$) 2/ ..... +150°C
Temperature (under bias) range ..... -55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage range ($V_{CC}$) ..... +4.5 V dc to +5.5 V dc
Ground voltage (GND) ..... 0 V dc
Input high voltage ($V_{IH}$) ..... 2.0 V dc minimum
Input low voltage ($V_{IL}$) ..... 0.8 V dc maximum
Case operating temperature range ($T_C$) ..... -55°C to +125°C

1/ Lid shall be transparent to permit ultraviolet light erasure.

2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, C, or D (see 4.3), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at least 25 percent of the total number of cells to any altered item drawing.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$4.5V \le V_{CC} \le 5.5V$<br>unless otherwise specified | Group A subgroups | Device types | Limits | | Units |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Input load current | $I_{LI}$ | $V_{IN}$ = 5.5 V and GND | 1,2,3 | All | -10 | 10 | µA |
| Input leakage current | $I_{IX}$ | $V_{IN} = V_{CC}$ and GND | 1,2,3 | All | -10 | 10 | µA |
| Output leakage current | $I_{OZ}$ | $V_{OUT}$ = 5.5 V and GND | 1,2,3 | All | -10 | 10 | µA |
| $V_{CC}$ active current (CMOS) | $I_{CC1}$ | CMOS inputs:<br>0 ± 0.3 V or $V_{cc}$ ±0.3 V 1/ | 1,2,3 | All | | 35 | mA |
| $V_{CC}$ active current (TTL) | $I_{CC2}$ | TTL inputs:<br>$V_{IL} \le 0.8$ V, $V_{IH} \ge 2.0$ V 1/ | 1,2,3 | All | | 50 | mA |
| Input high level voltage | $V_{IH}$ | | 1,2,3 | All | 2.0 | $V_{CC}$ +0.3 | V |
| Input low level voltage | $V_{IL}$ | | 1,2,3 | All | -0.1 | 0.8 | V |
| Ouput high voltage | $V_{OH}$ | $I_{OH}$ = -4 mA | 1,2,3 | All | 2.4 | | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 16 mA | 1,2,3 | All | | 0.4 | V |
| Functional tests | | See 4.3.1d | 7,8A,8B | All | | | |
| Input capacitance | $C_{IN}$ | $V_{IN}$ = 0 V 2/ ; $T_A$ = +25°C, f = 1 MHz | 4 | All | | 6 | pF |
| Output capacitance | $C_{OUT}$ | $V_{OUT}$ = 0 V 2/ ; $T_A$ = +25°C, f = 1 MHz | 4 | All | | 12 | pF |
| Address to output delay | $t_{ACC}$ | See figure 3 | 9,10,11 | 01 | | 70 | ns |
| | | | | 02 | | 55 | |
| | | | | 03 | | 45 | |
| | | | | 04 | | 35 | |
| $\overline{CS1}/V_{PP}$ to output delay | $t_{CS}$ | See figure 3 | 9,10,11 | 01-03 | | 25 | ns |
| | | | | 04 | | 20 | |
| Output disable to output float | $t_{DF}$ | See figure 3 3/ | 9,10,11 | All | | 25 | ns |
| Address to output hold | $t_{OH}$ | See figure 3 | 9,10,11 | All | 0 | | ns |

1/ Add 3 mA/MHz for ac power component.

2/ Tested initially and after any design or process changes that affect this parameter, and therefore shall be guaranteed to the limits specified in table I.

3/ May not be tested, but shall be guaranteed to the limits specified in table I.

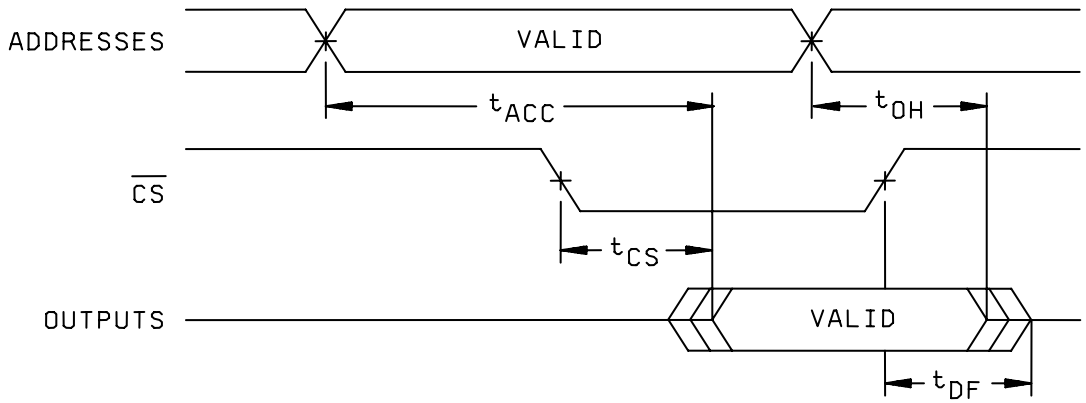
| Device types | All | |
|---|---|---|
| Case outlines | J, K, and L | 3 |
| Terminal number | Terminal symbol | |
| 1 | $A_7$ | NC |
| 2 | $A_6$ | $A_7$ |
| 3 | $A_5$ | $A_6$ |
| 4 | $A_4$ | $A_5$ |
| 5 | $A_3$ | $A_4$ |
| 6 | $A_2$ | $A_3$ |
| 7 | $A_1$ | $A_2$ |
| 8 | $A_0$ | $A_1$ |
| 9 | $O_0$ | $A_0$ |
| 10 | $O_1$ | NC |
| 11 | $O_2$ | $O_0$ |
| 12 | GND | $O_1$ |
| 13 | $O_3$ | $O_2$ |
| 14 | $O_4$ | GND |
| 15 | $O_5$ | NC |
| 16 | $O_6$ | $O_3$ |
| 17 | $O_7$ | $O_4$ |
| 18 | CS2 | $O_5$ |
| 19 | $A_{11}$ | $O_6$ |
| 20 | $\overline{CS1}$ /$V_{PP}$ | $O_7$ |
| 21 | $A_{10}$ | NC |
| 22 | $A_9$ | CS2 |
| 23 | $A_8$ | $A_{11}$ |
| 24 | $V_{CC}$ | $\overline{CS1}$ /$V_{PP}$ |
| 25 | --- | $A_{10}$ |
| 26 | --- | $A_9$ |
| 27 | --- | $A_8$ |
| 28 | --- | $V_{CC}$ |

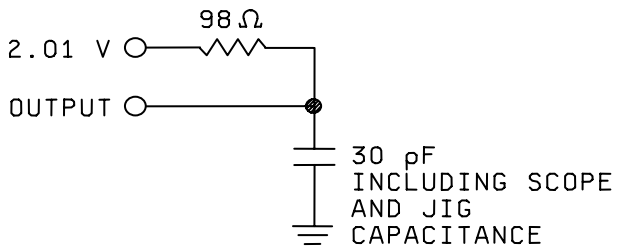
FIGURE 1. Terminal connections.

| Mode | $V_{CC}$ | $\overline{CS1}$ /$V_{PP}$ | CS2 | $O_0$-$O_7$ |
|---|---|---|---|---|
| Read | 5.0 V ±10% | $V_{IL}$ | $V_{IH}$ | $D_{OUT}$ |
| Output disable | 5.0 V ±10% | $V_{IH}$ | X 1/ | High Z |
| Output disable | 5.0 V ±10% | X 1/ | $V_{IL}$ | High Z |
| Program | $V_{CC}$ | $V_{PP}$ | X 1/ | $D_{IN}$ |
| Program verify | $V_{CC}$ | $V_{IL}$ | $V_{IH}$ | $D_{OUT}$ |

1/ X can be $V_{IL}$ or $V_{IH}$.

FIGURE 2. Truth table.




Test conditions (AC)

Input pulse levels: GND to 3.0 V
Input rise and fall times: ≤ 5 ns
Input timing reference levels: 1.5 V
Output reference levels: 1.5 V

FIGURE 3. AC read timing diagram and Test load circuit.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.6.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4 herein.

3.6.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 herein.

3.6.3 Verification of erasure of programmed EPROMS. When specified, devices shall be verified as either programmed to specified program or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.10 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done only for initial characterization and after any design or process changes which may affect reprogrammability of the device. This test shall consist of 25 program/erase cycles on 25 devices with the following conditions:

a. All devices selected for testing shall be programmed in accordance with 3.2.3.2 herein.

b. Verify pattern (see 3.6.3).

c. Erase (see 3.6.1).

d. Verify pattern erasure (see 3.6.3).

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method. 3/

(1) At +25°C, program greater than 95 percent of the bit locations, including the slowest programming cell. The remaining bits shall provide a worst case speed pattern.
(2) Bake, unbiased, for 72 hours at +140°C or for 32 hours at +150°C or for 8 hours at +200°C.
(3) At +25°C, perform a margin test using $V_m$ = +5.8 V to loose timing (i.e., $t_{ACC}$ = 1 µs).
(4) Perform dynamic burn-in accordance with 4.2a.
(5) At +25°C, perform a margin test using $V_m$ = +5.8 V.
(6) Perform electrical test in accordance with 4.2b.
(7) Erase in accordance with 3.6.1. Devices may be submitted to quality conformance inspection.
(8) Verify erasure in accordance with 3.6.3.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified except devices being submitted to groups B, C, and D testing.

d. As a minimum, subgroups 7, 8A, and 8B shall consist of verifying the EPROM pattern specified.

e. Subgroup 4 ($C_{IN}$ and $C_{OUT}$ measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

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3/ Steps 1 through 3 may be performed at the wafer level.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. All devices submitted for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified.

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 25 $Ws/cm^2$. The erasure time with this dosage is approximately 35 minutes using an ultraviolet lamp with a 12,000 $\mu W/cm^2$ power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 $Ws/cm^2$ (1 week at 12,000 $\mu W/cm^2$). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

TABLE II. Electrical test requirements.

| MIL-STD-883 test requirements | Subgroups (per method 5005, table I) |
|---|---|
| Interim electrical parameters (method 5004) | 1 |
| Final electrical test parameters for un-programmed devices (method 5004) | 1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 |
| Final electrical test parameters for programmed devices (method 5004) | 1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 |
| Group A test requirements (method 5005) | 1, 2, 3, 4**, (7, 8A, 8B)***, 9, 10, 11 |
| Groups C and D end-point electrical parameters (method 5005) | 2, 3, 7, 8A, 8B |

* PDA applies to subgroup 1 and 7.
** See 4.3.1e.
*** See 4.3.1d.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-12-05

Approved sources of supply for SMD 5962-90658 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor Similar PIN 2/ |
|---|---|---|
| 5962-9065801JA | 66579 | WS57C43C-70DMB |
| 5962-9065801JC | 66579 | WS57C43C-70DMB |
| 5962-9065801KA | 66579 | WS57C43C-70FMB |
| 5962-9065801KC | 66579 | WS57C43C-70FMB |
| 5962-9065801LA | 66579 | WS57C43C-70TMB |
| 5962-9065801LC | 66579 | WS57C43C-70TMB |
| 5962-90658013A | 66579 | WS57C43C-70CMB |
| 5962-90658013C | 66579 | WS57C43C-70CMB |
| 5962-9065802JA | 66579 | WS57C43C-55DMB |
| 5962-9065802JC | 66579 | WS57C43C-55DMB |
| 5962-9065802KA | 66579 | WS57C43C-55FMB |
| 5962-9065802KC | 66579 | WS57C43C-55FMB |
| 5962-9065802LA | 66579 | WS57C43C-55TMB |
| 5962-9065802LC | 66579 | WS57C43C-55TMB |
| 5962-90658023A | 66579 | WS57C43C-55CMB |
| 5962-90658023C | 66579 | WS57C43C-55CMB |
| 5962-9065803JA | 66579 | WS57C43C-45DMB |
| 5962-9065803JC | 66579 | WS57C43C-45DMB |
| 5962-9065803KA | 66579 | WS57C43C-45FMB |
| 5962-9065803KC | 66579 | WS57C43C-45FMB |
| 5962-9065803LA | 66579 | WS57C43C-45TMB |
| 5962-9065803LC | 66579 | WS57C43C-45TMB |
| 5962-90658033A | 66579 | WS57C43C-45CMB |
| 5962-90658033C | 66579 | WS57C43C-45CMB |
| 5962-9065804JA | 66579 | WS57C43C-35DMB |
| 5962-9065804JC | 66579 | WS57C43C-35DMB |
| 5962-9065804KA | 66579 | WS57C43C-35FMB |
| 5962-9065804KC | 66579 | WS57C43C-35FMB |

See notes at end of table.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor Similar PIN 2/ |
|---|---|---|
| 5962-9065804LA | 66579 | WS57C43C-35TMB |
| 5962-9065804LC | 66579 | WS57C43C-35TMB |
| 5962-90658043A | 66579 | WS57C43C-35CMB |
| 5962-90658043C | 66579 | WS57C43C-35CMB |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 0C7V7 | QP Semiconductor<br>2945 Oakmead Village Court<br>Santa Clara, CA 95051 |

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.