CY7C281A

1K x 8 PROM

Features

- CMOS for optimum speed/power
- High speed
  - 25 ns (Commercial)
- Low power
  - 495 mW (Commercial)
- EPROM technology 100% programmable
- Slim 300-mil or standard 600-mil DIP or 28-pin LCC
- 5V ±10% V_{CC}, commercial and military
- TTL-compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding >2001V static discharge

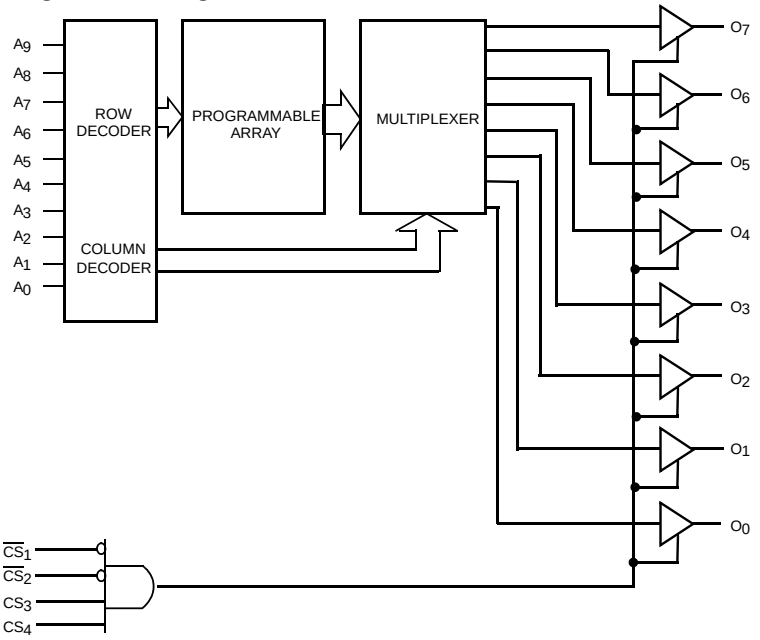
Functional Description

The CY7C281A is a high-performance 1024-word by 8-bit CMOS PROMs. It is packaged in 300-mil and 600-mil-wide packages respectively. The CY7C281A is also available in a 28-pin leadless chip carrier. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

The CY7C281A is a plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance, and programming yield. The EPROM cell requires only 12.5V for the super voltage, and low current requirements allow for gang programming. The EPROM cells allow each memory location to be tested 100% because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

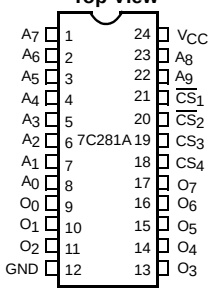
Reading is accomplished by placing an active LOW signal on $\overline{CS_1}$ and $\overline{CS_2}$, and active HIGH signals on CS_3 and CS_4. The contents of the memory location addressed by the address lines (A_0–A_9) will become available on the output lines (O_0–O_7).

LogicBlockDiagram

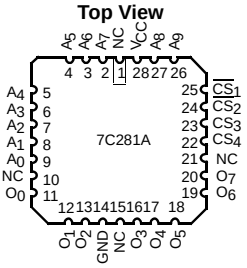


Pin Configurations

DIP
Top View



LCC/PLCC
Top View



Selection Guide

		7C281A-25	7C281A-30	Unit
Maximum Access Time		25	30	ns
Maximum Operating Current	Commercial	100	100	mA

Maximum Ratings[1]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12)..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage ..... –3.0V to +7.0V

DC Program Voltage (Pins 18, 20) 13.0V

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%

Electrical Characteristics Over the Operating Range[2,3]

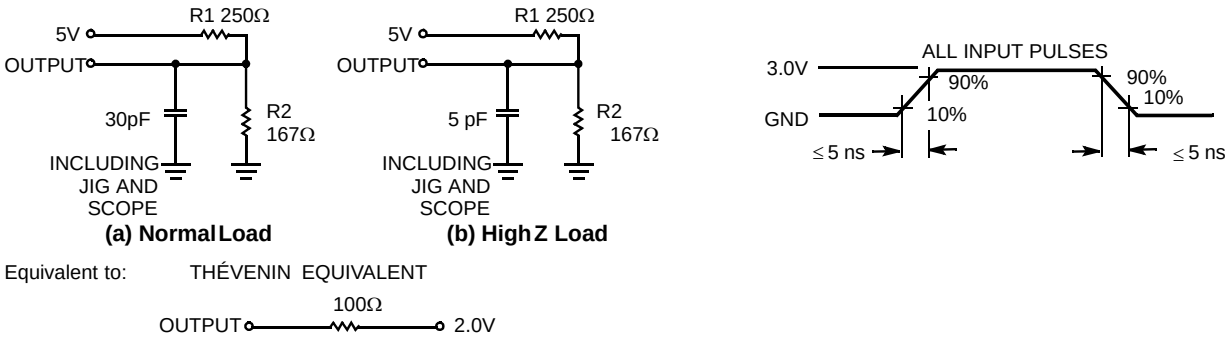
Parameter	Description	Test Conditions		7C281A-25 Min.	7C281A-25 Max.	7C281A-30 Min.	7C281A-30 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–10	+10	–10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND		–20	–90	–20	–90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		100		100	mA
V_{PP}	Program Voltage			12	13	12	13	V
V_{IHP}	Program HIGH Voltage			3.0		3.0		V
V_{ILP}	Program LOW Voltage				0.4		0.4	V
I_{PP}	Program Supply Current				50		50	mA

Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes
1. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. See the last page of this specification for Group A subgroup testing information.
3. See “Introduction to CMOS PROMs” in this Data Book for general information on testing.
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

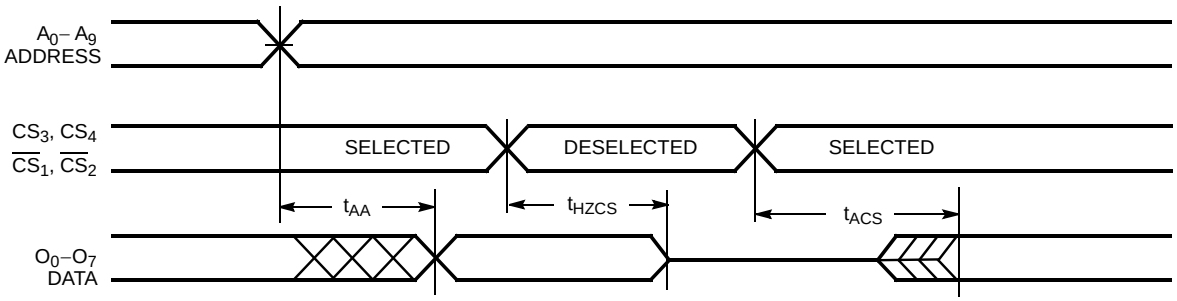
AC Test Loads and Waveforms[3]



Switching Characteristics Over the Operating Range[1,3]

Parameter	Description	7C281A-25		7C281A-30		Unit
		Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		25		30	ns
t_{HZCS}	Chip Select Inactive to High Z		15		20	ns
t_{ACS}	Chip Select Active to Output Valid		15		20	ns

Switching Waveforms



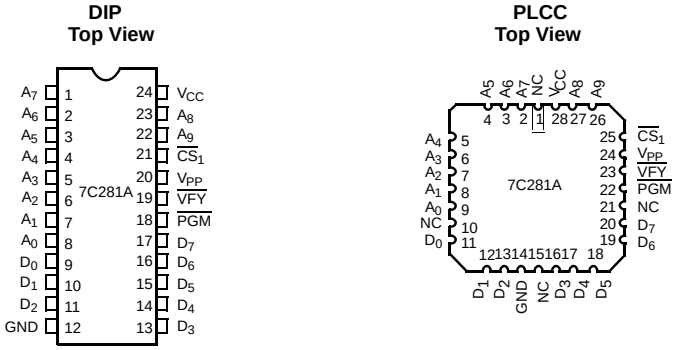
Programming Information

Programming support is available from Cypress as well as from a number of third party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[5]					
	Read or Output Disable	A_9–A_0	$\overline{CS_4}$	$\overline{CS_3}$	$\overline{CS_2}$	$\overline{CS_1}$	O_7–O_0
	Other	A_9–A_0	PGM	VFY	V_{PP}	$\overline{CS_1}$	D_7–D_0
Read		A_9–A_0	V_{IH}	V_{IH}	V_{IL}	V_{IL}	O_7–O_0
Output Disable		A_9–A_0	X	X	V_{IH}	X	High Z
Output Disable		A_9–A_0	X	V_{IL}	X	X	High Z
Output Disable		A_9–A_0	V_{IL}	X	X	X	High Z
Output Disable		A_9–A_0	X	X	X	V_{IH}	High Z
Program		A_9–A_0	V_{ILP}	V_{IHP}	V_{PP}	V_{ILP}	D_7–D_0
Program Verify		A_9–A_0	V_{IHP}	V_{ILP}	V_{PP}	V_{ILP}	O_7–O_0
Program Inhibit		A_9–A_0	V_{IHP}	V_{IHP}	V_{PP}	V_{ILP}	High Z
Intelligent Program		A_9–A_0	V_{ILP}	V_{IHP}	V_{PP}	V_{ILP}	D_7–D_0
Blank Check		A_9–A_0	V_{IHP}	V_{ILP}	V_{PP}	V_{ILP}	Zeros

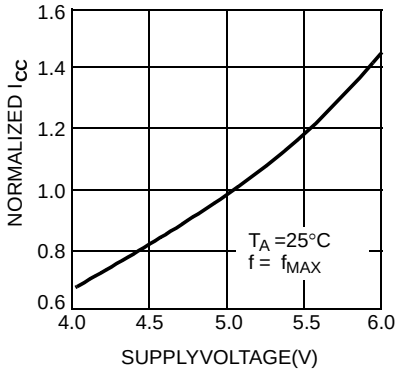
Figure 1. Programming Pinouts



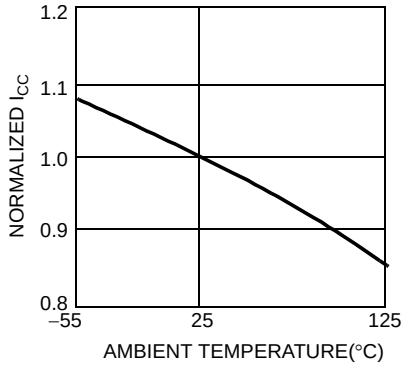
Note
5. X = “don’t care” but not to exceed V_{CC} ±5%.

Typical DC and AC Characteristics

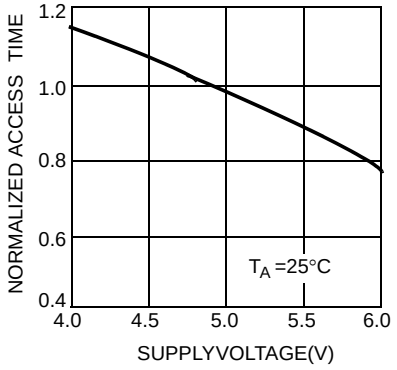
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



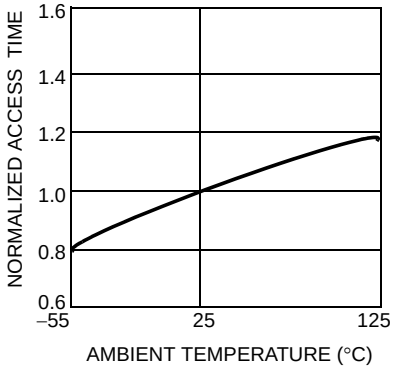
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



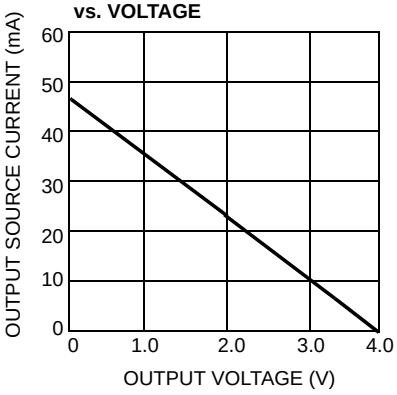
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



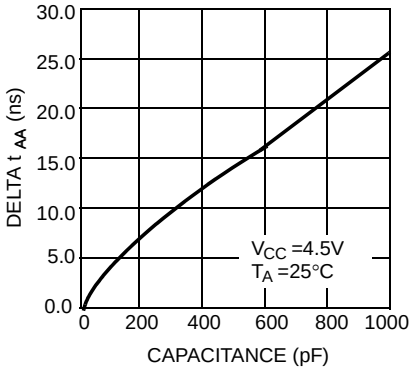
NORMALIZED ACCESSTIME vs.TEMPERATURE



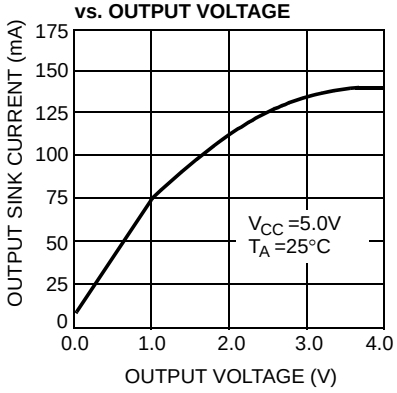
OUTPUT SOURCE CURRENT vs. VOLTAGE



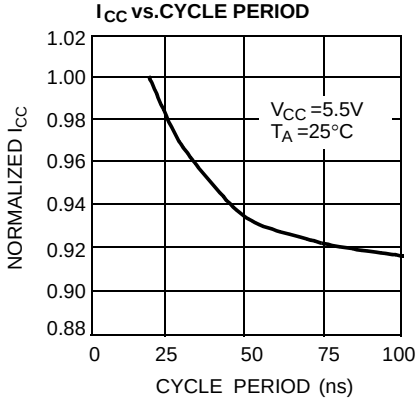
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



ICC vs.CYCLE PERIOD

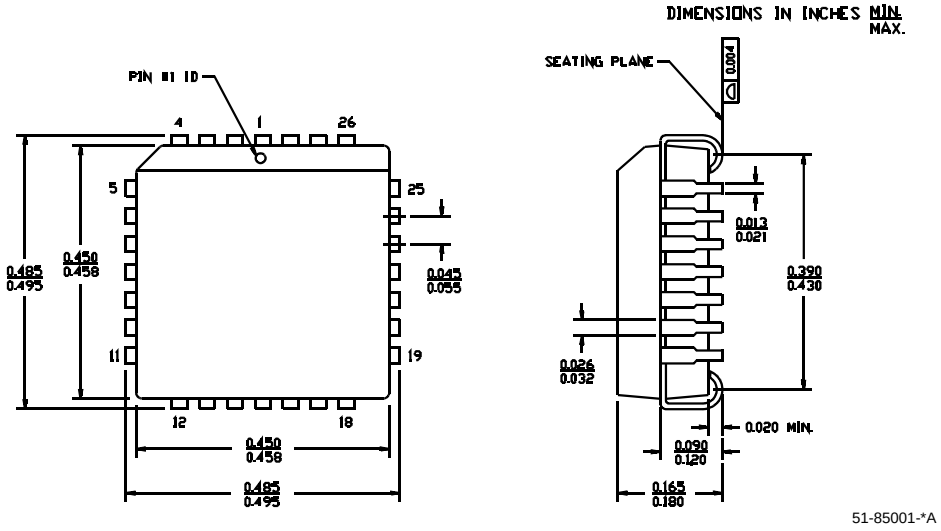


Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C281A-25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
30	CY7C281A-30PC	P13	24-Lead (300-Mil) Molded DIP	Commercial

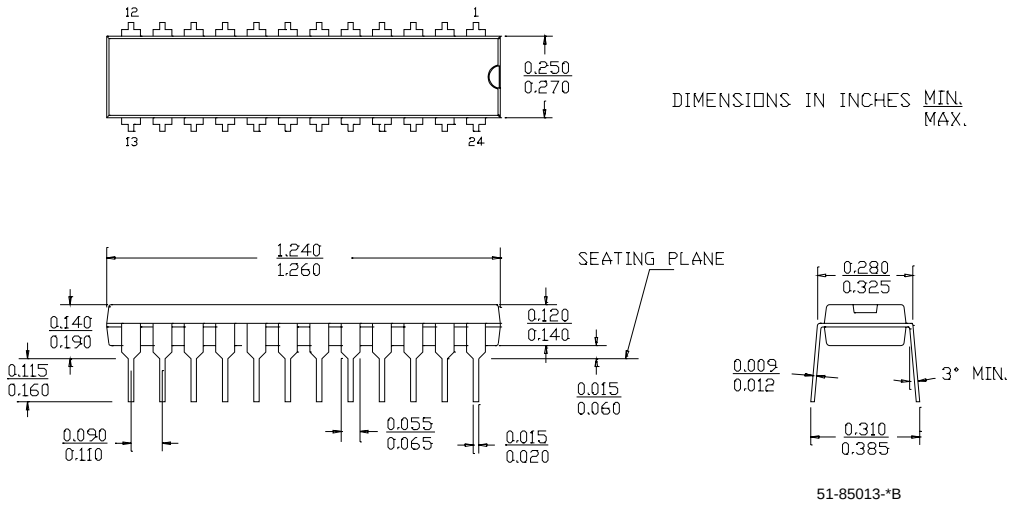
Package Diagrams

Figure 2. 28-Lead Plastic Leaded Chip Carrier J64



Package Diagrams

Figure 3. 24-Lead (300-Mil) PDIP P13



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Document History Page

Document Title: CY7C281A 1K x 8 PROM Document Number: 38-04003				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	113859	03/06/02	DSG	Changed from Spec number: 38-00227 to 38-04003
*A	118902	10/09/02	GBI	Updated ordering information
*B	122244	12/27/02	RBI	Added power up requirements to Maximum ratings information
*C	499538	See ECN	PCI	Updated ordering information