REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current requirements. Removed programming specifics from drawing. Editorial changes throughout. gap	01-02-07	Raymond Monnin
B	Boilerplate update and part of five year review. tcr	07-02-13	Joseph Rodenbeck

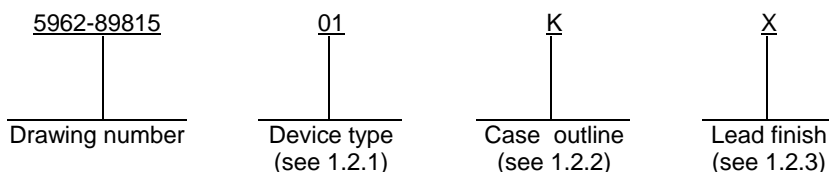THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																
SHEET																
REV																
SHEET																
REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B			
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A	PREPARED BY James E. Jamison	
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A		**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
	CHECKED BY Charles Reusing	
	APPROVED BY Michael A. Frye	MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 2K X 8 REGISTERED UVEPROM, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 91-12-30	
	REVISION LEVEL B	SIZE A

SIZE A	CAGE CODE **67268**	**5962-89815**
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5962-E261-07

1. SCOPE

1.1 <u>Scope</u>. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 <u>Part or Identifying Number (PIN)</u>. The complete PIN is as shown in the following example:

<pre>
5962-89815   01   K   X
     | | | |
 _____   _____   _____   _____
Drawing number   Device type   Case outline   Lead finish
                   (see 1.2.1)   (see 1.2.2)   (see 1.2.3)
</pre>

1.2.1 <u>Device type(s)</u>. The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Setup time
01	7C245A-35	2K x 8 registered UV EPROM	35 ns
02	7C245A-25	2K x 8 registered UV EPROM	25 ns
03	7C245A-18	2K x 8 registered UV EPROM	18 ns

1.2.2 <u>Case outline(s)</u>. The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or CDFP3-F24	24	flat package 1/
L	GDIP3-T24 or CDIP4-T24	24	dual-in-line package 1/
3	CQCC1-N28	28	square leadless chip carrier package 1/

1.2.3 <u>Lead finish</u>. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 <u>Absolute maximum ratings</u>.

Supply voltage range (V_{CC}) .... -0.5 V dc to +7.0 V dc
DC voltage applied to outputs in high Z state .... -0.5 V dc to +7.0 V dc
DC input voltage .... -3.0 V dc to +7.0 V dc
DC program voltage .... 13.0 V dc
Maximum power dissipation 2/ .... 1.0 W
Lead temperature (soldering, 10 seconds) .... +260°C
Thermal resistance, junction-to-case (θ_{JC}) .... See MIL-STD-1835
Junction temperature (T_J) .... +175°C
Storage temperature range .... -65°C to +150°C
Temperature under bias .... -55°C to +125°C
Endurance .... 10 cycles/byte, minimum
Data retention .... 10 years, minimum

1.4 <u>Recommended operating conditions</u>.

Supply voltage range (V_{CC}) .... +4.5 V dc to +5.5 V dc
Ground voltage (GND) .... 0 V dc
Input high voltage (V_{IH}) .... 2.0 V dc minimum
Input low voltage (V_{IL}) .... 0.8 V dc maximum
Case operating temperature range (T_C) .... -55°C to +125°C

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883   -   Test Method Standard Microcircuits.
MIL-STD-1835 -   Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 -   List of Standard Microcircuit Drawings.
MIL-HDBK-780 -   Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

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3.2.3.1 <u>Unprogrammed or erased devices</u>. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in screening (see 4.2) group A, C, or D (see 4.3), the devices shall be programmed by the manufacturer prior to test with a checkerboard pattern or equivalent (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.3.2 <u>Programmed devices</u>. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 <u>Electrical performance characteristics</u>. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 <u>Marking</u>. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 <u>Certification/compliance mark</u>. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 <u>Certificate of compliance</u>. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 <u>Certificate of conformance</u>. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 <u>Notification of change</u>. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 <u>Verification and review</u>. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 <u>Processing EPROMS</u>. All testing requirements and quality assurance provisions herein, shall be satisfied by the manufacturer prior to delivery.

3.10.1 <u>Erasure of EPROMS</u>. When specified, devices shall be erased in accordance with the procedures and characteristics specified by the manufacturer.

3.10.2 <u>Programmability of EPROMS</u>. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified by the manufacturer.

3.10.3 <u>Verification of programmed or erased EPROMs</u>. When specified, devices shall be verified as either programmed to a specified program, or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.11 <u>Data retention</u>. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

3.12 <u>Endurance</u>. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/, 2/ $-55°C \leq T_C \leq +125°C$ $4.5\ V \leq V_{CC} \leq 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Output high voltage	V_{OH}	$V_{CC} = 4.5\ V$, $I_{OH} = -4.0\ mA$ $V_{IN} = V_{IH}, V_{IL}$	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	$V_{CC} = 4.5\ V$, $I_{OL} = 16.0\ mA$ $V_{IN} = V_{IH}, V_{IL}$	1, 2, 3	All		0.4	V
Input high voltage 1/	V_{IH}		1, 2, 3	All	2.0		V
Input low voltage 1/	V_{IL}		1, 2, 3	All		0.8	V
Input leakage current	I_{IX}	$V_{IN} = V_{CC}$ to GND	1, 2, 3	All	-10	+10	μA
Output leakage current 3/	I_{OZ}	$V_{OUT} = V_{CC}$ to GND	1, 2, 3	All	-40	+40	μA
Output short circuit current 4/, 5/	I_{OS}	$V_{CC} = 4.5\ V$, and 5.5 V $V_{OUT} = 0.0\ V$	1, 2, 3	All	-20	-90	mA
Power supply current	I_{CC}	$\overline{E}/\overline{E}_S = V_{IL}$, $\overline{INIT} = V_{IH}$, Addresses cycling between 0 V and 3 V, $V_{CC} = 5.5\ V$, $f = \dfrac{1}{2t_{PWC}}$	1, 2, 3	All		120	mA
Input capacitance 5/	C_{IN}	$V_{CC} = 5.0\ V$, $V_{IN} = 0\ V$ $T_A = +25°C$, $f = 1\ MHz$ (see 4.3.1c)	4	All		10	pF
Output capacitance 5/	C_{OUT}	$V_{CC} = 5.0\ V$, $V_{OUT} = 0\ V$ $T_A = +25°C$, $f = 1\ MHz$ (see 4.3.1c)	4	All		10	pF
Functional tests		See 4.3.1e	7, 8	All			
Address setup to clock high	t_{SA}	See figures 3 and 4 6/	9, 10, 11	01	35		ns
				02	25		
				03	18		
Address hold from clock high	t_{HA}		9, 10, 11	All	0		ns
Clock high to valid output	t_{CO}		9, 10, 11	01		15	ns
				02, 03		12	

See footnotes at end of table.

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TABLE I. <u>Electrical performance characteristics</u> - Continued.

Test	Symbol	Conditions 1/, 2/ -55°C ≤ T_C ≤+125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Clock pulse width 5/	t_{PWC}	See figures 3 and 4 6/	9, 10, 11	01	20		ns
				02	15		
				03	12		
$\overline{E}_S$ setup to clock high 5/	t_{SES}		9, 10, 11	01	15		ns
				02	12		
				03	10		
$\overline{E}_S$ hold from clock high 5/	t_{HES}		9, 10, 11	All	5		ns
Delay from $\overline{INIT}$ to valid output	t_{DI}		9, 10, 11	All		20	ns
$\overline{INIT}$ recovery to clock high	t_{RI}		9, 10, 11	01	20		ns
				02, 03	15		
$\overline{INIT}$ pulse width	t_{PWI}		9, 10, 11	01	20		ns
				02, 03	15		
Valid output from clock high 5/, 7/	t_{COS}		9, 10, 11	01		20	ns
				02, 03		15	
Inactive output from clock high 5/, 7/, 8/	t_{HZC}		9, 10, 11	01		20	ns
				02, 03		15	
Valid output from $\overline{E}$ low 9/	t_{DOE}		9, 10, 11	01		20	ns
				02, 03		15	
Inactive output from $\overline{E}$ high 5/, 8/, 9/	t_{HZE}		9, 10, 11	01		20	ns
				02, 03		15	

1/ These are absolute voltages with respect to device ground pin and include all overshoots due to system or tester noise.
2/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load on figure 3.
3/ For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
4/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
5/ This parameter tested initially and after any design or process changes which could affect this parameter, and therefore shall be guaranteed to the limits specified in table I.
6/ See figure 3, circuit A, for all switching characteristics except t_{HZ}.
7/ Applies only when the synchronous ($\overline{E}_S$) function is used.
8/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input with the output load on figure 3, circuit B.
9/ Applies only when the asynchronous ($\overline{E}$) function is used.

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Device types	All	
Case outlines	K, L	3
Terminal number	Terminal symbol	
1	A_7	NC
2	A_6	A_7
3	A_5	A_6
4	A_4	A_5
5	A_3	A_4
6	A_2	A_3
7	A_1	A_2
8	A_0	A_1
9	O_0	A_0
10	O_1	NC
11	O_2	O_0
12	GND	O_1
13	O_3	O_2
14	O_4	GND
15	O_5	NC
16	O_6	O_3
17	O_7	O_4
18	CP	O_5
19	$\overline{E}/\overline{E}_S$	O_6
20	$\overline{INIT}$	O_7
21	A_{10}	NC
22	A_9	CP
23	A_8	$\overline{E}/\overline{E}_S$
24	V_{CC}	$\overline{INIT}$
25	---	A_{10}
26	---	A_9
27	---	A_8
28	---	V_{CC}

FIGURE 1. Terminal connections.

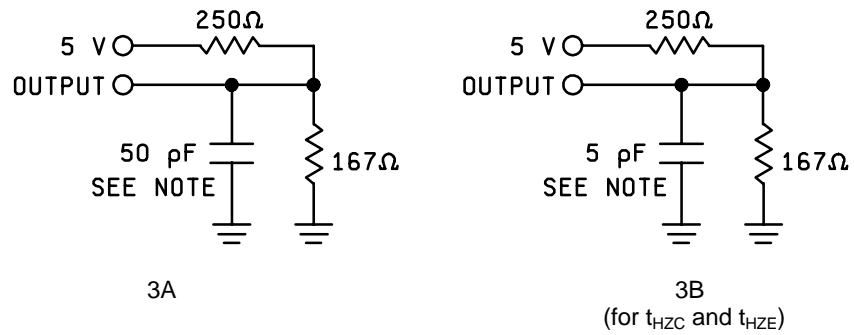|	Pin function					
Mode	A_3	CP	$\overline{E}/\overline{E}_S$	$\overline{INIT}$	A_0	Outputs
Read 1/ 2/ 3/	X	X	V_{IL}	V_{IH}	X	Data out
Output disable 1/ 4/	X	X	V_{IH}	V_{IH}	X	High Z

1/   X = Don't care.

2/   During read operation, the output latches are loaded on a "0" to "1" transition of CP.

3/   In the synchronous mode, pin $\overline{E}_S$ must be low prior to the "0" to "1" transition on CP that loads the register.

4/   In the synchronous mode, pin $\overline{E}_S$ must be high prior to the "0" to "1" transition on CP that loads the register.
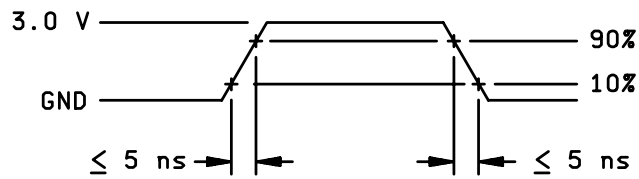
FIGURE 2. Truth table.

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3A

3B
(for t_{HZC} and t_{HZE})

OUTPUT LOAD

NOTE: including scope and jig. (minimum values)

Input pulse levels	GND to 3.0 V
Input rise and fall times	$\leq$ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 3. Output load circuit and test conditions.

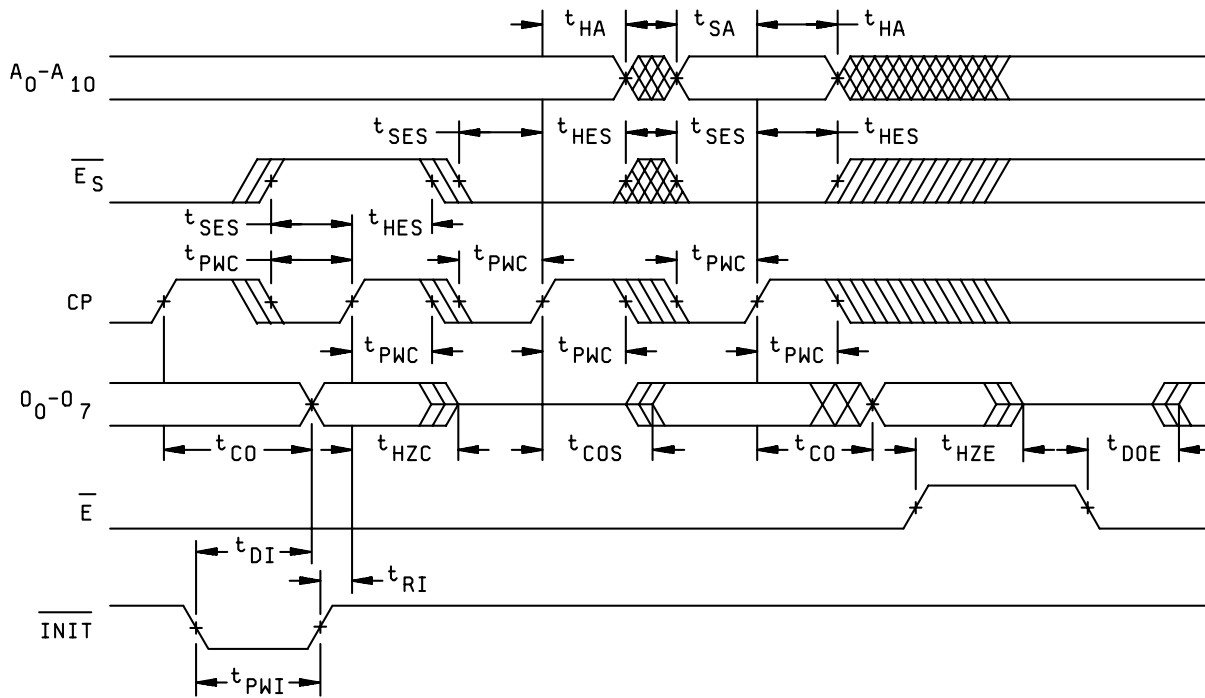| STANDARD MICROCIRCUIT DRAWING	SIZE **A**		**5962-89815**
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FIGURE 4. Switching waveforms.

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4. VERIFICATION

4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

  (1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

  (2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. <u>Electrical test requirements</u>.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**,7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

1/   * Indicates PDA applies to subgroups 1 and 7.
2/   Any or all subgroups may be combined when using high-speed testers.
3/   ** See 4.3.1c.

4.3 <u>Quality conformance inspection</u>. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 <u>Group A inspection</u>.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input or output capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

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d. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).

   e. Subgroups 7 and 8 shall include verification of the truth table and the EPROM pattern specified in 4.3.1d.

   4.3.2 <u>Groups C and D inspections</u>.

   a. End-point electrical parameters shall be as specified in table II herein.

   b. Steady-state life test conditions, method 1005 of MIL-STD-883.

      (1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

      (2) T_A = +125°C, minimum.

      (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

   c. All devices submitted for testing shall be programmed with a checkerboard pattern, or equivalent. After completion of all testing, the devices shall be erased and verified.

5. PACKAGING

5.1 <u>Packaging requirements</u>. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 <u>Record of users</u>. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 <u>Comments</u>. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 <u>Approved sources of supply</u>. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-02-13

Approved sources of supply for SMD 5962-89815 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8981501LA	0C7V7	WS57C45-35KMB
	0C7V7	QP7C245A-35WMB
	3/	CY7C245A-35WMB
5962-8981501KA	0C7V7	WS57C45-35HMB
	0C7V7	QP7C245A-35TMB
	3/	CY7C245A-35TMB
5962-89815013A	0C7V7	WS57C45-35ZMB
	0C7V7	QP7C245A-35QMB
	3/	CY7C245A-35QMB
5962-89815013C	0C7V7	WS57C45-35ZMB
5962-8981502LA	0C7V7	WS57C45-25KMB
	0C7V7	QP7C245A-25WMB
	3/	CY7C245A-25WMB
5962-8981502KA	0C7V7	WS57C45-25HMB
	0C7V7	QP7C245A-25TMB
	3/	CY7C245A-25TMB
5962-89815023A	0C7V7	WS57C45-25ZMB
	0C7V7	QP7C245A-25QMB
	3/	CY7C245A-25QMB

STANDARD MICROCIRCUIT DRAWING BULLETIN - continued.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-89815023C	0C7V7	WS57C45-25ZMB
5962-8981503LA	0C7V7	CY7C245A-18WMB
	0C7V7	QP7C245A-18WMB
	3/	CY7C245A-18WMB
5962-8981503KA	0C7V7	7C245A/KA
	0C7V7	QP7C245A-18TMB
	3/	CY7C245A-18TMB
5962-89815033A	0C7V7	QP7C245A-18QMB
	3/	CY7C245A-18QMB

1/ The lead finish shown for each PIN representing
    a hermetic package is the most readily available
    from the manufacturer listed for that part. If the
    desired lead finish is not listed contact the vendor
    to determine its availability.
2/ Caution. Do not use this number for item
    acquisition. Items acquired to this number may not
    satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE   Vendor name
  number   and address

  0C7V7   QP Semiconductor
                                         2945 Oakmead Village Ct.
                                         Santa Clara, CA 95051-0812

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