SN74LS682, SN74LS684, SN74LS688

8-Bit Magnitude Comparators

The SN74LS682, 684, 688 are 8-bit magnitude comparators. These device types are designed to perform comparisons between two eight-bit binary or BCD words. All device types provide $\overline{P = Q}$ outputs and the LS682 and LS684 have $\overline{P > Q}$ outputs also.

The LS682, LS684 and LS688 are totem pole devices. The LS682 has a 20 kΩ pullup resistor on the Q inputs for analog or switch data.

TYPE	$\overline{P = Q}$	$\overline{P > Q}$	OUTPUT ENABLE	OUTPUT CONFIGURATION	PULLUP
LS682	yes	yes	no	totem-pole	yes
LS684	yes	yes	no	totem-pole	no
LS688	yes	no	yes	totem-pole	no

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			– 0.4	mA
I_{OL}	Output Current – Low			24	mA

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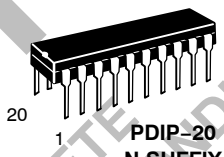
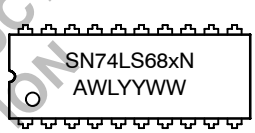
LOW POWER SCHOTTKY

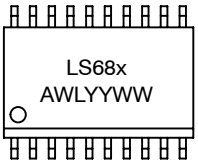


PDIP–20
N SUFFIX
CASE 738

MARKING DIAGRAMS



SOIC–20
DW SUFFIX
CASE 751D

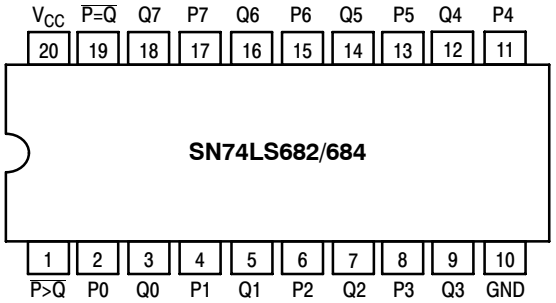


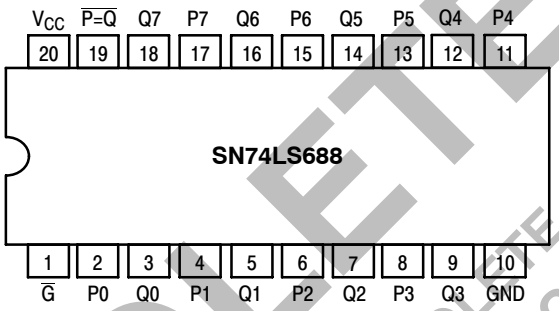
x = 2, 4, or 8
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
SN74LS682N	PDIP–20	1440 Units/Box
SN74LS682DW	SOIC–WIDE	38 Units/Rail
SN74LS682DWR2	SOIC–WIDE	2500/Tape & Reel
SN74LS684N	PDIP–20	1440 Units/Box
SN74LS684DW	SOIC–WIDE	38 Units/Rail
SN74LS684DWR2	SOIC–WIDE	2500/Tape & Reel
SN74LS688N	PDIP–20	1440 Units/Box
SN74LS688DW	SOIC–WIDE	38 Units/Rail
SN74LS688DWR2	SOIC–WIDE	2500/Tape & Reel

CONNECTION DIAGRAMS (TOP VIEW)





FUNCTION TABLE

INPUTS			OUTPUTS	
DATA	ENABLES			
P, Q	$\overline{G}$, $\overline{GT}$	$\overline{G2}$	$\overline{P = Q}$	$\overline{P > Q}$
P = Q	L	L	L	H
P > Q	L	L	H	L
P < Q	L	L	H	H
X	H	H	H	H

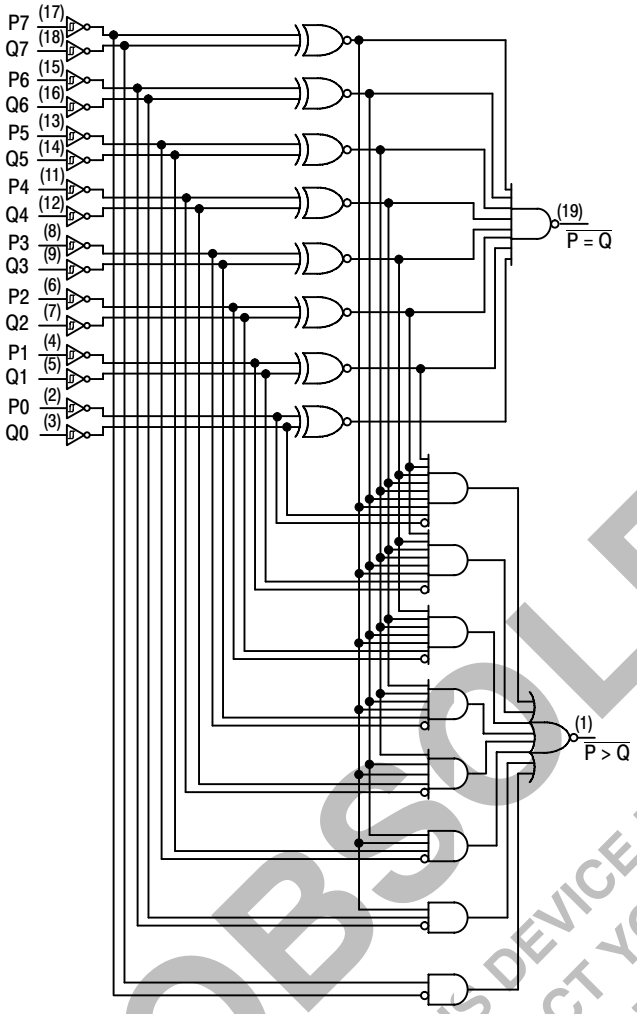
H = HIGH Level, L = LOW Level, X = Irrelevant

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

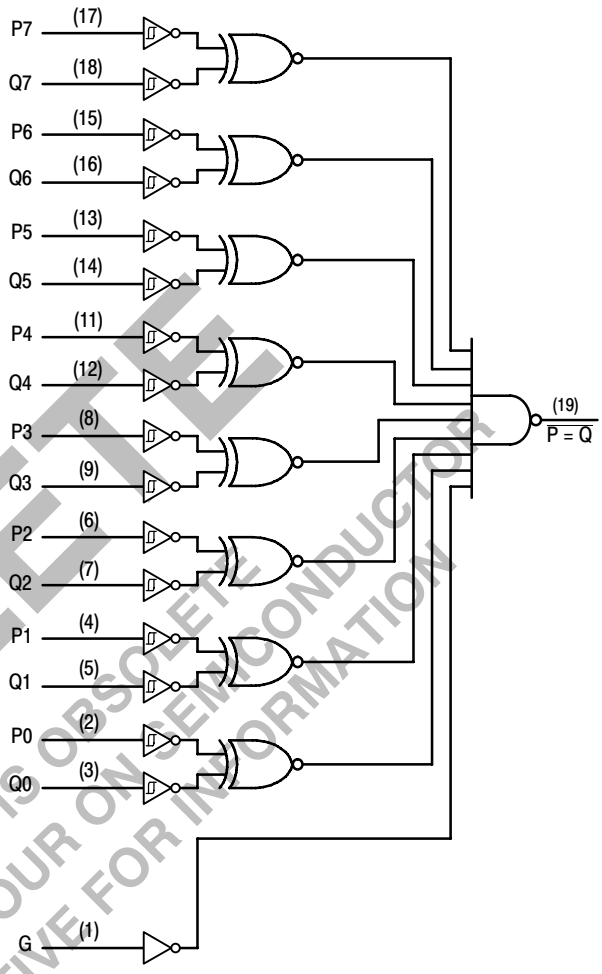
Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage		2.7	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage			0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
				0.35	0.5	V	I_{OL} = 24 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
		LS682-Q Inputs			0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
		Others			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current	LS682-Q Inputs			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
		Others			−0.2	mA		
I_{OS}	Short Circuit Current (Note 1)		−30		−130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current	LS682			70	mA	V_{CC} = MAX	
		LS684			65	mA		
		LS688			65	mA		

1. Not more than one output should be shorted at a time, nor for more than 1 second.

LOGIC DIAGRAMS



SN74LS682 and LS684



SN74LS688

AC CHARACTERISTICS (T_A = 25°C)

SN74LS682

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P = Q}$		13 15	25 25	ns	V_{CC} = 5.0 V C_L = 45 pF R_L = 667 Ω
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P = Q}$		14 15	25 25	ns	
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P > Q}$		20 15	30 30	ns	
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P > Q}$		21 19	30 30	ns	

SN74LS684

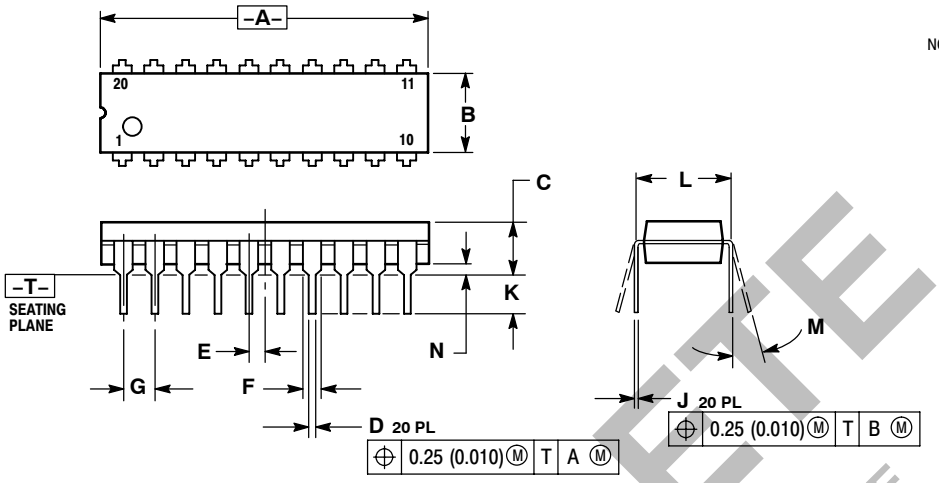
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P = Q}$		15 17	25 25	ns	V_{CC} = 5.0 V C_L = 45 pF R_L = 667 Ω
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P = Q}$		16 15	25 25	ns	
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P > Q}$		22 17	30 30	ns	
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P > Q}$		24 20	30 30	ns	

SN74LS688

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P = Q}$		12 17	18 23	ns	V_{CC} = 5.0 V C_L = 45 pF R_L = 667 Ω
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P = Q}$		12 17	18 23	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{G}$, $\overline{G1}$ to $\overline{P = Q}$		12 13	18 20	ns	

PACKAGE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 738−03
ISSUE E

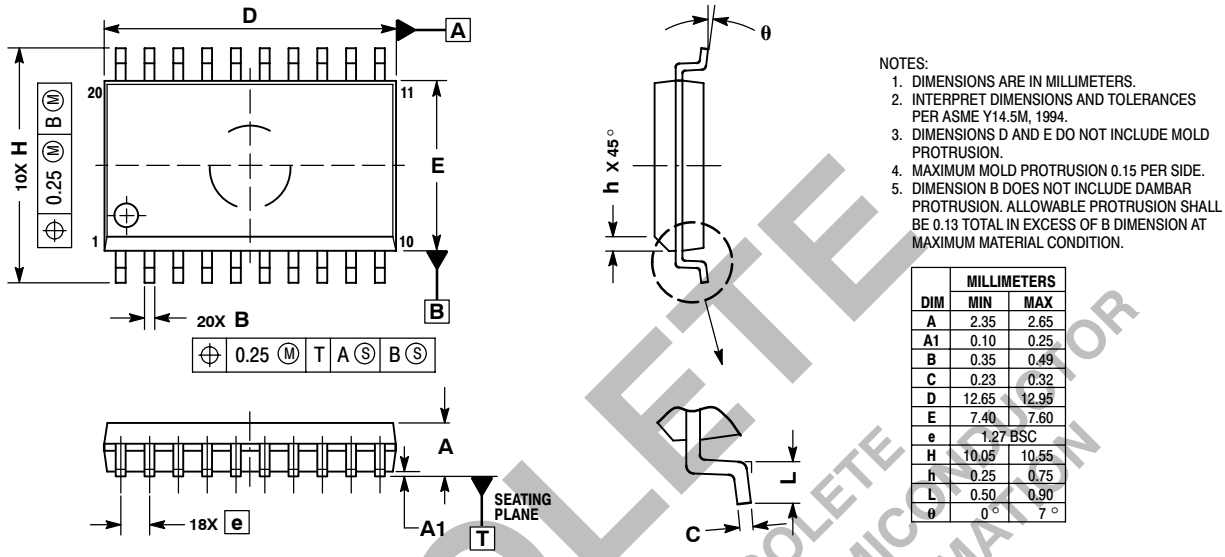


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

PACKAGE DIMENSIONS

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–05
ISSUE F



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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SN74LS682/D