DUAL 2:1 AND 1:2 DIFFERENTIAL-TO-LVDS MULTIPLEXER

ICS85454

General Description

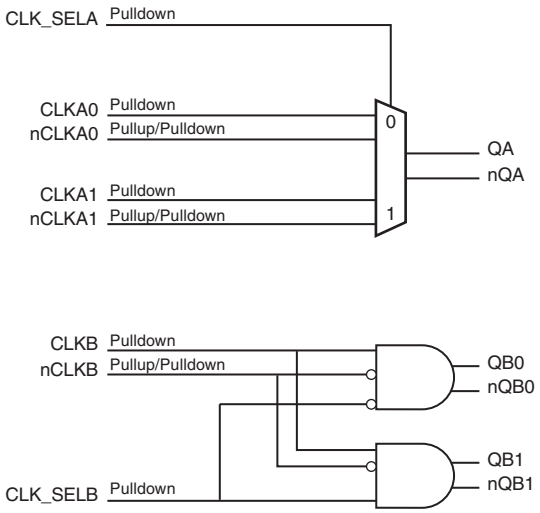
The ICS85454 is a dual 2:1 and 1:2 Multiplexer and a member of the HiPerClockS™ family of high performance clock solutions from IDT. The 2:1 Multiplexer allows one of 2 inputs to be selected onto one output pin and the 1:2 MUX switches one input to one of two outputs. This device is useful for multiplexing multi-rate Ethernet PHYs which have 100 M bit and 1000 bit transmit/receive pairs onto an optical SFP module which has a single trasmit/receive pair. See Application Section for further information.

The ICS85454 is optimized for applications requiring very high performance and has a maximum operating frequency of 2.5GHz. The device is packaged in a small, 3mm x 3mm VFQFN package, making it ideal for use on space-constrained boards.

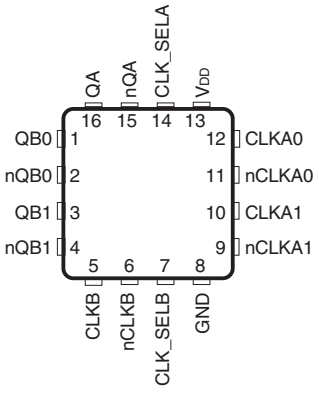
Features

- Three LVDS outputs
- Three differential clock inputs
- CLKx pair can accept the following differential input levels: LVPECL, LVDS, CML
- Maximum output frequency: 2.5GHz
- Additive phase jitter, RMS: 0.11ps (typical)
- Part-to-part skew: 200ps (maximum)
- Propagation delay: 425ps (maximum), QA/nQA
  375ps (maximum), QBx/nQBx
- Full 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS85454
16-Lead VFQFN
3mm x 3mm x 0.95 package body
K Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	QB0, nQB0	Output		Differential output pair. LVDS interface levels.
3, 4	QB1, nQB1	Output		Differential output pair. LVDS interface levels.
5	CLKB	Input	Pulldown	Non-inverting LVPECL differential clock input.
6	nCLKB	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
7	CLK_SELB	Input	Pulldown	Clock select pin for QBx outputs. When HIGH, selects QB1, nQB1 outputs. When LOW, selects QB0, nQB0 outputs. LVCMOS/LVTTL interface levels.
8	GND	Power		Power supply ground.
9	nCLKA1	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
10	CLKA1	Input	Pulldown	Non-inverting LVPECL differential clock input.
11	nCLKA0	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
12	CLKA0	Input	Pulldown	Non-inverting LVPECL differential clock input.
13	V_{DD}	Power		Positive supply pin.
14	CLK_SELA	Input	Pulldown	Clock select pin for CLKA inputs. When HIGH, selects CLKA1/nCLKA1 inputs. When LOW, selects CLKA0/nCLKA0 inputs. LVCMOS/LVTTL interface levels.
15, 16	nQA, QA	Output		Differential output pair. LVDS interface levels.

NOTE: *Pulldown and Pullup* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistors			37.5		kΩ
$R_{VDD}/2$	Pullup/Pulldown Resistors			37.5		kΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE, BANK A

Bank A	
Control Inputs	**Outputs**
CLK_SELA	**QA, nQA**
0	Selects CLKA0, nCLKA0
1	Selects CLKA1, nCLKA1

TABLE 3B. CONTROL INPUT FUNCTION TABLE, BANK B

Bank B		
Control Inputs	**Outputs**	
CLK_SELB	**QB0, nQB0**	**QB1, nQB1**
0	Follows CLKB input	Logic Low
1	Logic Low	Follows CLKB input

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	51.5°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				94	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 2.5V ± 5%, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.7	V
I_{IH}	Input High Current	CLK_SELA, CLK_SELB	V_{DD} = V_{IN} = 2.625V			150	µA
I_{IL}	Input Low Current	CLK_SELA, CLK_SELB	V_{DD} = 2.625V, V_{IN} = 0	-10			µA

Table 4C. Differential DC Characteristics, V_{DD} = 2.5V ± 5%, TA = -40°C to 85°C

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{IH}	Input High Current	CLKAx, CLKB nCLKx, nCLKB			150			150			150	µA
I_{IL}	Input Low Current	CLKAx, CLKB nCLKx, nCLKB	-150			-150			-150			µA
V_{PP}	Peak-to-Peak Input Voltage		0.15		1.2	0.15		1.2	0.15		1.2	V
V_{CMR}	Commond Mode Input Voltage; NOTE 1, 2		1.2		V_{DD}	1.2		V_{DD}	1.2		V_{DD}	V

NOTE 1: Common mode input voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLKAx, nCLKAx and CLKB, nCLKB is V_{DD} + 0.3V.

TABLE 4D. LVDS DC CHARACTERISTICS, V_{DD} = 2.5V ± 5%, TA = -40°C TO 85°C

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OD}	Differential Output Voltage	250	350	450	250	350	450	250	350	450	mV
ΔV_{OD}	V_{OD} Magnitude Change			30			30			30	mV
V_{OS}	Offset Voltage	0.93	1.18	1.43	0.97	1.22	1.47	1.02	1.27	1.52	V
ΔV_{OS}	V_{OS} Magnitude Change			10			10			10	mV

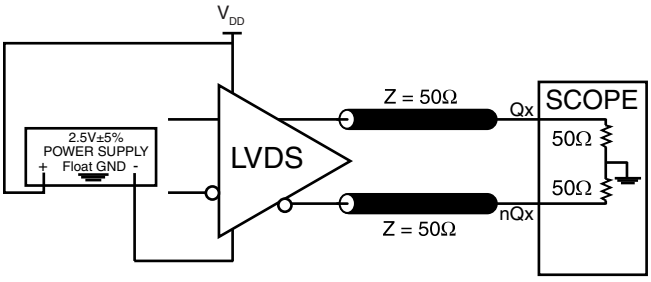
NOTE 1: Refer to Parameter Measurement Information, "2.5V Output Load Test Circuit" diagram.

TABLE 5. AC CHARACTERISTICS, V_{DD} = 2.5V ± 5%, TA = -40°C TO 85°C

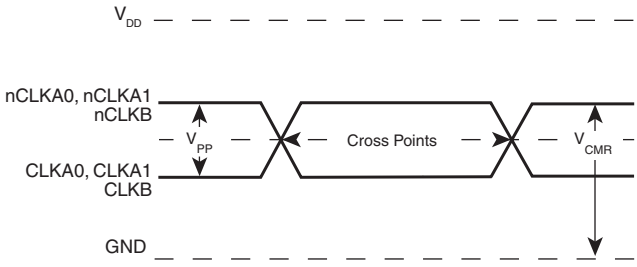
Symbol	Parameter		Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					2.5	GHz
t_{PD}	Propagation Delay; NOTE 1	QA, nQA		250		425	ps
		QBx, nQBx		200		375	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 4	QA, nQA			0.11		ps
		QBx, nQBx			0.11		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3					200	ps
$MUX_{-ISOLATION}$	MUX Isolation				55		dB
t_R/t_F	Output Rise/Fall Time		20% to 80%	100		200	ps
odc	Output Duty Cycle	QA, nQA		47		53	%
		QBx, nQBx		48		52	%

All parameters are measured ≤ 1.2GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Measured using clock input at 622MHz.

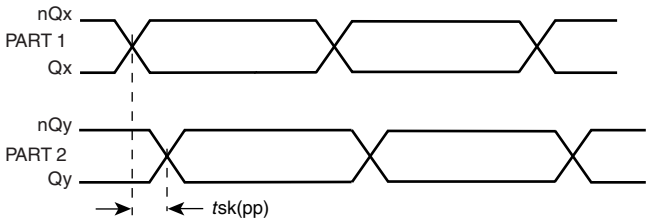
PARAMETER MEASUREMENT INFORMATION



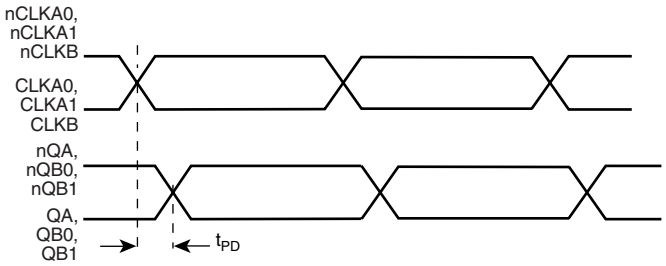
OUTPUT LOAD 2.5V AC TEST CIRCUIT



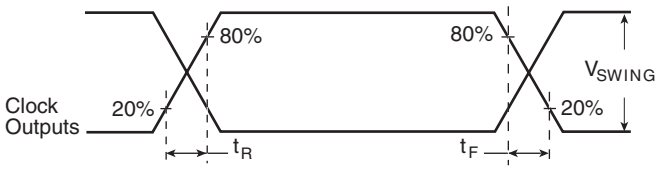
DIFFERENTIAL INPUT LEVEL



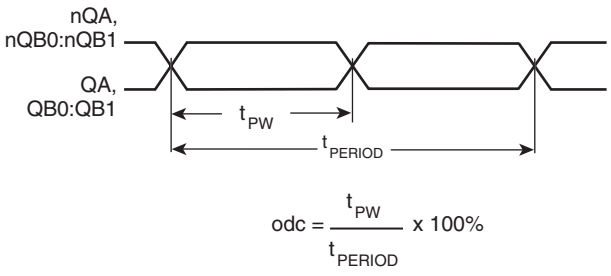
PART-TO-PART SKEW



PROPAGATION DELAY



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

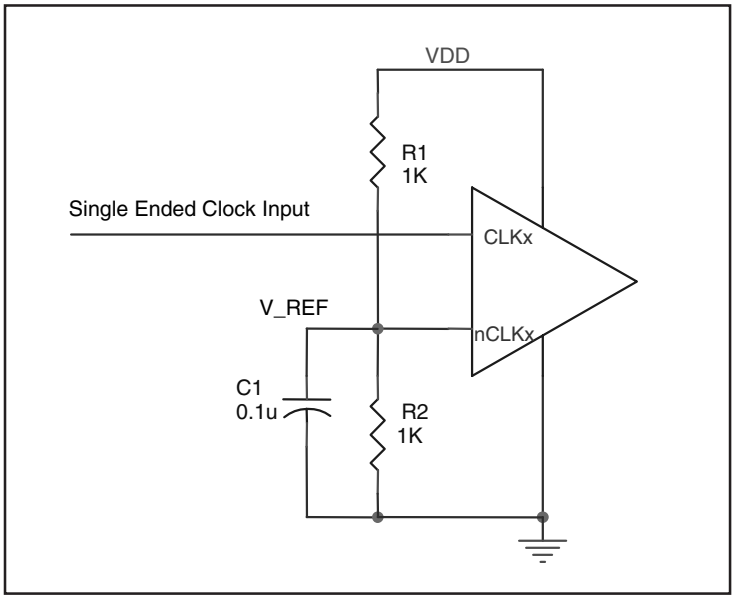


Figure 1. Single Ended Signal Driving Differential Input

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Input:
For applications not requiring the use of a differential input, both the CLK and nCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS
All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

2.5V LVDS Driver Termination

Figure 2 shows a typical termination for LVDS driver in characteristic impedance of 100Ω differential (50Ω single) transmission line environment. For buffer with multiple LVDS driver, it is recommended to terminate the unused outputs.

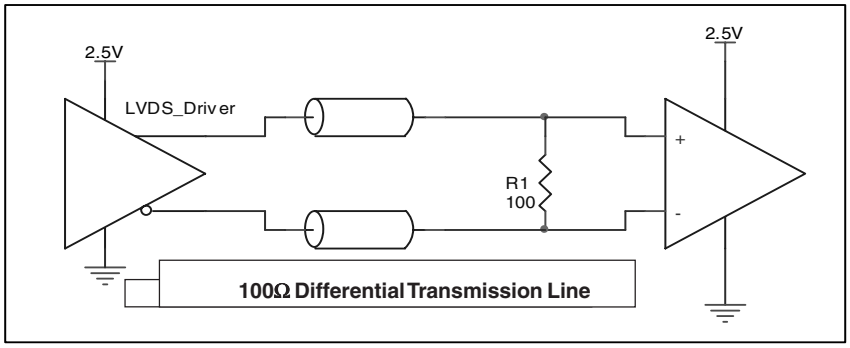


Figure 2. Typical LVDS Driver Termination

Thermal Release Path

The expose metal pad provides heat transfer from the device to the P.C. board. The expose metal pad is ground pad connected to ground plane through thermal via. The exposed pad on the device to the exposed metal pad on the PCB is contacted through solder as shown in *Figure 3.* For further information, please refer to the Application Note on Surface Mount Assembly of Amkor's Thermally /Electrically Enhance Leadframe Base Package, Amkor Technology.

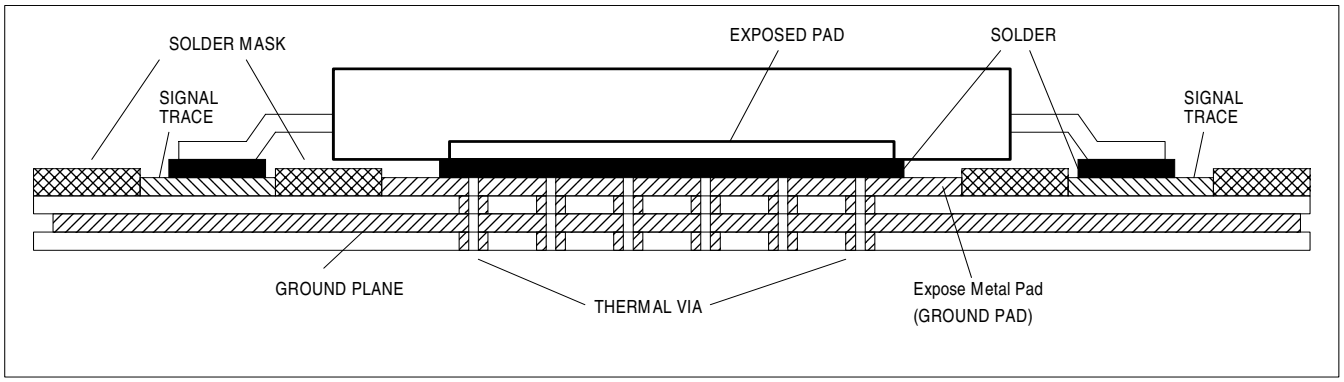
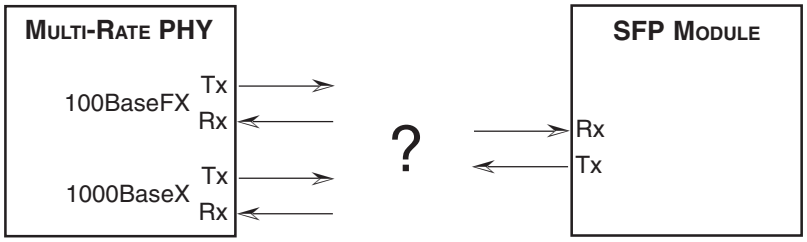


Figure 3. P.C. Board for Exposed Pad Thermal Release Path Example

A Typical Application for the ICS85454

Used to connect a multi-rate PHY with the Tx/Rx pins of an SFP Module.

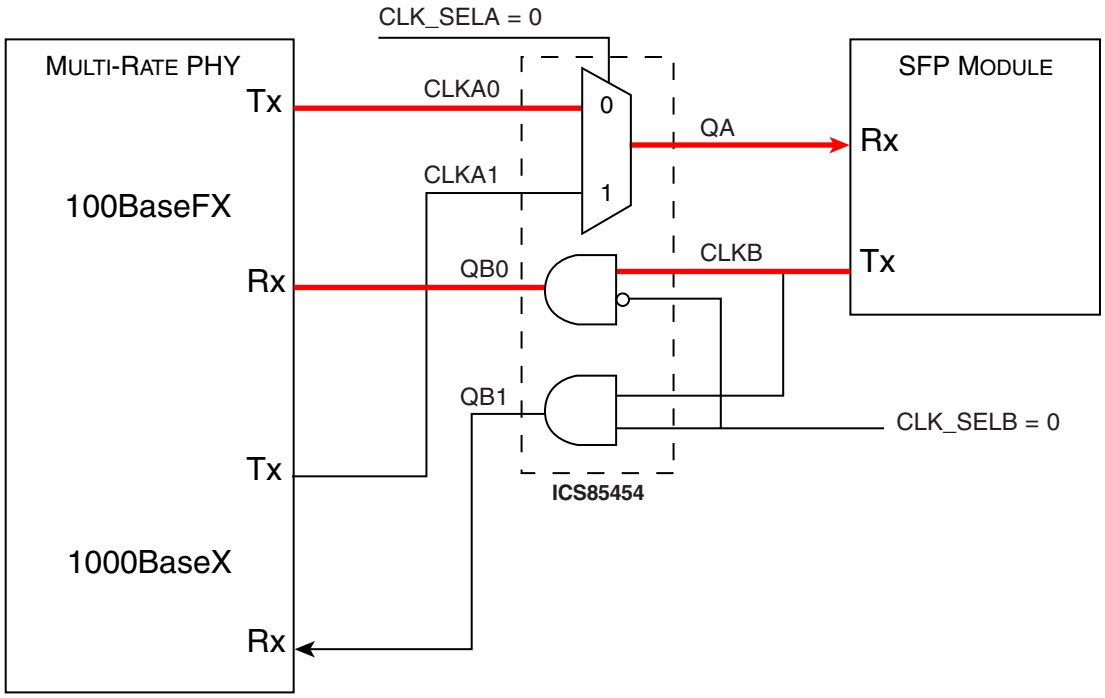
Problem Addressed: How to map the 2 Tx/Rx pairs of the multi-rate PHY to the single Tx/Rx pair on the SFP Module.



Mode 1, 100BaseX Connected to SFP

All lines are differential pairs, but drawn as single-ended to simplify the drawing.

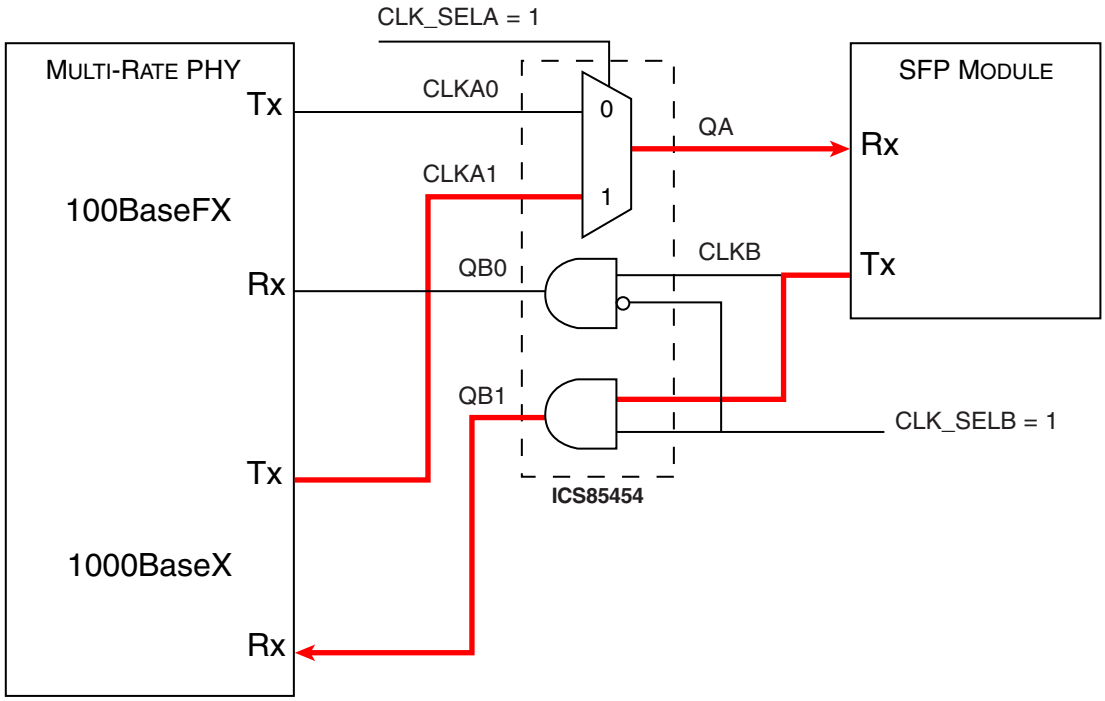
Bold red lines ——— are active connections highlighting the signal path.



MODE 2, 100BASEX CONNECTED TO SFP

All lines are differential pairs, but drawn as single-ended to simplify the drawing.

Bold red lines ——— are active connections highlighting the signal path.



POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS85454.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS85454 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 2.5V + 5% = 2.625V, which gives worst case results.

- Power_$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 2.625V * 94mA = **247mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 51.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.247W * 51.5°C/W = 97.7°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 16-PIN VFQFN, FORCED CONVECTION

θ_{JA} vs. 0 Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 16 Lead VFQFN

θ_{JA} at 0 Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

Transistor Count

The transistor count for ICS85454 is: 189

Package Outline - K Suffix for 16 Lead VFQFN

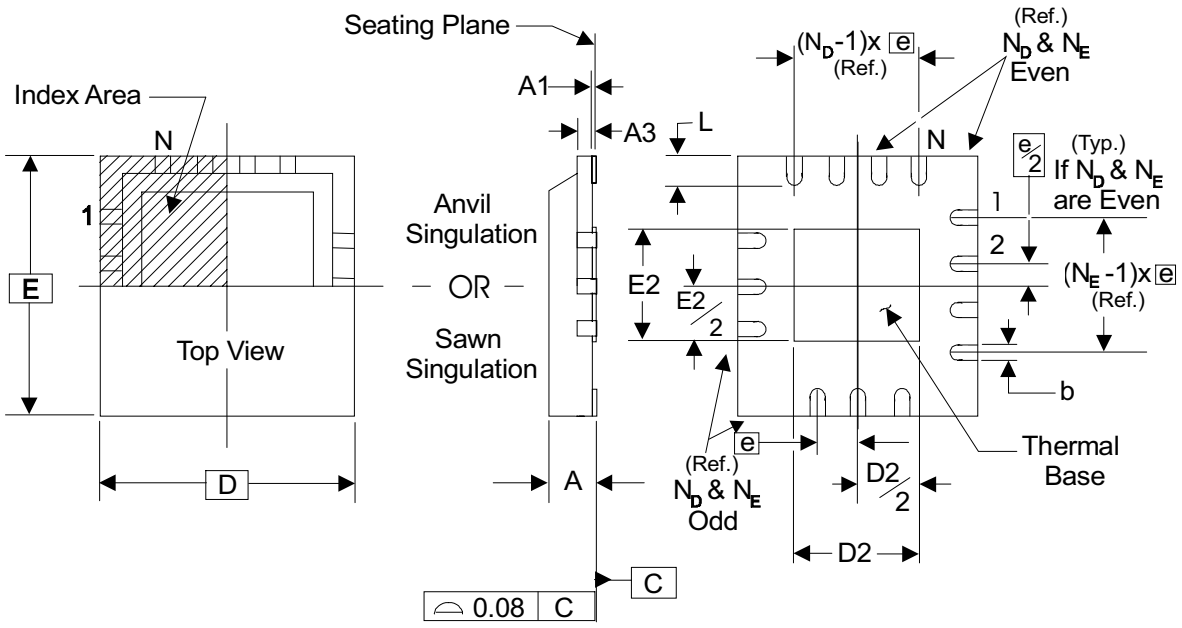


Table 8. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	16	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	4	
N_E	4	
D	3.0	
D2	1.0	1.8
E	3.0	
E2	1.0	1.8
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
85454AK	454A	16 Lead VFQFN	Tube	-40°C to 85°C
85454AKT	454A	16 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C
85454AKLF	44AL	16 Lead "Lead-Free" VFQFN	Tube	-40°C to 85°C
85454AKLFT	44AL	16 Lead "Lead-Free" VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A		13	Ordering Information Table - corrected lead-free marking.	7/20/06
B	T4D	4 7	LVDS DC Characteristics table - corrected V_{OD}, ΔV_{OD}, and ΔV_{OS}. Added *Thermal Release Path.*	12/21/06

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