PRERELEASE
Electrical Specifications Subject to Change

LTC6994-1/LTC6994-2

TimerBlox: Delay Block/ Debouncer

FEATURES

- **Delay Range: 1µs to 33.6 Seconds**
- Configured with 1 to 3 Resistors
- Delay Max Error:
  - <2.3% for Delay > 512µs
  - <3.4% for Delay of 8µs to 512µs
  - <5.1% for Delay of 1µs to 8µs
- Delay One or Both Rising/Falling Edges
- 2.25V to 5.5V Single Supply Operation
- 70µA Supply Current at 10µs Delay
- 500µs Start-Up Time
- CMOS Output Driver Sources/Sinks 20mA
- –40°C to 125°C Operating Temperature Range
- Available in Low Profile (1mm) SOT-23 (ThinSOT™) and 2mm × 3mm DFN

APPLICATIONS

- Noise Discriminators/Pulse Qualifiers
- Delay Matching
- Switch Debouncing
- High Vibration, High Acceleration Environments
- Portable and Battery-Powered Equipment

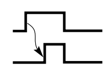
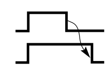
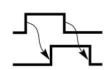
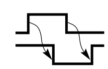
DESCRIPTION

The LTC®6994 is a programmable delay block with a range of 1µs to 33.6 seconds. The LTC6994 is part of the TimerBlox™ family of versatile silicon timing devices.

A single resistor, R_{SET}, programs the LTC6994's internal master oscillator frequency. The input-to-output delay is determined by this master oscillator and an internal clock divider, N_{DIV}, programmable to eight settings from 1 to 2^{21}:

$$t_{DELAY} = \frac{N_{DIV} \bullet R_{SET}}{50k\Omega} \bullet 1\mu s,\ N_{DIV} = 1, 8, 64, ..., 2^{21}$$

The output (OUT) follows the input (IN) after delaying the rising and/or falling transitions. The LTC6994-1 will delay the rising or falling edge. The LTC6994-2 will delay both transitions, and adds the option to invert the output.

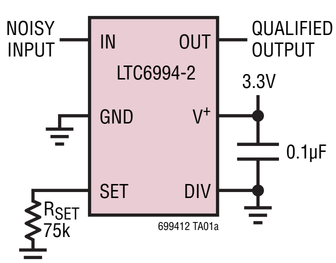
DEVICE	DELAY FUNCTION		
LTC6994-1		or	
LTC6994-2		or	

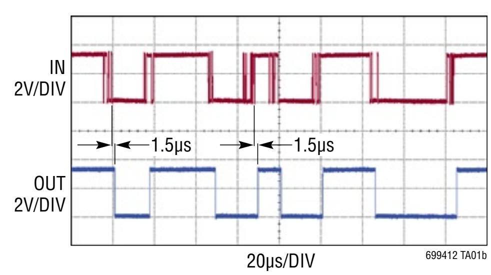
The LTC6994 also offers the ability to dynamically adjust the width of the output pulse via a separate control voltage.

The LTC6994 is available in the 6-lead SOT-23 (ThinSOT) and 6-lead 2mm × 3mm DFN packages.

TYPICAL APPLICATION

Noise Discriminator

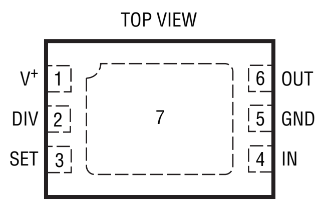




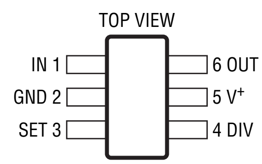
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V^+) to GND 6V
Maximum Voltage
on Any Pin ....(GND – 0.3V) ≤ V_{PIN} ≤ (V^+ + 0.3V)
Operating Temperature Range (Note 2)
LTC6994C ....–40°C to 85°C
LTC6994I ....–40°C to 85°C
LTC6994H.. –40°C to 125°C
Specified Temperature Range (Note 3)
LTC6994C .... 0°C to 70°C
LTC6994I ....–40°C to 85°C
LTC6994H....................................... –40°C to 125°C
Junction Temperature .... 150°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
S6 Package ....300°C

PIN CONFIGURATION



DCB PACKAGE
6-LEAD (2mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 64°C/W, θ_{JC} = 10.6°C/W
EXPOSED PAD (PIN 7) CONNECTED TO GND,
PCB CONNECTION OPTIONAL



S6 PACKAGE
6-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 230°C/W, θ_{JC} = 51°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6994CDCB-1#PBF	LTC6994CDCB-1#TRPBF	LFCT	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC6994IDCB-1#PBF	LTC6994IDCB-1#TRPBF	LFCT	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6994HDCB-1#PBF	LTC6994HDCB-1#TRPBF	LFCT	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6994CDCB-2#PBF	LTC6994CDCB-2#TRPBF	LFCW	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC6994IDCB-2#PBF	LTC6994IDCB-2#TRPBF	LFCW	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6994HDCB-2#PBF	LTC6994HDCB-2#TRPBF	LFCW	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6994CS6-1#PBF	LTC6994CS6-1#TRPBF	LTFCV	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6994IS6-1#PBF	LTC6994IS6-1#TRPBF	LTFCV	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6994HS6-1#PBF	LTC6994HS6-1#TRPBF	LTFCV	6-Lead Plastic TSOT-23	–40°C to 125°C
LTC6994CS6-2#PBF	LTC6994CS6-2#TRPBF	LTFCX	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6994IS6-2#PBF	LTC6994IS6-2#TRPBF	LTFCX	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6994HS6-2#PBF	LTC6994HS6-2#TRPBF	LTFCX	6-Lead Plastic TSOT-23	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 2.25V to 5.5V, IN = 0V, DIVCODE = 0 to 15 (N_{DIV} = 1 to 2^{21}), R_{SET} = 50k to 800k, R_{LOAD} = 5k, C_{LOAD} = 5pF unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
t_{DELAY}	Delay Time				1µ		33.55	sec
Δt_{DELAY}	Delay Accuracy (Note 4)	N_{DIV} ≥ 512		 ●		±1.7	±2.3 ±3.0	% %
		8 ≤ N_{DIV} ≤ 64		 ●		±2.4	±3.4 ±4.4	% %
		N_{DIV} = 1 Rising Edge Delay		 ●		±3.8	±5.1 ±6.2	% %
$\Delta t_{DELAY}/\Delta T$	Delay Drift Over Temperature	N_{DIV} ≥ 512 N_{DIV} ≤ 64		● ●		±0.006 ±0.008		%/°C %/°C
	Delay Change With Supply	N_{DIV} ≥ 512	V^+ = 4.5V to 5.5V V^+ = 2.25V to 4.5V	● ●	–0.6 –0.4	–0.2 –0.1		% %
		8 ≤ N_{DIV} ≤ 64	V^+ = 4.5V to 5.5V V^+ = 2.7V to 4.5V V^+ = 2.25V to 2.7V	● ● ●	–0.9 –0.7 –1.1	–0.2 –0.2 –0.1	 0.4 0.9	% % %
	Delay Jitter (Note 10)	N_{DIV} = 1	V^+ = 5.5V V^+ = 2.25V			1.0 0.5		$\%_{P-P}$ $\%_{P-P}$
		N_{DIV} = 8				0.20		$\%_{P-P}$
		N_{DIV} = 64				0.05		$\%_{P-P}$
		N_{DIV} = 512				0.20		$\%_{P-P}$
		N_{DIV} = 4096				0.03		$\%_{P-P}$
t_S	Delay Change Settling Time (Note 9)	$t_{MASTER} = t_{DELAY}/N_{DIV}$				6 • t_{MASTER}		µs
Power Supply								
V^+	Operating Supply Voltage Range			●	2.25		5.5	V
	Power-On Reset Voltage			●			1.95	V
$I_{S(IDLE)}$	Supply Current (Idle)	R_L = ∞, R_{SET} = 50k, N_{DIV} ≤ 64	V^+ = 5.5V V^+ = 2.25V	● ●		165 125	200 160	µA µA
		R_L = ∞, R_{SET} = 50k, N_{DIV} ≥ 512	V^+ = 5.5V V^+ = 2.25V	● ●		135 105	175 140	µA µA
		R_L = ∞, R_{SET} = 800k, N_{DIV} ≤ 64	V^+ = 5.5V V^+ = 2.25V	● ●		70 60	110 95	µA µA
		R_L = ∞, R_{SET} = 800k, N_{DIV} ≥ 512	V^+ = 5.5V V^+ = 2.25V	● ●		65 55	100 90	µA µA
Analog Inputs								
V_{SET}	Voltage at SET Pin			●	0.97	1.00	1.03	V
$\Delta V_{SET}/\Delta T$	V_{SET} Drift Over Temperature			●		±75		µV/°C
R_{SET}	Frequency-Setting Resistor			●	50		800	kΩ
V_{DIV}	DIV Pin Voltage			●	0		V^+	V
$\Delta V_{DIV}/\Delta V^+$	DIV Pin Valid Code Range (Note 5)	Deviation from Ideal V_{DIV}/V^+ = (DIVCODE + 0.5)/16		●			±1.5	%
	DIV Pin Input Current			●			±10	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 2.25V to 5.5V, IN = 0V, DIVCODE = 0 to 15 (N_{DIV} = 1 to 2^{21}), R_{SET} = 50k to 800k, R_{LOAD} = ∞, C_{LOAD} = 5pF unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Digital I/O								
	IN Pin Input Capacitance					2.5		pF
	IN Pin Input Current	IN = 0V to V^+					±10	nA
V_{IH}	High Level IN Pin Input Voltage	(Note 6)		●	0.7 • V^+			V
V_{IL}	Low Level IN Pin Input Voltage	(Note 6)		●			0.3 • V^+	V
$I_{OUT(MAX)}$	Output Current	V^+ = 2.7V to 5.5V				±20		mA
V_{OH}	High Level Output Voltage (Note 7)	V^+ = 5.5V	I_{OUT} = –1mA I_{OUT} = –16mA	● ●	5.45 4.84	5.48 5.15		V V
		V^+ = 3.3V	I_{OUT} = –1mA I_{OUT} = –10mA	● ●	3.24 2.75	3.27 2.99		V V
		V^+ = 2.25V	I_{OUT} = –1mA I_{OUT} = –8mA	● ●	2.17 1.58	2.21 1.88		V V
V_{OL}	Low Level Output Voltage (Note 7)	V^+ = 5.5V	I_{OUT} = 1mA I_{OUT} = 16mA	● ●		0.02 0.26	0.04 0.54	V V
		V^+ = 3.3V	I_{OUT} = 1mA I_{OUT} = 10mA	● ●		0.03 0.22	0.05 0.46	V V
		V^+ = 2.25V	I_{OUT} = 1mA I_{OUT} = 8mA	● ●		0.03 0.26	0.07 0.54	V V
t_{PD}	Propagation Delay	V^+ = 5.5V V^+ = 3.3V V^+ = 2.25V				10 14 24		ns ns ns
t_{WIDTH}	Minimum Recognized Input Pulse Width	V^+ = 3.3V				5		ns
t_r	Output Rise Time (Note 8)	V^+ = 5.5V V^+ = 3.3V V^+ = 2.25V				1.1 1.7 2.7		ns ns ns
t_f	Output Fall Time (Note 8)	V^+ = 5.5V V^+ = 3.3V V^+ = 2.25V				1.0 1.6 2.4		ns ns ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC6994C is guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 3: The LTC6994C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6994C is designed, characterized and expected to meet specified performance from –40°C to 85°C but it is not tested or QA sampled at these temperatures. The LTC6994I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6994H is guaranteed to meet specified performance from –40°C to 125°C.

Note 4: Frequency accuracy is defined as the deviation from the f_{OUT} equation, assuming R_{SET} is used to program the frequency.

Note 5: See Operation section, Table 1 and Figure 2 for a full explanation of how the DIV pin voltage selects the value of DIVCODE.

Note 6: The IN pin has hysteresis to accommodate slow rising or falling signals. The threshold voltages are proportional to V^+. Typical values can be estimated at any supply voltage using:

$$V_{IN(RISING)} \approx 0.55 \cdot V^+ + 185mV \text{ and } V_{IN(FALLING)} \approx 0.48 \cdot V^+ - 155mV$$

Note 7: To conform to the Logic IC Standard, current out of a pin is arbitrarily given a negative value.

Note 8: Output rise and fall times are measured between the 10% and the 90% power supply levels with 5pF output load. These specifications are based on characterization.

Note 9: Settling time is the amount of time required for the output to settle within ±1% of the final delay after a 0.5× or 2× change in I_{SET}.

Note 10: Jitter is the ratio of the deviation of the programmed delay to the mean of the delay. This specification is based on characterization and is not 100% tested.

TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = 3.3V$, $R_{SET} = 200k$ and $T_A = 25°C$ unless otherwise noted.

Delay Error vs Temperature ($N_{DIV} = 1$)

Delay Error vs Temperature ($N_{DIV} = 1$)

Delay Error vs Temperature ($N_{DIV} = 1$)

Delay Error vs Temperature ($8 \le N_{DIV} \le 64$)

Delay Error vs Temperature ($8 \le N_{DIV} \le 64$)

Delay Error vs Temperature ($8 \le N_{DIV} \le 64$)

Delay Error vs Temperature ($N_{DIV} \ge 512$)

Delay Error vs Temperature ($N_{DIV} \ge 512$)

Delay Error vs Temperature ($N_{DIV} \ge 512$)

TYPICAL PERFORMANCE CHARACTERISTICS

V^+ = 3.3V, R_{SET} = 200k and T_A = 25°C unless otherwise noted.

Delay Error vs DIVCODE

Delay Error vs DIVCODE

Delay Error vs DIVCODE

Delay Error vs R_{SET} (N_{DIV} =1)

Delay Error vs R_{SET} ($8 \le N_{DIV} \le 64$)

Delay Error vs R_{SET} ($N_{DIV} \ge 512$)

Delay Drift vs Supply Voltage (N_{DIV} =1)

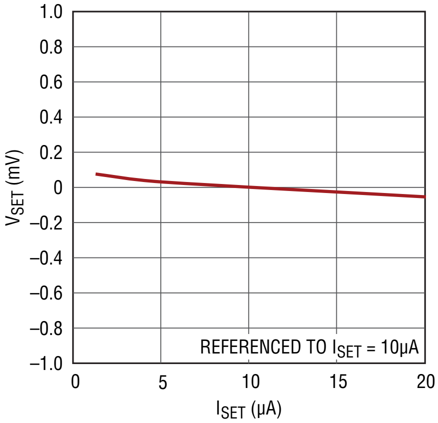
Delay Drift vs Supply Voltage ($8 \le N_{DIV} \le 64$)

Delay Drift vs Supply Voltage ($N_{DIV} \ge 512$)

TYPICAL PERFORMANCE CHARACTERISTICS

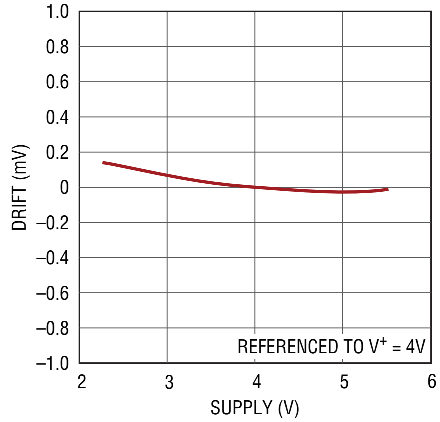
$V^+ = 3.3V$, $R_{SET} = 200k$ and $T_A = 25°C$ unless otherwise noted.

V_{SET} Drift vs I_{SET}



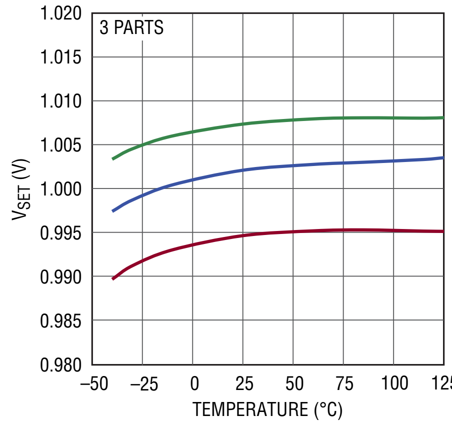
699412 G19

V_{SET} Drift vs Supply



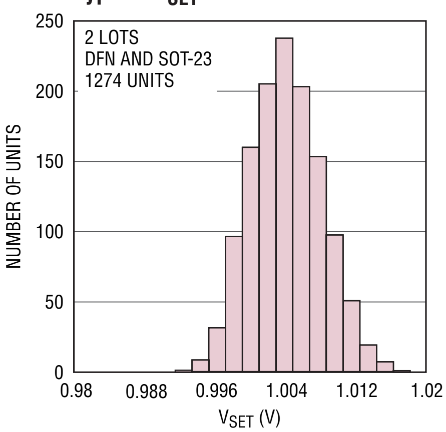
699412 G20

V_{SET} vs Temperature



699412 G21

Typical V_{SET} Distribution



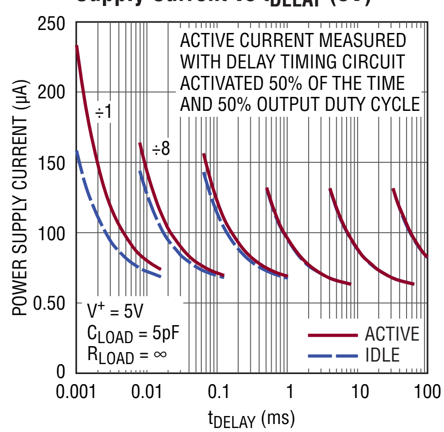
699412 G22

Supply Current vs Supply Voltage

Supply Current vs Temperature

Supply Current vs IN Pin Voltage

Supply Current vs t_{DELAY} (5V)



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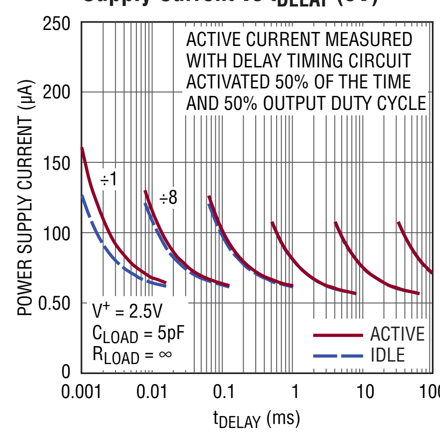
Supply Current vs t_{DELAY} (3V)

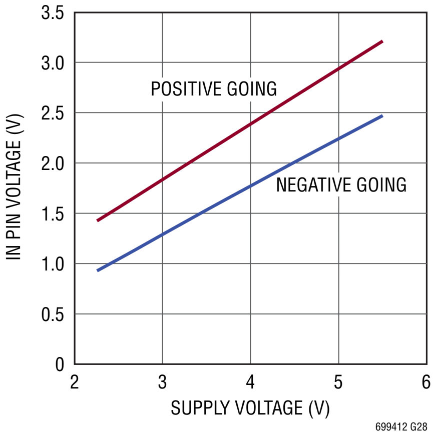


699412 G27

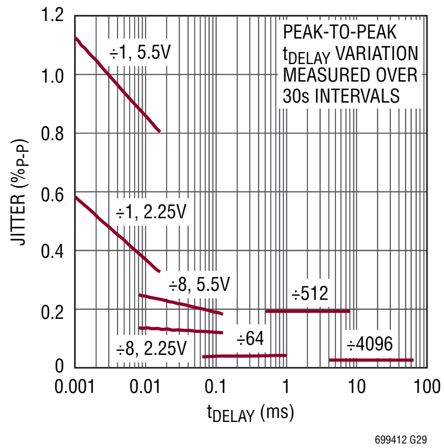
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = 3.3V$, $R_{SET} = 200k$ and $T_A = 25°C$ unless otherwise noted.

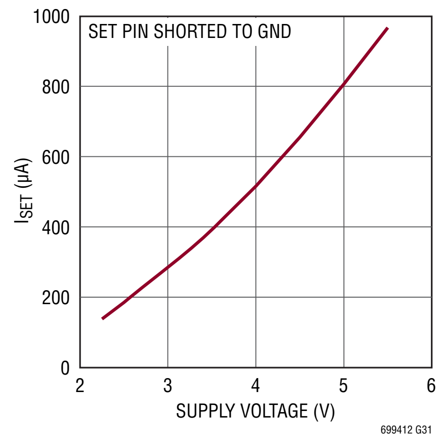
IN Threshold Voltage vs Supply Voltage



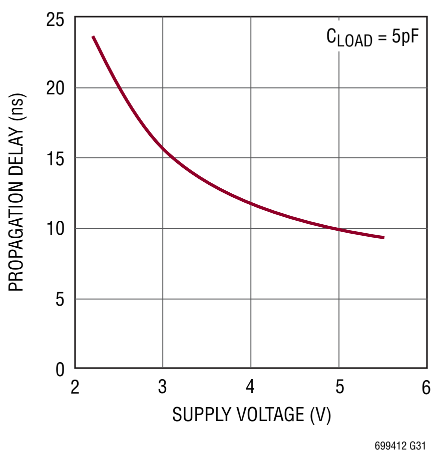
Peak-to-Peak Jitter vs t_{DELAY}



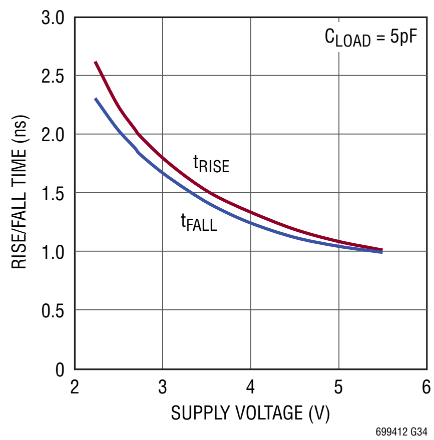
Typical I_{SET} Current Limit vs V^+



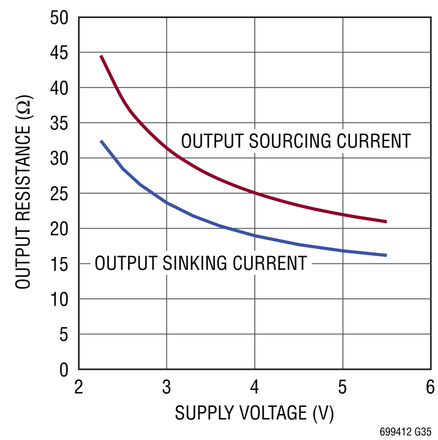
Input Propagation Delay (t_{PD}) vs Supply Voltage



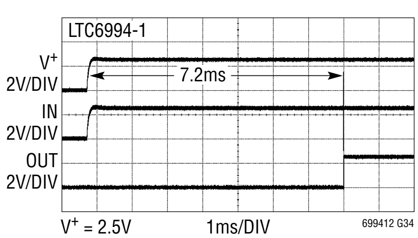
Rise and Fall Time vs Supply Voltage



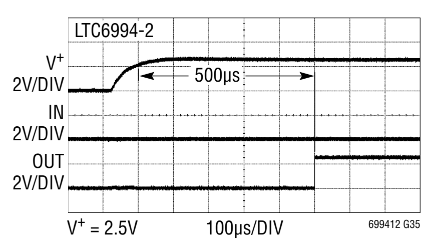
Output Resistance vs Supply Voltage



Start-Up, $R_{SET} = 800k$ (LTC6994-1)



Start-Up, $R_{SET} = 50k$ (LTC6994-2, POL = 1)



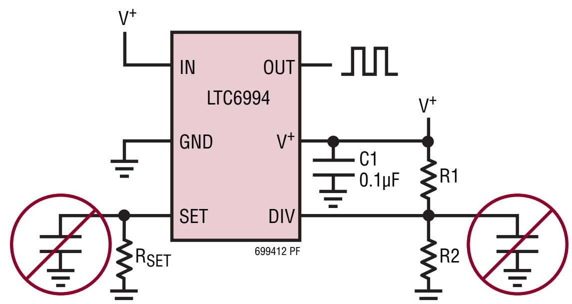
PIN FUNCTIONS (DCB/S6)

V^+ (Pin 1/Pin 5): Supply Voltage (2.25V to 5.5V). This supply should be kept free from noise and ripple. It should be bypassed directly to the GND pin with a 0.1µF capacitor.

DIV (Pin 2/Pin 4): Programmable Divider and Polarity Input. The DIV pin voltage (V_{DIV}) is internally converted into a 4-bit result (DIVCODE). V_{DIV} may be generated by a resistor divider between V^+ and GND. Use 1% resistors to ensure an accurate result. The DIV pin and resistors should be shielded from the OUT pin or any other traces that have fast edges. Limit the capacitance on the DIV pin to less than 100pF so that V_{DIV} settles quickly. The MSB of DIVCODE (POL) selects the delay functionality. For the LTC6994-1, POL = 0 will delay the rising transition and POL = 1 will delay the falling transition. For the LTC6994-2, both transitions are delayed so POL = 1 can be used to invert the output.

SET (Pin 3/Pin 3): Delay Setting Input. The voltage on the SET pin (V_{SET}) is regulated to 1V above GND. The amount of current sourced from the SET pin (I_{SET}) programs the master oscillator frequency. The I_{SET} current range is 1.25µA to 20µA. The delayed output transition will be not occur if I_{SET} drops below approximately 500nA. Once I_{SET} increases above 500nA the delayed edge will transition. A resistor connected between SET and GND is the most accurate way to set the delay. For best performance, use a precision metal or thin film resistor of 0.5% or better tolerance and 50ppm/°C or better temperature coefficient. For lower accuracy applications an inexpensive 1% thick film resistor may be used.

Limit the capacitance on the SET pin to less than 10pF to minimize jitter and ensure stability. Capacitance less than 100pF maintains the stability of the feedback circuit regulating the V_{SET} voltage.

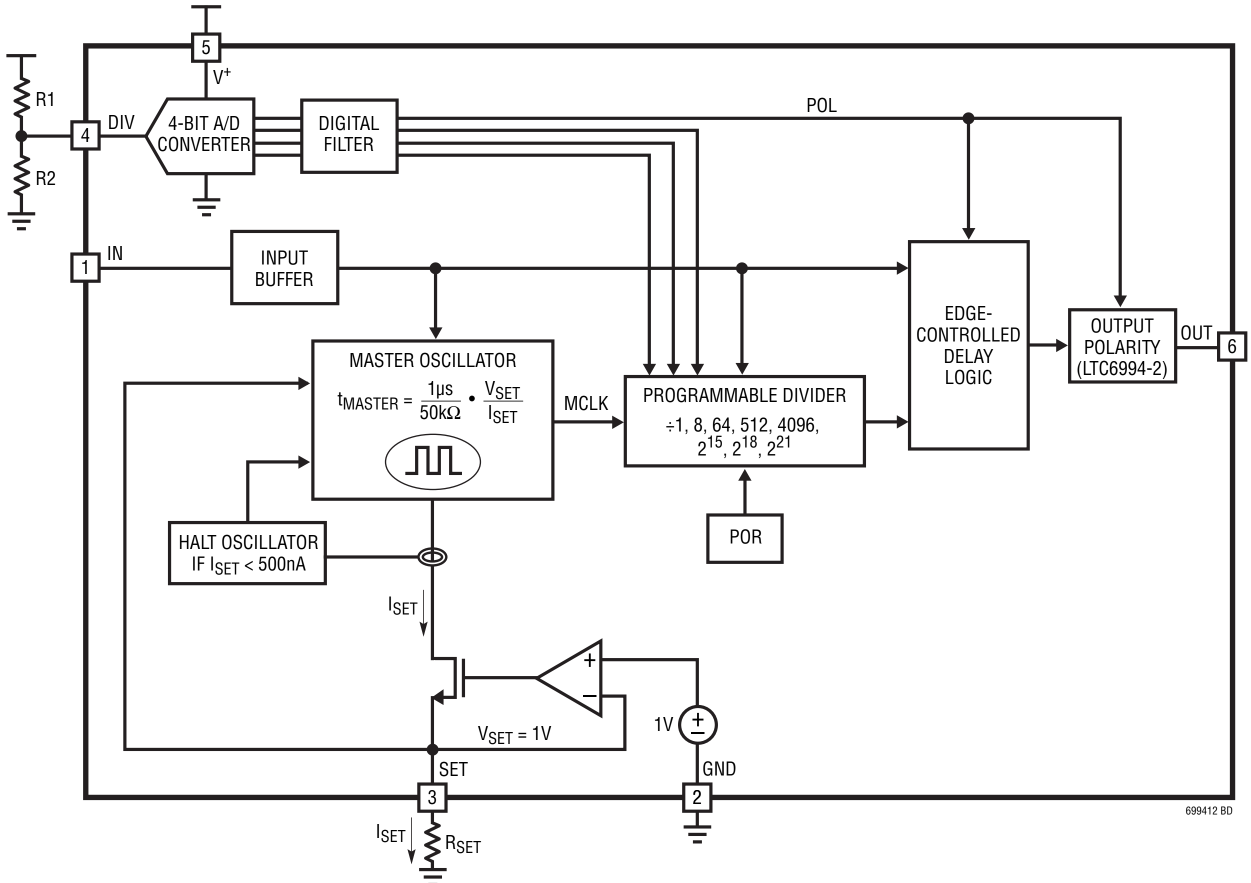


IN (Pin 4/Pin 1): Logic Input. Depending on the version and POL bit setting, rising or falling edges on IN will propagate to OUT after a programmable delay. The LTC6994-1 will delay only the rising or falling edge. The LTC6994-2 will delay both edges.

GND (Pin 5/Pin 2): Ground. Tie to a low inductance ground plane for best performance.

OUT (Pin 6/Pin 6): Output. The OUT pin swings from GND to V^+ with an output resistance of approximately 30Ω. When driving an LED or other low impedance load a series output resistor should be used to limit source/sink current to 20mA.

BLOCK DIAGRAM (S6 package pin numbers shown)



OPERATION

The LTC6994 is built around a master oscillator with a 1µs minimum period. The oscillator is controlled by the SET pin current (I_{SET}) and voltage (V_{SET}), with a 1µs/50kΩ conversion factor that is accurate to ±1.7% under typical conditions.

$$t_{MASTER} = \frac{1\mu s}{50k\Omega} \bullet \frac{V_{SET}}{I_{SET}}$$

A feedback loop maintains V_{SET} at 1V ±30mV, leaving I_{SET} as the primary means of controlling the input-to-output delay. The simplest way to generate I_{SET} is to connect a resistor (R_{SET}) between SET and GND, such that I_{SET} = V_{SET}/R_{SET}. The master oscillator equation reduces to:

$$t_{MASTER} = 1\mu s \bullet \frac{R_{SET}}{50k\Omega}$$

From this equation, it is clear that V_{SET} drift will not affect the input-to-output delay when using a single program resistor (R_{SET}). Error sources are limited to R_{SET} tolerance and the inherent accuracy Δt_{DELAY} of the LTC6994.

R_{SET} may range from 50k to 800k (equivalent to I_{SET} between 1.25µA and 20µA).

When the input makes a transition that will be delayed (as determined by the part version and POL bit setting), the master oscillator is enabled to time the delay. When the desired duration is reached, the output is allowed to transition.

The LTC6994 also includes a programmable frequency divider which can further divide the frequency by 1, 8, 64, 512, 4096, 2^{15}, 2^{18} or 2^{21}. This extends the delay duration by those same factors. The divider ratio N_{DIV} is set by a resistor divider attached to the DIV pin.

$$t_{DELAY} = \frac{N_{DIV}}{50k\Omega} \bullet \frac{V_{SET}}{I_{SET}} \bullet 1\mu s$$

With R_{SET} in place of V_{SET}/I_{SET} the equation reduces to:

$$t_{DELAY} = \frac{N_{DIV} \bullet R_{SET}}{50k\Omega} \bullet 1\mu s$$

DIVCODE

The DIV pin connects to an internal, V^+ referenced 4-bit A/D converter that determines the DIVCODE value. DIVCODE programs two settings on the LTC6994:

1. DIVCODE determines the output frequency divider setting, N_{DIV}.
2. The DIVCODE MSB is the POL bit, and configures a different polarity setting on the two versions.
   a. LTC6994-1: POL selects rising or falling-edge delays. POL = 0 will delay rising-edge transitions. POL = 1 will delay falling-edge transitions.
   b. LTC6994-2: POL selects the output inversion. POL = 1 inverts the output signal.

V_{DIV} may be generated by a resistor divider between V+ and GND as shown in Figure 1.

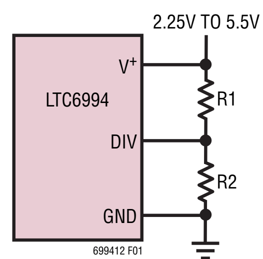


Figure 1. Simple Technique for Setting DIVCODE

Table 1 offers recommended 1% resistor values that accurately produce the correct voltage division as well as the corresponding N_{DIV} and POL values for the recommended resistor pairs. Other values may be used as long as:

1. The V_{DIV}/V^+ ratio is accurate to ±1.5% (including resistor tolerances and temperature effects)
2. The driving impedance (R1||R2) does not exceed 500kΩ.

OPERATION

If the voltage is generated by other means (i.e., the output of a DAC) it must track the V^+ supply voltage. The last column in Table 1 shows the ideal ratio of V_{DIV} to the supply voltage, which can also be calculated as:

$$\frac{V_{DIV}}{V^+} = \frac{DIVCODE + 0.5}{16} \pm 1.5\%$$

For example, if the supply is 3.3V and the desired DIVCODE is 4, V_{DIV} = 0.281 • 3.3V = 928mV ± 50mV.

Figure 2 illustrates the information in Table 1, showing that N_{DIV} is symmetric around the DIVCODE midpoint.

Table 1. DIVCODE Programming

DIVCODE	POL	N_{DIV}	Recommended t_{DELAY}	R1 (k)	R2 (k)	V_{DIV}/V^+
0	0	1	1µs to 16µs	Open	Short	≤ 0.03125 ±0.015
1	0	8	8µs to 128µs	976	102	0.09375 ±0.015
2	0	64	64µs to 1.024ms	976	182	0.15625 ±0.015
3	0	512	512µs to 8.192ms	1000	280	0.21875 ±0.015
4	0	4,096	4.096ms to 65.54ms	1000	392	0.28125 ±0.015
5	0	32,768	32.77ms to 524.3ms	1000	523	0.34375 ±0.015
6	0	262,144	262.1ms to 4.194ms	1000	681	0.40625 ±0.015
7	0	2,097,152	2.097sec to 33.55sec	1000	887	0.46875 ±0.015
8	1	2,097,152	2.097sec to 33.55sec	887	1000	0.53125 ±0.015
9	1	262,144	262.1ms to 4.194ms	681	1000	0.59375 ±0.015
10	1	32,768	32.77ms to 524.3ms	523	1000	0.65625 ±0.015
11	1	4,096	4.096ms to 65.54ms	392	1000	0.71875 ±0.015
12	1	512	512µs to 8.192ms	280	1000	0.78125 ±0.015
13	1	64	64µs to 1.024ms	182	976	0.84375 ±0.015
14	1	8	8µs to 128µs	102	976	0.90625 ±0.015
15	1	1	1µs to 16µs	Short	Open	≥ 0.96875 ±0.015

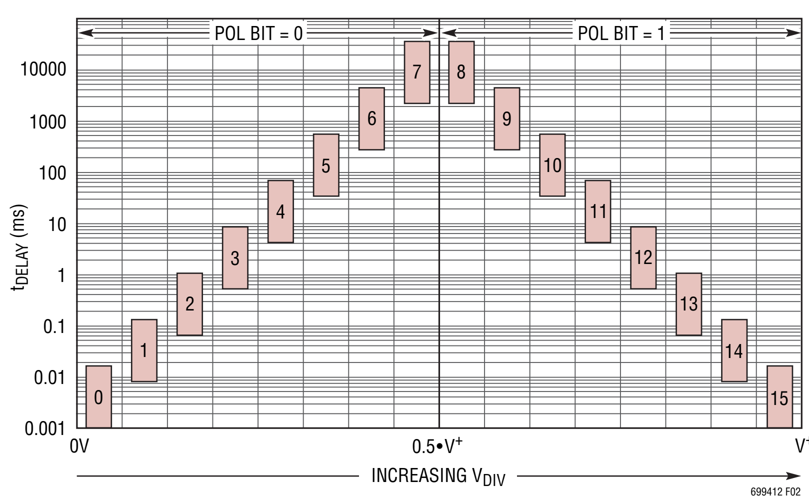


Figure 2. Pulse Width Range and POL Bit vs DIVCODE

OPERATION

Edge-Controlled Delay

The LTC6994 is a programmable delay or pulse qualifier. It can perform noise filtering, which distinguishes it from a delay line (which simply delays all input transitions).

When the voltage on the LTC6994 input pin (IN) transitions low or high, the LTC6994 can delay the corresponding output transition by any time from 1µs to 33.6 seconds.

LTC6994-1 Functionality

Figures 3 details the basic operation of the LTC6994-1 when configured to delay rising edge transitions (POL = 0). A rising edge on the IN pin initiates the timing. OUT remains low for the duration of t_{DELAY}. If IN stays high then OUT will transition high after this time. If the input doesn't remain high long enough for OUT to transition high then the timing will restart on each successive rising edge. In this way, the LTC6994-1 can serve as a pulse qualifier, filtering out noisy or short signals.

On a falling edge at the input, the output will follow immediately (after a short propagation delay t_{PD}).

Finally, note that the output pulse width may be extremely short if IN falls immediately after OUT rises.

Figure 4 details the operation of the LTC6994-1 when configured to delay falling edges (POL = 1).

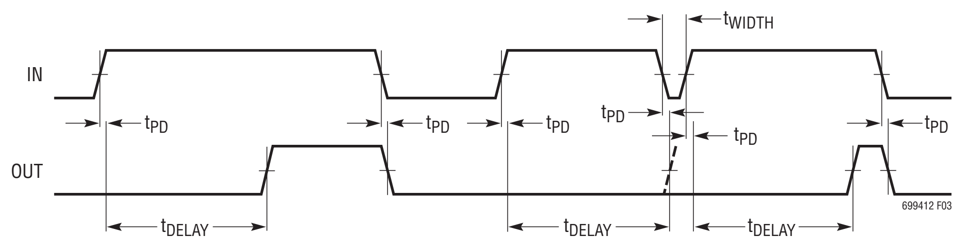


Figure 3. Rising-Edge Delayed Timing Diagram (LTC6994-1, POL = 0)

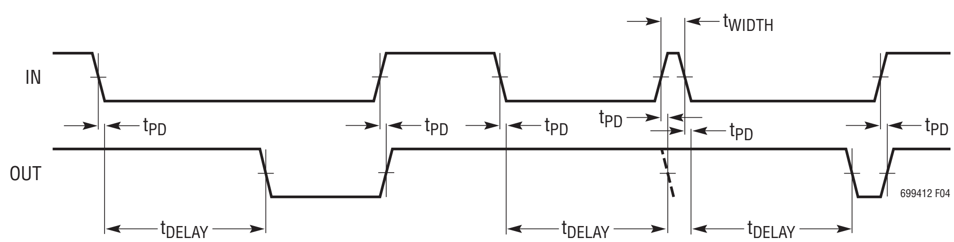


Figure 4. Falling-Edge Delayed Timing Diagram (LTC6994-1, POL = 1)

OPERATION

LTC6994-2 Functionality

Figures 5 details the basic operation of the LTC6994-2 when configured for noninverting operation (POL = 0). As before, a rising edge on the IN pin initiates the timing and, if IN remains high, OUT will transition high after t_{DELAY}.

Unlike the LTC6994-1, falling edges are delayed in the same way. When IN transitions low, OUT will follow after t_{DELAY}.

If the input doesn't remain high or low long enough for OUT to follow, the timing will restart on the next transition.

Also unlike the LTC6994-1, the output pulse width can never be less than t_{DELAY}. Therefore, the LTC6994-2 can generate pulses with a defined minimum width.

Figure 6 details the operation of the LTC6994-2 when the output is inverted (POL = 1).

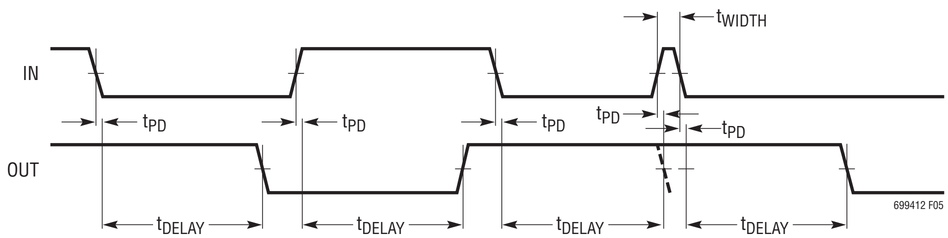


Figure 5. Both Edges Delayed Timing Diagram (LTC6994-2, POL = 0)

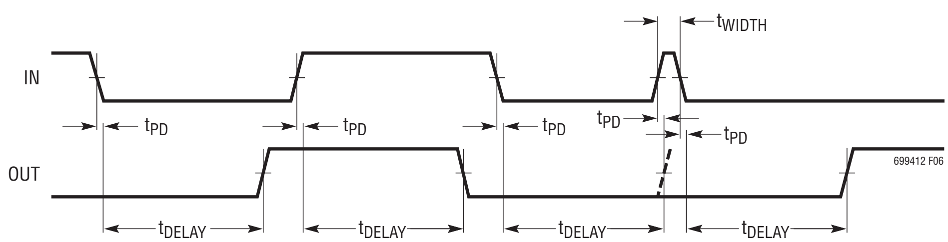


Figure 6. Both Edges Delayed (Inverting) Timing Diagram (LTC6994-2, POL = 1)

OPERATION

Changing DIVCODE After Start-Up

Following start-up, the A/D converter will continue monitoring V_{DIV} for changes. Changes to DIVCODE will be recognized slowly, as the LTC6994 places a priority on eliminating any "wandering" in the DIVCODE. The typical delay depends on the difference between the old and new DIVCODE settings and is proportional to the master oscillator period.

$$t_{DIVCODE} = 16 \bullet (\Delta DIVCODE + 6) \bullet t_{MASTER}$$

A change in DIVCODE will not be recognized until it is stable, and will not pass through intermediate codes. A digital filter is used to guarantee the DIVCODE has settled to a new value before making changes to the output. However, if the delay timing is active during the transition, the actual delay can take on a value between the two settings.

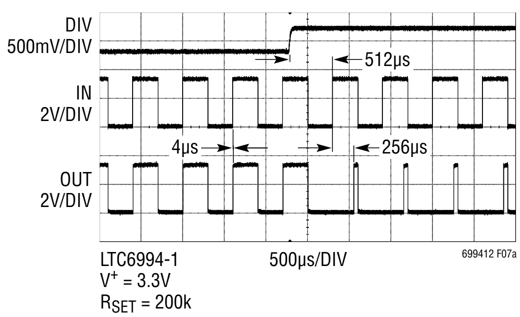


Figure 7a. DIVCODE Change from 0 to 2

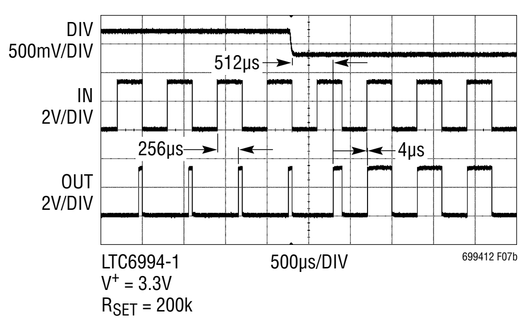


Figure 7b. DIVCODE Change from 2 to 0

Start-Up Time

When power is first applied, the power-on reset (POR) circuit will initiate the start-up time, t_{START}. The OUT pin is held low during this time and the IN pin has no control over the output. The typical value for t_{START} ranges from 0.5ms to 8ms depending on the master oscillator frequency (independent of N_{DIV}):

$$t_{START(TYP)} = 500 \bullet t_{MASTER}$$

During start-up, the DIV pin A/D converter must determine the correct DIVCODE before an output pulse can be generated. The start-up time may increase if the supply or DIV pin voltages are not stable. For this reason, it is recommended to minimize the capacitance on the DIV pin so it will properly track V^+. Less than 100pF will not extend the start-up time.

At the end of t_{START} the DIVCODE and IN pin settings are recognized, and the state of the IN pin is transferred to the output (without additional delay). If IN is high at the end of t_{START}, OUT will go high. Otherwise OUT will remain low. The LTC6994-2 is the exception because it inverts the signal. At this point, the LTC6994 is ready to respond to rising/falling edges on the input.

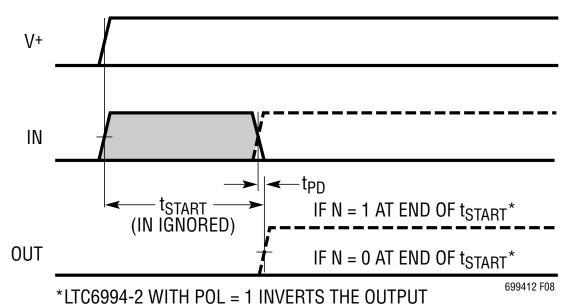


Figure 8. Start-Up Timing Diagram

APPLICATIONS INFORMATION

Basic Operation

The simplest and most accurate method to program the LTC6994 is to use a single resistor, R_{SET}, between the SET and GND pins. The design procedure is a 3-step process.

Step 1: Select the LTC6994 Version and POL Bit Setting.

Choose LTC6994-1 to delay one (rising or falling) input transition. The POL bit then defines which edge is to be delayed. POL = 0 delays rising edges. POL = 1 delays falling edges.

Choose LTC6994-2 to delay rising and falling edges. Set POL = 0 for normal operation, or POL = 1 to invert the output.

Step 2: Select the N_{DIV} Frequency Divider Value.

As explained earlier, the voltage on the DIV pin sets the DIVCODE which determines both the POL bit and the N_{DIV} value. For a given delay time (t_{DELAY}), N_{DIV} should be selected to be within the following range:

$$\frac{t_{DELAY}}{16\mu s} \le N_{DIV} \le \frac{t_{DELAY}}{1\mu s} \quad (1)$$

To minimize supply current, choose the lowest N_{DIV} value. However, in some cases a higher value for N_{DIV} will provide better accuracy (see Electrical Characteristics).

Table 1 can also be used to select the appropriate N_{DIV} values for the desired t_{DELAY}.

With POL already chosen, this completes the selection of DIVCODE. Use Table 1 to select the proper resistor divider or V_{DIV}/V^+ ratio to apply to the DIV pin.

Step 3: Calculate and Select R_{SET}.

The final step is to calculate the correct value for R_{SET} using the following equation:

$$R_{SET} = \frac{50k}{1\mu s} \bullet \frac{t_{DELAY}}{N_{DIV}} \quad (2)$$

Select the standard resistor value closest to the calculated value.

Example: Design a one-shot circuit to delay falling edges by t_{DELAY} = 100µs with minimum power consumption.

Step 1: Select the LTC6994 Version and POL Bit Setting.

To delay negative transitions, choose the LTC6994-1 with POL = 1.

Step 2: Select the N_{DIV} Frequency Divider Value.

Choose an N_{DIV} value that meets the requirements of Equation (1), using t_{DELAY} = 100µs:

$$6.25 \le N_{DIV} \le 100$$

Potential settings for N_{DIV} include 8 and 64. N_{DIV} = 8 is the best choice, as it minimizes supply current by using a large R_{SET} resistor. POL = 1 and N_{DIV} = 8 requires DIVCODE = 14. Using Table 1, choose R1 = 102k and R2 = 976k values to program DIVCODE = 14.

Step 3: Select R_{SET}.

Calculate the correct value for R_{SET} using Equation (2).

$$R_{SET} = \frac{50k}{1\mu s} \bullet \frac{100\mu s}{8} = 625k$$

Since 625k is not available as a standard 1% resistor, substitute 619k if a –0.97% shift in t_{DELAY} is acceptable. Otherwise, select a parallel or series pair of resistors such as 309k and 316k to attain a more precise resistance.

The completed design is shown in Figure 9.

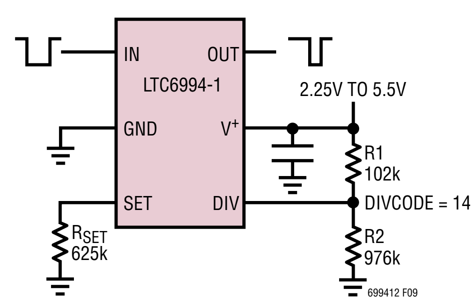


Figure 9. 100µs Negative-Edge Delay

APPLICATIONS INFORMATION

Voltage-Controlled Delay

With one additional resistor, the LTC6994 output delay can be manipulated by an external voltage. As shown in Figure 10, voltage V_{CTRL} sources/sinks a current through R_{MOD} to vary the I_{SET} current, which in turn modulates the delay as described in Equation (3):

$$t_{DELAY} = \frac{N_{DIV} \bullet R_{MOD}}{50k\Omega} \bullet \frac{1\mu s}{1 + \frac{R_{MOD}}{R_{SET}} - \frac{V_{CTRL}}{V_{SET}}} \quad (3)$$

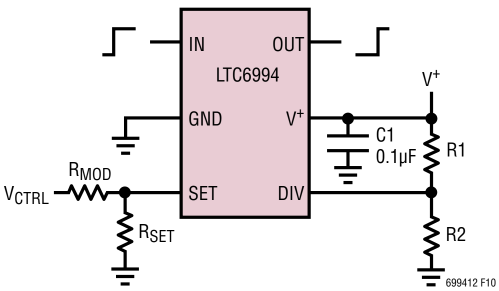


Figure 10. Voltage-Controlled Delay

Digital Delay Control

The control voltage can be generated by a DAC (digital-to-analog converter), resulting in a digitally-controlled delay. Many DACs allow for the use of an external reference. If such a DAC is used to provide the V_{CTRL} voltage, the V_{SET} dependency can be eliminated by buffering V_{SET} and using it as the DAC's reference voltage, as shown in Figure 11. The DAC's output voltage now tracks any V_{SET} variation and eliminates it as an error source. The SET pin cannot be tied directly to the reference input of the DAC because the current drawn by the DAC's REF input would affect the delay.

I_{SET} Extremes (Master Oscillator Frequency Extremes)

When operating with I_{SET} outside of the recommended 1.25µA to 20µA range, the master oscillator operates outside of the 62.5kHz to 1MHz range in which it is most accurate.

The oscillator will still function with reduced accuracy for I_{SET} < 1.25µA. At approximately 500nA, the oscillator will stop. Under this condition, the output pulse can still be initiated, but will not terminate until I_{SET} increases and the master oscillator starts again.

At the other extreme, it is not recommended to operate the master oscillator beyond 2MHz because the accuracy of the DIV pin ADC will suffer.

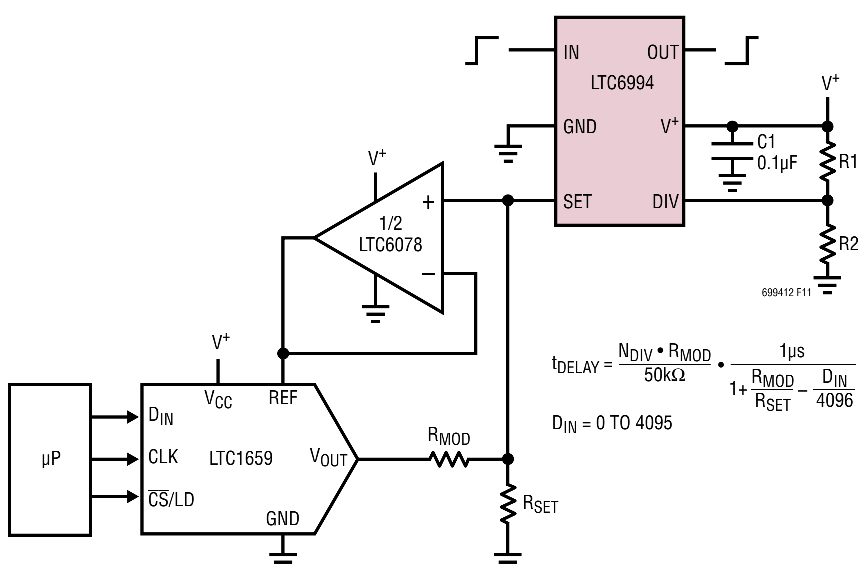


Figure 11. Digitally Controlled Delay

APPLICATIONS INFORMATION

Settling Time

Following a 2× or 0.5× step change in I_{SET}, the output delay takes approximately six master clock cycles (6 • t_{MASTER}) to settle to within 1% of the final value. An example is shown in Figure 12, using the circuit in Figure 10.

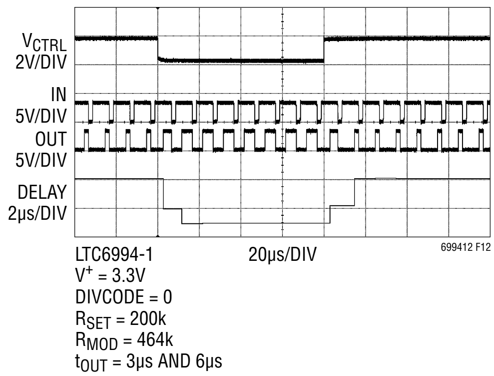


Figure 12. Typical Settling Time

Coupling Error

The current sourced by the SET pin is used to bias the internal master oscillator. The LTC6994 responds to changes in I_{SET} almost immediately, which provides excellent settling time. However, this fast response also makes the SET pin sensitive to coupling from digital signals, such as the IN input.

Even an excellent layout (examples are provided in the next section) will allow *some* coupling between IN and SET that can affect fast output pulses. Additional error is included in the specified accuracy for N_{DIV} = 1 to account for this.

A very poor layout can actually degrade performance further. The PCB layout should avoid routing SET next to IN (or any other fast-edge, wide-swing signal).

APPLICATIONS INFORMATION

Power Supply Current

TBA

Supply Bypassing and PCB Layout Guidelines

The LTC6994 is an accurate monostable multivibrator when used in the appropriate manner. The part is simple to use and by following a few rules, the expected performance is easily achieved. Adequate supply bypassing and proper PCB layout are important to ensure this.

Figure 13 shows example PCB layouts for both the SOT-23 and DCB packages using 0603 sized passive components. The layouts assume a two layer board with a ground plane layer beneath and around the LTC6994. These layouts are a guide and need not be followed exactly.

1. Connect the bypass capacitor, C1, directly to the V^+ and GND pins using a low inductance path. The connection from C1 to the V^+ pin is easily done directly on the top layer. For the DCB package, C1's connection to GND is also simply done on the top layer. For the SOT-23, OUT can be routed through the C1 pads to allow a good C1 GND connection. If the PCB design rules do not allow that, C1's GND connection can be accomplished through multiple vias to the ground plane. Multiple vias for both the GND pin connection to the ground plane and the C1 connection to the ground plane are recommended to minimize the inductance. Capacitor C1 should be a 0.1µF ceramic capacitor.
2. Place all passive components on the top side of the board. This minimizes trace inductance.
3. Place R_{SET} as close as possible to the SET pin and make a direct, short connection. The SET pin is a current summing node and currents injected into this pin directly modulate the output delay. Having a short connection minimizes the exposure to signal pickup.
4. Connect R_{SET} directly to the GND pin. Using a long path or vias to the ground plane will not have a significant affect on accuracy, but a direct, short connection is recommended and easy to apply.
5. Use a ground trace to shield the SET pin. This provides another layer of protection from radiated signals.
6. Place R1 and R2 close to the DIV pin. A direct, short

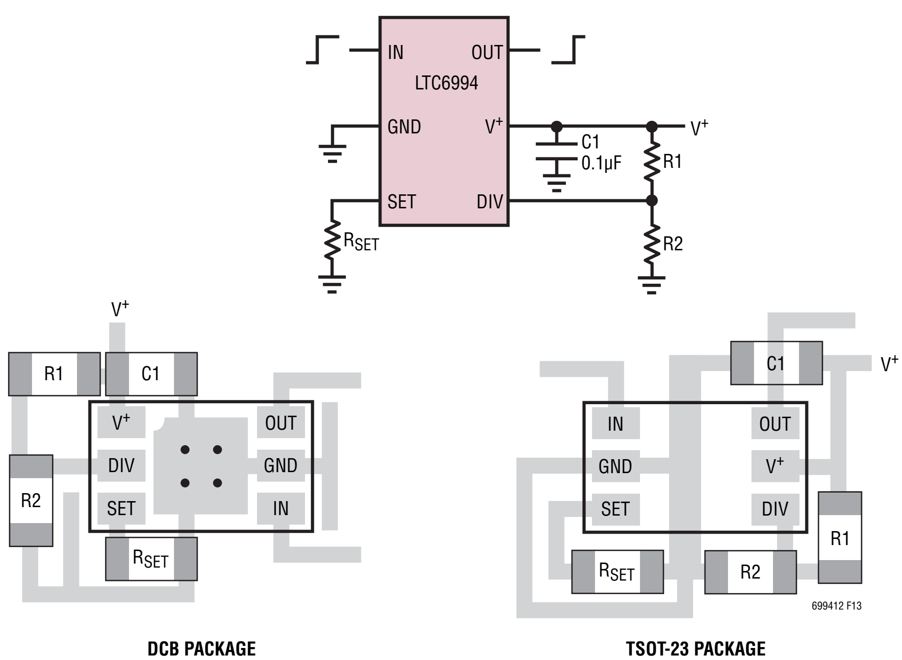
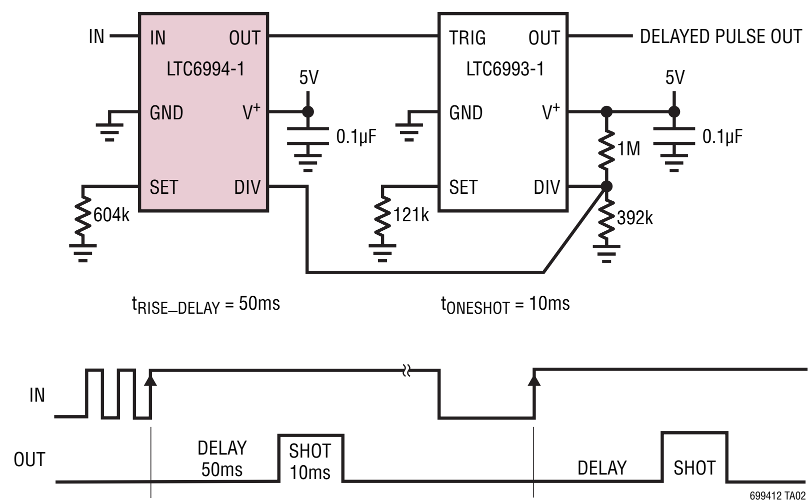


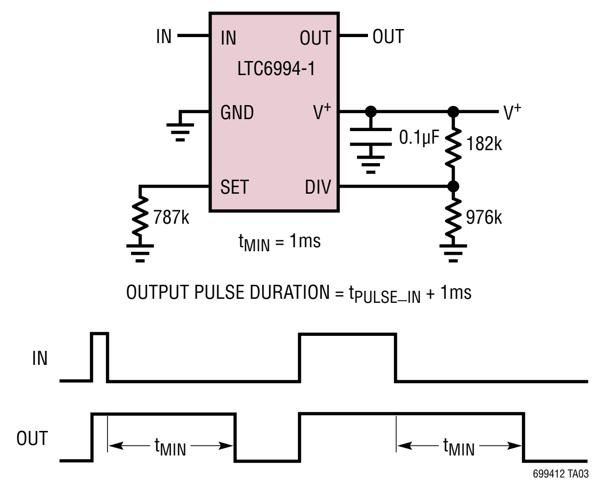
Figure 13. Supply Bypassing and PCB Layout

TYPICAL APPLICATIONS

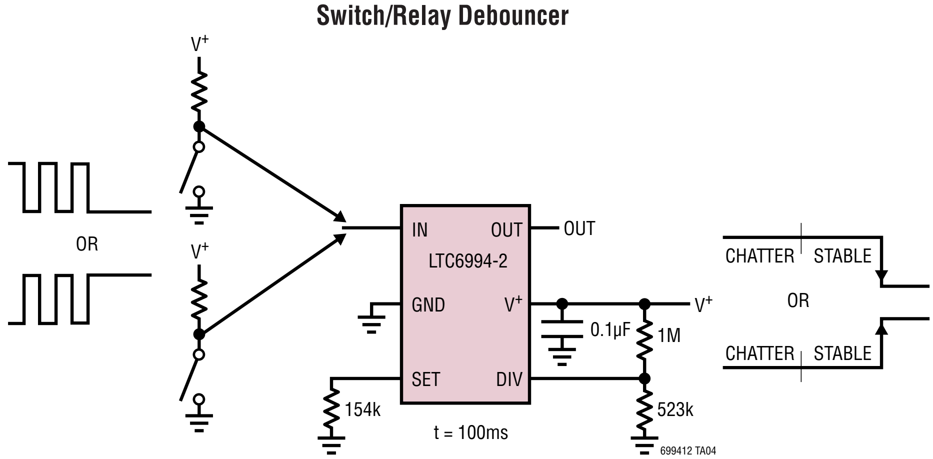
Delayed One-Shot



Pulse Stretcher



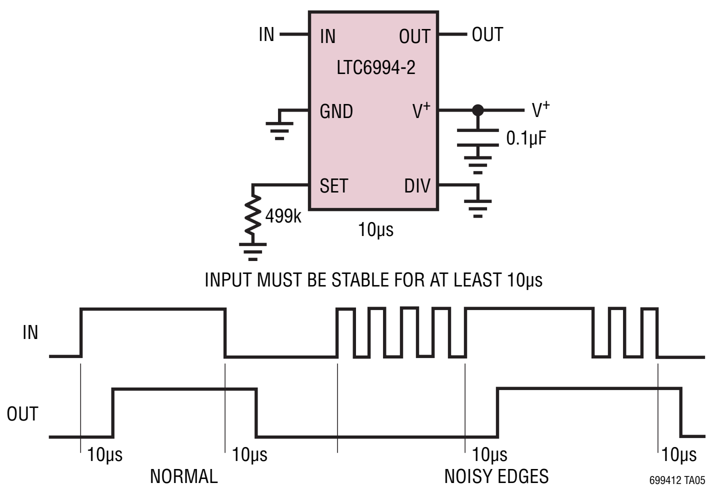
Switch/Relay Debouncer



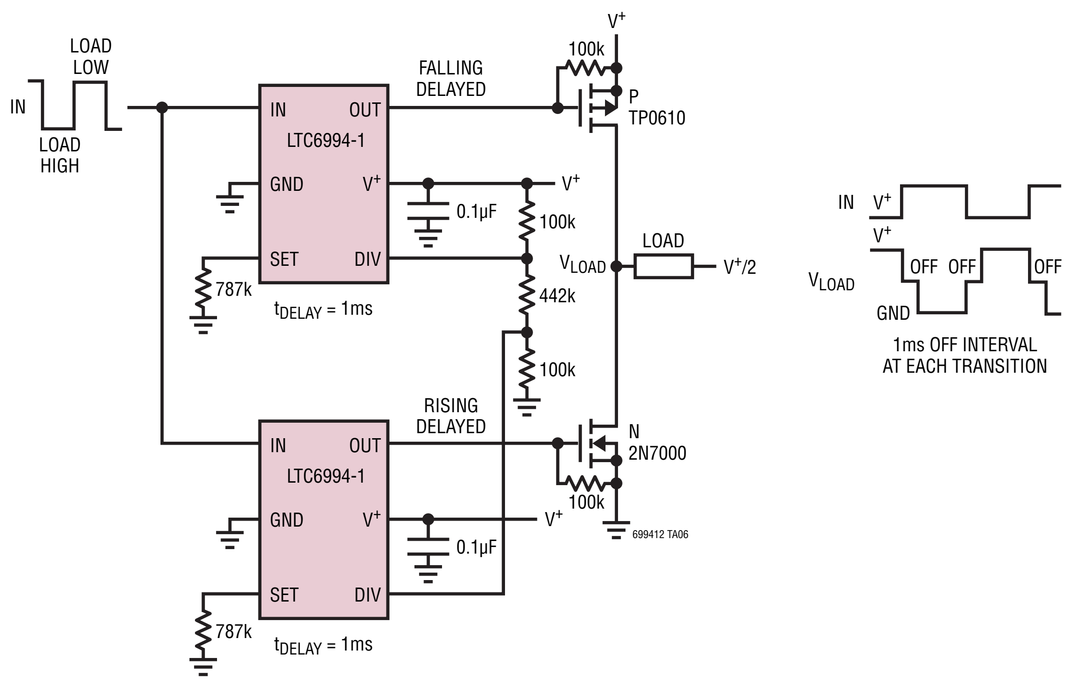
OUTPUT GOES TO SAME FINAL LEVEL OF INPUT
AFTER STABLE FOR 100ms

TYPICAL APPLICATIONS

Edge Chatter Filter

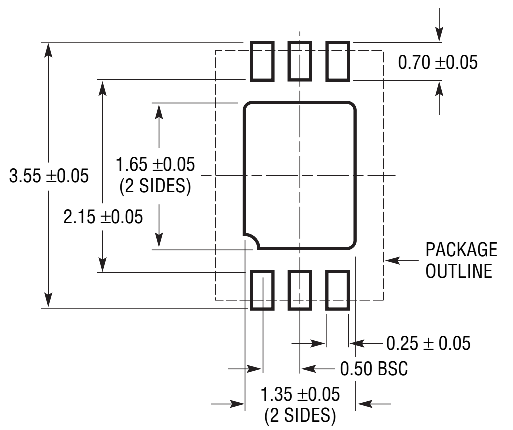


Crossover Gate—Break-Before-Make Interval Timer

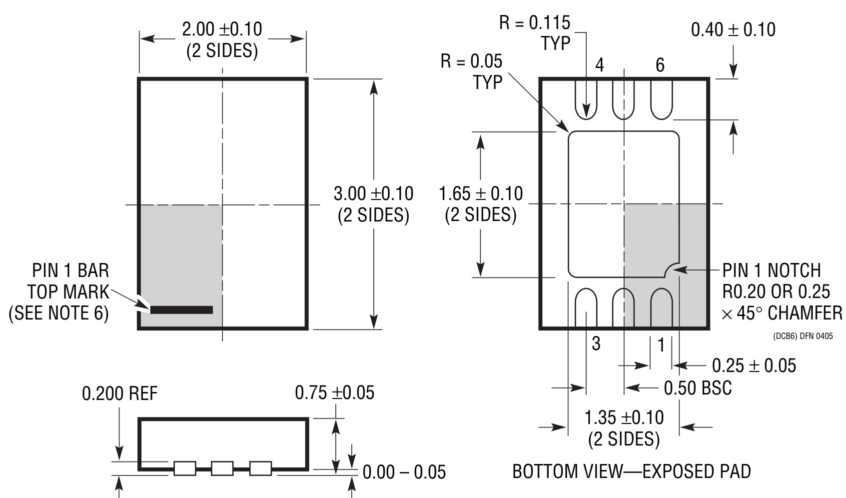


PACKAGE DESCRIPTION

DCB Package
6-Lead Plastic DFN (2mm × 3mm)
(Reference LTC DWG # 05-08-1715 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

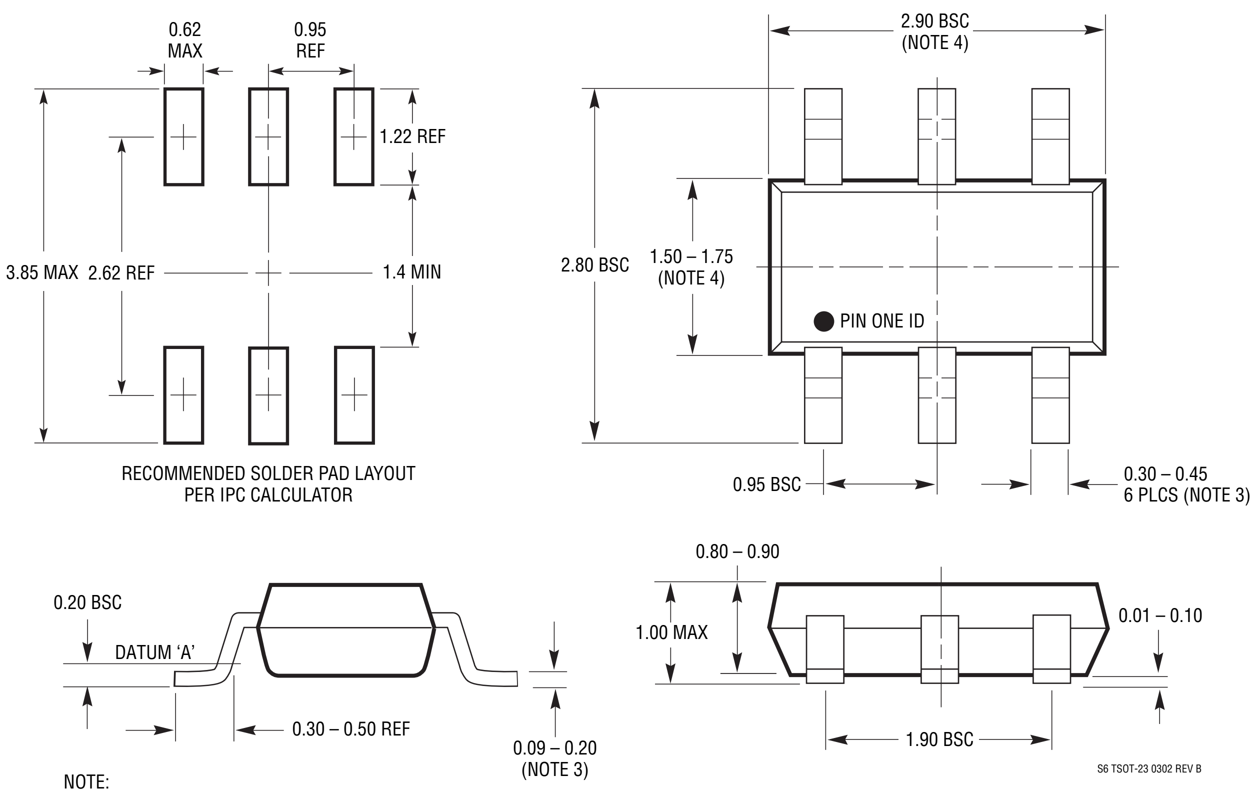


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (TBD)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

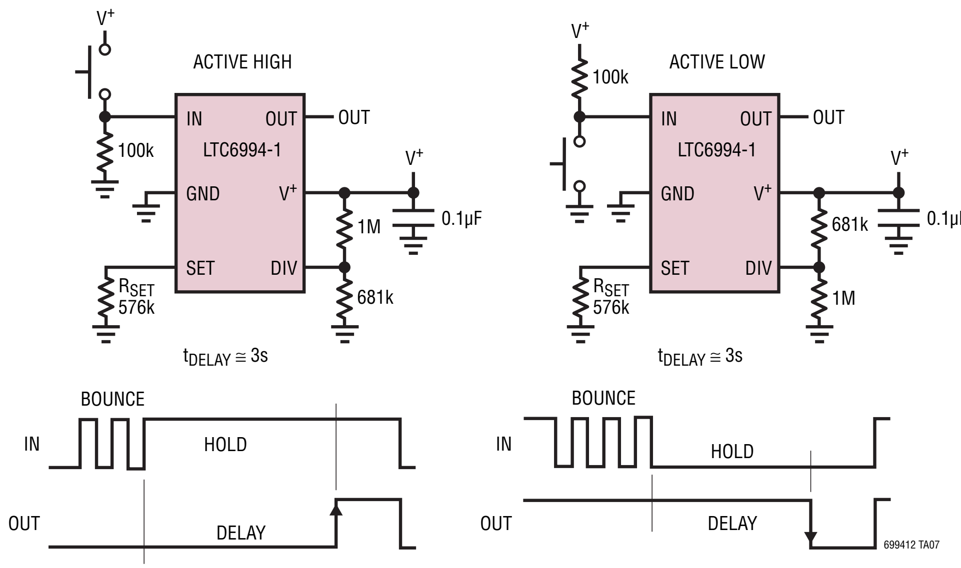
S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

TYPICAL APPLICATION

Press-and-Hold (0.3s to 4s) Delay Timer



R_{SET} (kΩ) = 190 • t_{DELAY} (SECONDS)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1799	1MHz to 33MHz ThinSOT Silicon Oscillator	Wide Frequency Range
LTC6900	1MHz to 20MHz ThinSOT Silicon Oscillator	Low Power, Wide Frequency Range
LTC6906/LTC6907	10kHz to 1MHz or 40kHz ThinSOT Silicon Oscillator	Micropower, I_{SUPPLY} = 35µA at 400kHz
LTC6930	Fixed Frequency Oscillator, 32.768kHz to 8.192MHz	0.09% Accuracy, 110µs Start-Up Time, 105µA at 32kHz
LTC6990	TimerBlox: Voltage-Controlled Silicon Oscillator	Fixed-Frequency or Voltage-Controlled Operation
LTC6991	TimerBlox: Resettable Low Frequency Oscillator	Clock Periods up to 9.5 hours
LTC6992	TimerBlox: Voltage-Controlled Pulse Width Modulator (PWM)	Simple PWM with Wide Frequency Range
LTC6993	TimerBlox: Monostable Pulse Generator (One-Shot)	Resistor-Programmable Pulse Width of 1µs to 34s

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