



# Serially Programmable Frequency Generator

## General Description

The AV9110 generates user specified clock frequencies using an externally generated input reference, such as 14.318 MHz or 10.00 MHz crystal connected between pins 1 and 14. Alternately, a TTL input reference clock signal can be used. The output frequency is determined by a 24-bit digital word entered through the serial port. The serial port enables the user to change the output frequency on-the-fly.

The clock outputs utilize CMOS level output buffers that operate up to 130 MHz.

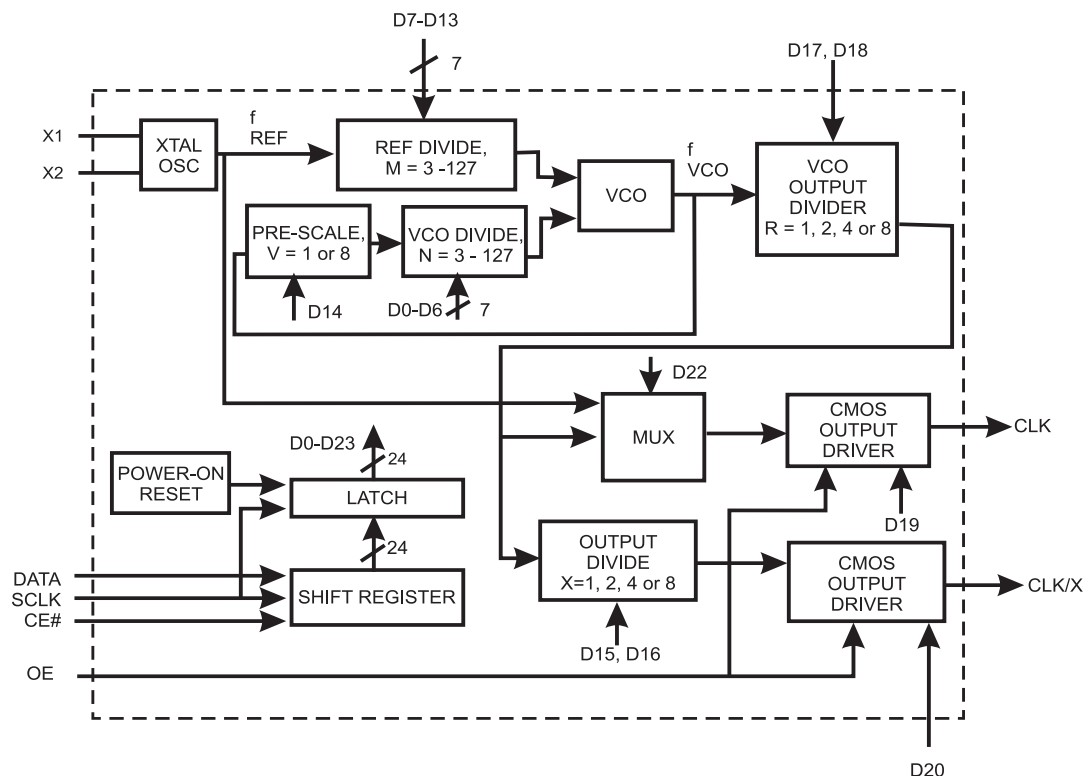
## Features

- Complete user programmability of output frequency through serial input data port
- On-chip Phase-Locked Loop for clock generation
- Generates accurate frequencies up to 130 MHz
- Tristate CMOS outputs
- 5 volt power supply
- Low power CMOS technology
- 14-pin DIP or 150-mil SOIC
- Very low jitter
- Wide operating range VCO

## Applications

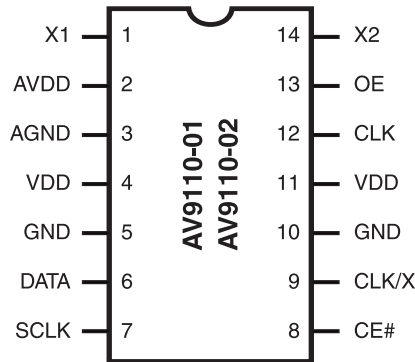
Graphics: The AV9110 generates low jitter, high speed pixel (or dot) clocks. It can be used to replace multiple expensive high speed crystal oscillators. The flexibility of this device allows it to generate nonstandard graphics clocks, allowing the user to program frequencies on-the-fly.

## Block Diagram





## Pin Configuration



14 Pin Dip, SOIC

## Clock Reference Implementations: AV9110-01 vs. AV9110-02

The AV9110 requires a stable reference clock (5 to 32 MHz) to generate a stable, low jitter output clock. The AV9110-01 is optimized to use an external quartz crystal as a frequency reference, without the need of additional external components. The AV9110-02 is optimized to accept an TTL clock reference. Either device can be used with an external crystal or accept a TTL clock reference, although extra components may be required. The various combinations implied are summarized in Figure 2 (see page 7).

## Pin Descriptions

| PIN NUMBER | PIN NAME | PIN TYPE | DESCRIPTION                                      |
|------------|----------|----------|--|
| 1          | X1       | Input    | Crystal input or TTL reference clock.            |
| 2          | AVDD     | Power    | ANALOG power supply. Connect to +5V.             |
| 3          | AGND     | Power    | ANALOG GROUND.                                   |
| 4          | VDD      | Power    | Digital power supply. Connect to +5V.            |
| 5          | GND      | Power    | Digital GROUND.                                  |
| 6          | DATA     | Input    | Serial DATA pin.                                 |
| 7          | SCLK     | Input    | SERIAL CLOCK. Clocks shift register.             |
| 8          | CE#      | Input    | CHIP ENABLE. Active low, controls data transfer. |
| 9          | CLK/X    | Output   | CMOS CLOCK divided by X output.                  |
| 10         | GND      | Power    | Digital GROUND.                                  |
| 11         | VDD      | Power    | Digital power supply. Connect to +5V.            |
| 12         | CLK      | Output   | CMOS CLOCK output.                               |
| 13         | OE       | Input    | OUTPUT ENABLE. Tristates both outputs when low.  |
| 14         | X2       | Output   | Crystal input or TTL reference clock.            |



### Absolute Maximum Ratings

- Supply Voltage ..... 7.0 V
- Voltage on I/O pins referenced to GND ..... GND -0.5 V to V<sub>DD</sub> +0.5 V
- Operating Temperature under bias ..... 0°C to +70°C
- Power dissipation ..... 0.8 Watts
- Storage Temperature ..... -65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Electrical Characteristics

V<sub>DD</sub> = +5V±10%, T<sub>A</sub> = 0 – 70° C unless otherwise stated

| DC/STATIC                                     |                                       |                                   |      |        |     |       |
|---|---------------------------------------|-----------------------------------|------|--------|-----|-------|
| PARAMETER                                     | SYMBOL                                | TEST CONDITIONS                   | MIN  | TYP    | MAX | UNITS |
| Input Low Voltage                             | V <sub>IL</sub>                       | V <sub>DD</sub> = 5V              | -    | -      | 0.8 | V     |
| Input High Voltage                            | V <sub>IH</sub>                       | V <sub>DD</sub> = 5V              | 2.0  | -      | -   | V     |
| Input Low Current                             | I <sub>IL</sub>                       | V <sub>IN</sub> = 0V              | -    | -      | -5  | µA    |
| Input High Current                            | I <sub>IH</sub>                       | V <sub>IN</sub> = V <sub>DD</sub> | -    | -      | 5   | µA    |
| Output Low Voltage <sup>1</sup>               | V <sub>OL</sub>                       | I <sub>OL</sub> = 8Ma             | -    | -      | 0.4 | V     |
| Output High Voltage <sup>1</sup>              | V <sub>OH</sub> I <sub>OH</sub> = 8Ma |                                   | 2.4  | -      | -   | V     |
| Input Clock Rise Time <sup>1</sup>            | I <sub>CLKr</sub>                     |                                   | -    | -      | 20  | ns    |
| Input Clock Fall Time <sup>1</sup>            | I <sub>CLKf</sub>                     |                                   | -    | -      | 20  | ns    |
| Supply Current                                | I <sub>DD</sub>                       | No load                           | -    | 25     | -   | mA    |
| AC/DYNAMIC                                    |                                       |                                   |      |        |     |       |
| Output frequency range                        | f <sub>o</sub>                        |                                   | 0.78 | -      | 130 | MHz   |
| Rise time, 20-80% <sup>1</sup>                | t <sub>r</sub>                        | 25pF load                         | -    | -      | 3   | ns    |
| Fall time, 80-20% <sup>1</sup>                | t <sub>f</sub>                        | 25pF load                         | -    | -      | 3   | ns    |
| Duty cycle <sup>1</sup> @ 50%                 | d <sub>t</sub>                        | 25pF load                         | 40   | -      | 60  | %     |
| Jitter, 1 sigma <sup>1</sup>                  |                                       |                                   | -    | ±40    | -   | ps    |
| Jitter, absolute <sup>1</sup>                 |                                       |                                   | -    | ±125   | -   | ps    |
| Input reference freq.; AV9110-01 <sup>1</sup> | f <sub>REF</sub>                      | Crystal input                     | 5    | 14.318 | 32  | MHz   |
| Input reference freq.; AV9110-02 <sup>1</sup> | f <sub>REF</sub>                      | TTL input                         | 0.6  | 14.318 | 32  | MHz   |
| Input DATA or SCLK frequency <sup>1</sup>     | f <sub>DATA</sub>                     |                                   | -    | -      | 32  | MHz   |
| Skew, Output to Output/X1                     | t <sub>skew</sub>                     |                                   | -    | 400    | -   | ps    |

**Note 1:** Parameter is guaranteed by design and characterization. Not 100% tested in production.



## Serial Programming

The AV9110 is programmed to generate clock frequencies by entering data through the shift register. Figure 1 displays the proper timing sequence. On the negative going edge of CE#, the shift register is enabled and the data at the DATA pin is loaded into the shift register on the rising edge of the SCLK. Bit D0 is loaded first, followed by D1, D2, etc. This data consists of the 24 bits shown in the Shift Register Bit Assignment in Table 1, and therefore takes 24 clock cycles to load. An internal counter then disables the input and transfers

the data to internal latches on the rising edge of the 24th cycle of the SCLK. Any data entered after the 24th cycle is ignored until CE# must remain low for a minimum of 24 SCLK clock cycles. If CE# is taken high before 24 clock cycles have elapsed, the data is ignored (no frequency change occurs) and the counter is reset. Tables 1 and 2 display the bit location for generating the output clock frequency and the output divider circuitry, respectively.

| BIT | ASSIGNMENT  | EQUATION VARIABLE | DEFAULT |     | BIT |
|-----|---|-------------------|---------|-----|-----|
|     |   |                   | -01     | -02 |     |
| 0   | VCO frequency divider (LSB)                             | N<br>Integer      | 1       | 1   | 0   |
| 1   | VCO frequency divider                                   |                   | 1       | 1   | 1   |
| 2   | VCO frequency divider                                   |                   | 1       | 1   | 2   |
| 3   | VCO frequency divider                                   |                   | 1       | 1   | 3   |
| 4   | VCO frequency divider                                   |                   | 1       | 1   | 4   |
| 5   | VCO frequency divider                                   |                   | 1       | 1   | 5   |
| 6   | VCO frequency divider (MSB)                             | M<br>Integer      | 1       | 1   | 6   |
| 7   | Reference frequency divider (LSB)                       |                   | 0       | 0   | 7   |
| 8   | Reference frequency divider                             |                   | 1       | 1   | 8   |
| 9   | Reference frequency divider                             |                   | 0       | 0   | 9   |
| 10  | Reference frequency divider                             |                   | 0       | 0   | 10  |
| 11  | Reference frequency divider                             |                   | 1       | 1   | 11  |
| 12  | Reference frequency divider                             |                   | 0       | 0   | 12  |
| 13  | Reference frequency divider (MSB)                       | V                 | 0       | 0   | 13  |
| 14  | VCO pre-scale divide (0=divide by 1, 1=divide by 8)     |                   | 0       | 0   | 14  |
| 15  | CLK/X output divide COD0 (see Table 2)                  | X                 | 0       | 1   | 15  |
| 16  | CLK/X output divide COD1 (see Table 2)                  |                   | 1       | 0   | 16  |
| 17  | VCO output divide VOD0 (see Table 3)                    | R                 | 0       | 0   | 17  |
| 18  | VCO output divide VOD1 (see Table 3)                    |                   | 1       | 1   | 18  |
| 19  | Output enable CLK (0=tristate)                          |                   | 1       | 1   | 19  |
| 20  | Output enable CLK/X (0=tristate)                        |                   | 1       | 1   | 20  |
| 21  | Reserved. Should be programmed high (1)                 |                   | 1       | 1   | 21  |
| 22  | Reference clock select on CLK (1 = reference frequency) |                   | 0       | 0   | 22  |
| 23  | Reserved. Should be programmed high (1)                 |                   | 1       | 1   | 23  |



## Output Divider Turth Tables

**Table 2**

| COD1 | COD0 | CLK/X Output Divide (X) |
|------|------|-------------------------|
| 0    | 0    | 1                       |
| 0    | 1    | 2                       |
| 1    | 0    | 4                       |
| 1    | 1    | 8                       |

**Table 3**

| COD1 | COD0 | VCO Output Divide (R) |
|------|------|-----------------------|
| 0    | 0    | 1                     |
| 0    | 1    | 2                     |
| 1    | 0    | 4                     |
| 1    | 1    | 8                     |

## Programming the PLL

The AV9110 has a wide operating range but it is recommended that it is operated within the following limits:

|  |   |
|--|---|
| $2 \text{ MHz} < f_{\text{REF}} < 32 \text{ MHz}$            | $f_{\text{REF}} = \text{Input reference frequency}$     |
| $200 \text{ kHz} < \frac{f_{\text{REF}}}{M} < 5 \text{ MHz}$ | $M = \text{Reference divide, 3 to 127}$                 |
| $50 \text{ MHz} < f_{\text{VCO}} < 250 \text{ MHz}$          | $f_{\text{VCO}} = \text{VCO output frequency}$          |
| $f_{\text{VCO}} < 250 \text{ MHz}$                           | $f_{\text{CLK}} = \text{CLK or CLK/X output frequency}$ |

The AV9110 is a classical PLL circuit and the VCO output frequency is given by:

$$f_{\text{VCO}} = \frac{N \cdot V \cdot f_{\text{REF}}}{M}$$

Where  $N = \text{VCO divided, 3 to 127}$   
 $M = m \text{ Reference divide, 3 to 127}$   
 $V = \text{Perscale, 1 or 8}$

The 2 output drivers then give the following frequencies:

$$f_{\text{CLK}} = \frac{f_{\text{VCO}}}{R} = \frac{N \cdot V \cdot f_{\text{REF}}}{M \cdot R} \quad \text{or } f_{\text{REF}} \text{ (output mixable by bit 17)}$$

$$f_{\text{CLK/X}} = \frac{f_{\text{VCO}}}{R \cdot X} = \frac{f_{\text{VCLK}}}{X} \quad \text{Where } R, X = \text{output dividers 1, 2, 4 or 8}$$

Notes:

1. Output frequency accuracy will depend solely on input reference frequency accuracy.
2. For output frequencies below 125 MHz, it is recommended that the VCO output divide, R, should be 2 or greater. This will give improved duty cycle.
3. The minimum output frequency step size is approximately 0.2% due to the divider range provided.

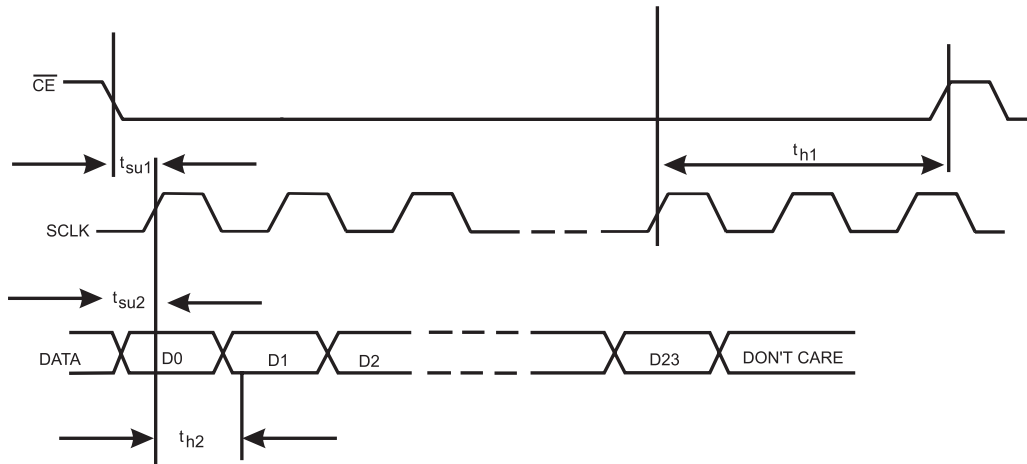


Figure 1 - Serial Programming

AC Timing

| Parameter | Minimum time (ns) |
|-----------|-------------------|
| $t_{su1}$ | 10                |
| $t_{su2}$ | 10                |
| $t_{h1}$  | 10                |
| $t_{h2}$  | 10                |

Frequency Acquisition Time

Frequency acquisition (or “lock”) time is the time that it takes to change from one frequency to another, and is a function of the difference between the old and new frequencies. The AV9110 can typically lock to within 1% of a new frequency in less than 200 microseconds. This is also true with power-on.

Power-On Reset

Upon power-up the internal latches are preset to provide the following output clock frequencies (14.318 MHz reference assumed):

|           |            |              |
|-----------|------------|--------------|
| Device    | CLK output | CLK/X output |
| AV9110-01 | 25.175 MHz | 6.29 MHz     |
| AV9110-02 | 25.175 MHz | 12.59 MHz    |

These preset default frequencies can be changed with a custom metal mask, as can other attributes.

The actual numbers of these output clock frequencies (14.318MHz reference assumed) are:

|           |            |              |
|-----------|------------|--------------|
| Device    | CLK output | CLK/X output |
| AV9110-01 | 25.255 MHz | 6.31 MHz     |
| AV9110-02 | 25.255 MHz | 12.63 MHz    |

and these are within 0.32%.

Jitter

For high performance applications, the AV9110 offers extremely low jitter and excellent power supply rejection. The one sigma jitter distribution is typically less than  $\pm 125$ ps. For optimum performance, the device should be decoupled with both a 2.2mF and a 0.1mF capacitor. Refer to Recommended Board Layout diagram on page 8.

Output Enable

The AV9110 outputs can be disabled with either the OE pin or through serial programming. Setting the OE pin low tristates CLK and CLK/X. Alternatively, setting bits D19 and D20 low in the serial word will tristate the two outputs. Both the OE pin and D19 or D20 must be high to enable an output.

Frequency Transition Glitches

The AV9110 starts changing frequency on the rising edge of the 24th serial clock. If the programming of any output divider is changed, the output clock may glitch before locking to the new frequency in less than 200 $\mu$ s with no output glitches (no partial clock cycles).



### AV9110 Quartz Crystal Selection

When an external quartz crystal will be used as a frequency reference for the AV9110, attention needs to be given to crystal selection if accurate reference frequency and output frequency is desired. The AV9110 uses a Pierce oscillator design which operates the quartz crystal in parallel-resonant mode. It requires a quartz crystal cut for parallel-resonant operation to ensure an accurate frequency of oscillation (a less expensive series-resonant crystal can be used with the device but it will oscillate approximately 0.1% too fast). The AV9110-01 has internal crystal load capacitors which result in a total crystal load capacitance of approximately 12pF±10%. The AV9110-02 does not have internal load capacitors, but contributes about 3pF load capacitance to the crystal.

Following is a list of recommended crystal devices for the AV9110. They have been tested by the crystal manufacturer to operate suitably with the AV91xx-series crystal oscillator design, having load capacitance characteristics that are compatible with the AV9110-01.

#### Toyocom

- Part Number  
 TN4-30374 ..... 14.318 MHz surface mount crystal  
 TN4-30375 ..... 20 MHz surface mount crystal  
 TN4-30376 ..... 14.318 MHz through-hole crystal  
 TN4-30377 ..... 20 MHz through-hole crystal

#### Epson

- Part Number  
 MA-505 or ..... Surface mount crystal  
 MA-506  
 CA-301 ..... Through-hole crystal

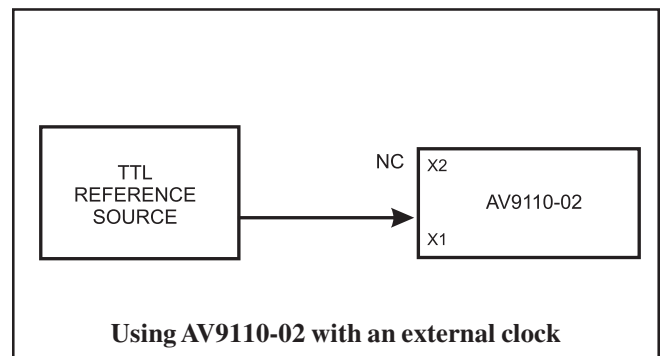
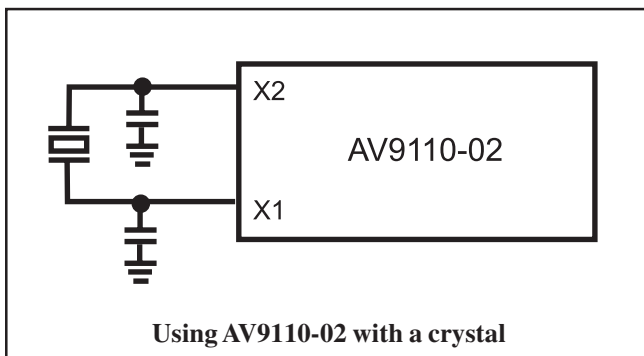
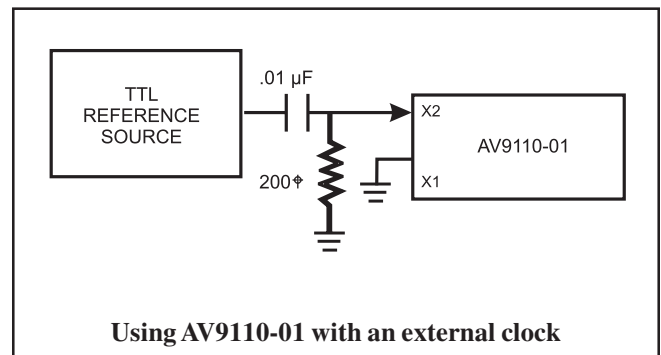
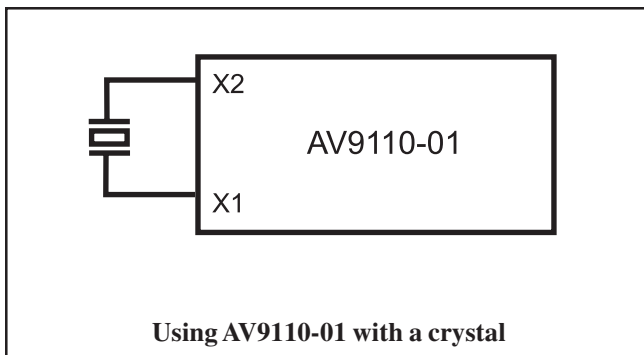
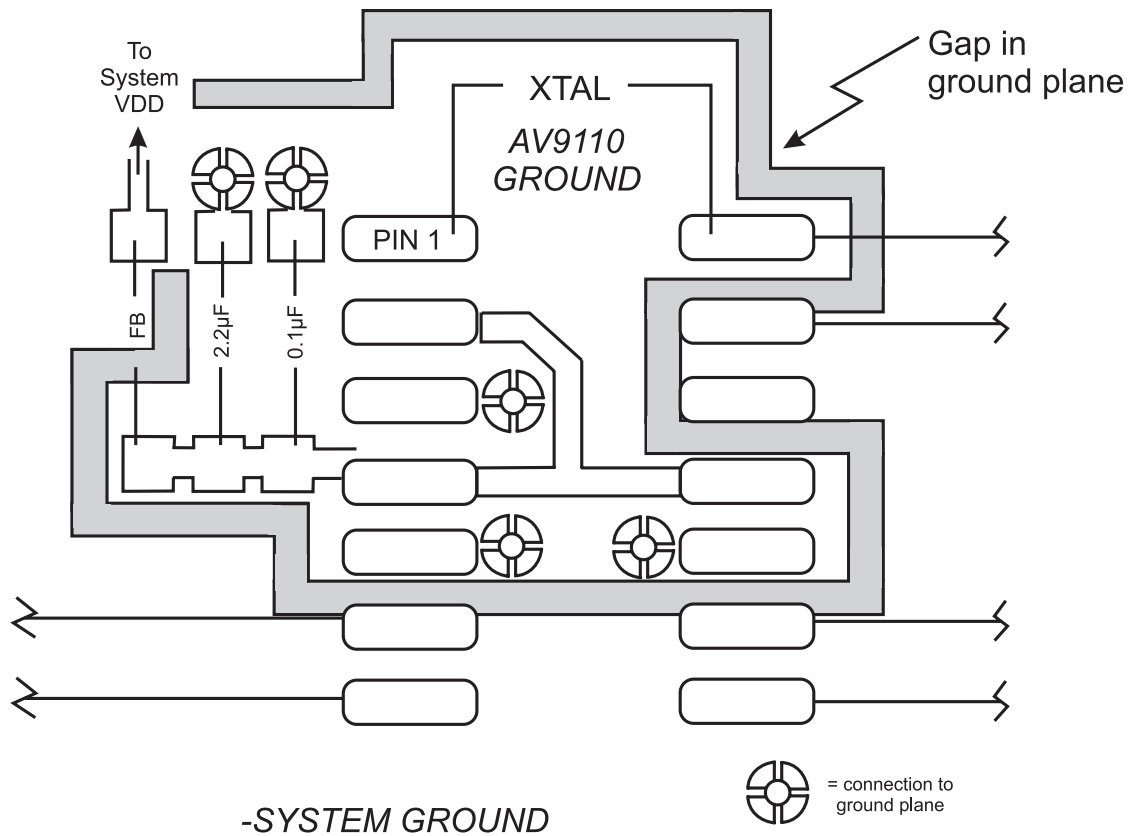


Figure 2 - Clock Reference Combinations

## AV9110 Recommended Board Layout

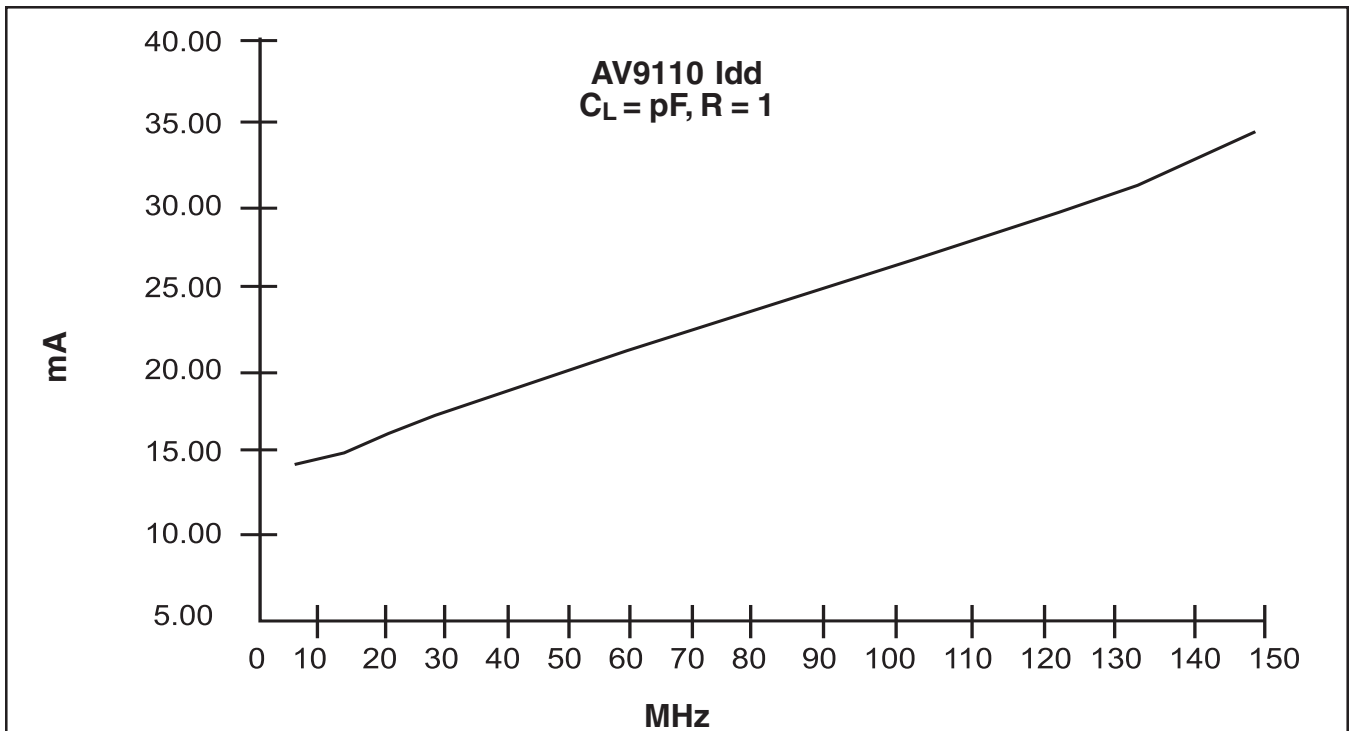
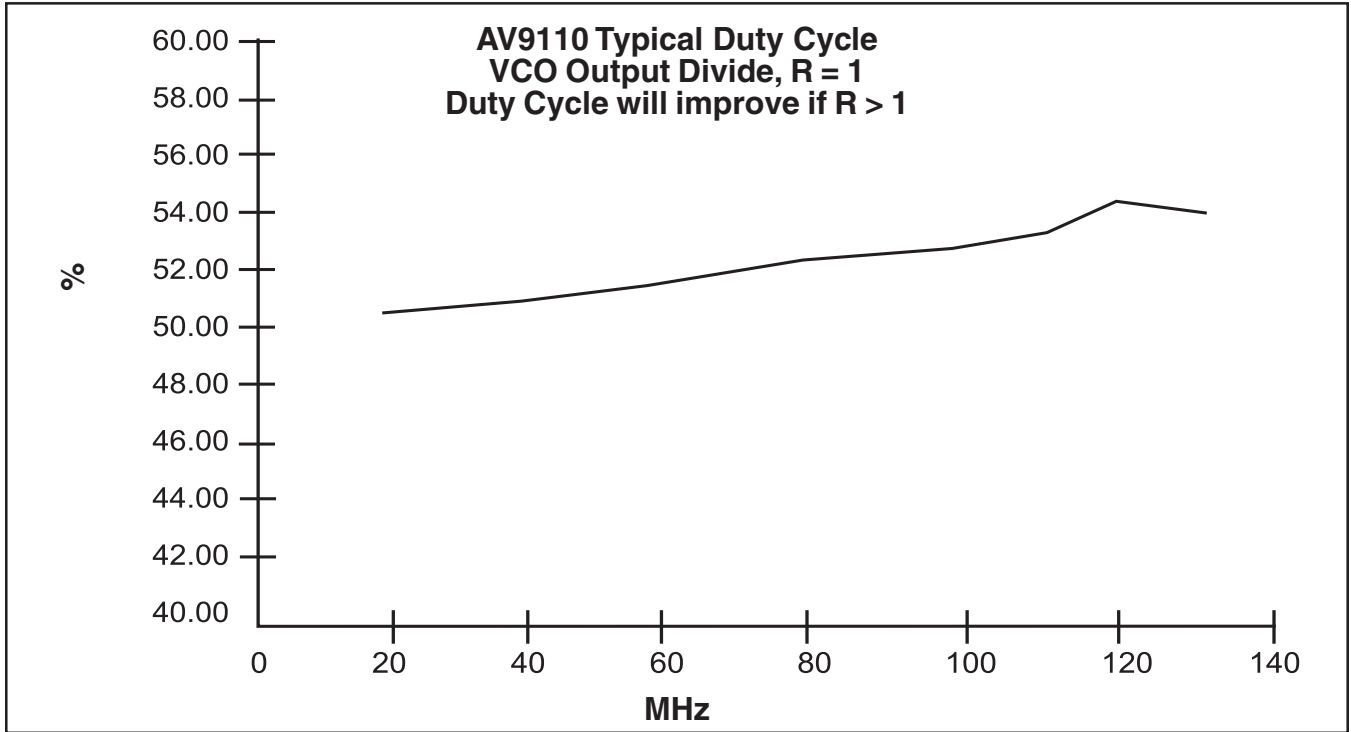


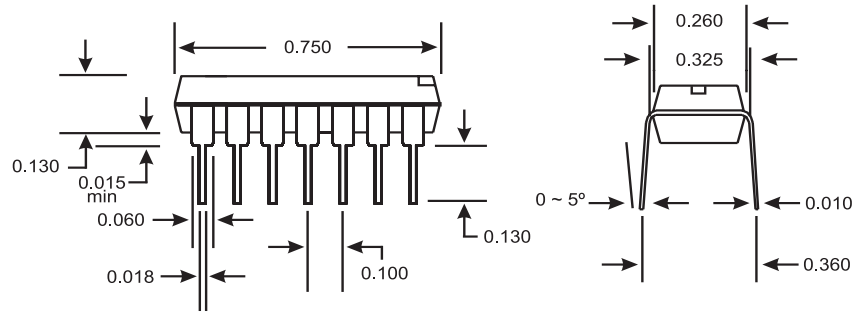
This is the recommended layout for the **AV9110** to maximize clock performance. Shown are the power and ground connections, the ground plane, and the input/output traces.

Use of the isolated ground plane and power connection, as shown, will prevent stray high frequency ground and system noise from coupling to the **AV9110**. As when compared to using the system ground and power planes, this technique will lessen output clock jitter. The isolated ground plane should be connected to the system ground plane at one point near the 2.2mF decoupling cap. For lowest jitter performance, the isolated ground plane should be kept away from clock output pins and traces. Keeping the isolated ground plane area as small as possible will minimize EMI radiation. Use a sufficient gap between the isolated ground plane and system ground plane to prevent AC coupling. The ferrite bead in the VDD line is optional, but will help reduce EMI.

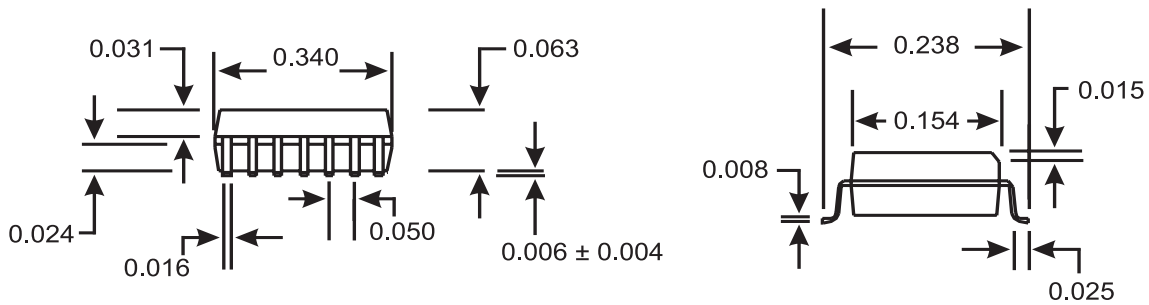
The traces to distribute the output clocks should be over an unbroken system ground or power supply plane. The trace width should be about two times the thickness of the PC board between the trace and the underlying plane. These guidelines help minimize clock jitter and EMI radiation. The traces to distribute power should be as wide as possible.







14-Pin DIP Package



14-Pin 150 mil SOIC Package

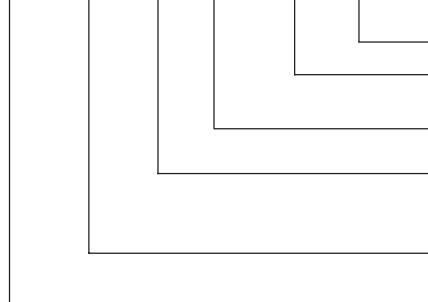
Ordering Information

AV9110-01CN14LF, AV9110-02CN14LF

AV9110-01CS14LF, AV9110-02CS14LF

Example:

ICS XXXX S-PPP X#W LF



Lead Free, RoHS Compliant (Optional)

Lead Count

Lead Count=1,2 or 3 digits

Pattern Number(2 or 3 digit number for parts with ROM code patterns)

Package Type

S=SOIC

N=DIP (plastic)

Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS=Standard Device



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**Revision History**

| Rev. | Issue Date | Description                    | Page # |
|------|------------|--------------------------------|--------|
| G    | 3/19/2008  | added LF ordering Information. | 10     |
|      |            |                                |        |
|      |            |                                |        |
|      |            |                                |        |