TMC2023

CMOS Digital Output Correlator

64-Bit, 25, 30, 35, and 50 MHz

Features

- 25, 30, 35, and 50 MHz correlation rates
- All inputs and outputs TTL compatible
- Serial data input, parallel correlation output
- Programmable word length
- Independently clocked registers
- Programmable threshold detection and flag output
- Available in 24 pin Ceramic and Plastic DIP, 28-lead Plastic and Ceramic chip carrier and 28-contact chip carrier
- Available to Standard Military Drawing (SMD)
- Pin-Compatible with TDC1023
- Output format flexibility
- Three-state outputs
- Low-power CMOS

Applications

- Check sorting equipment
- High density recording
- Bar code identification

Description

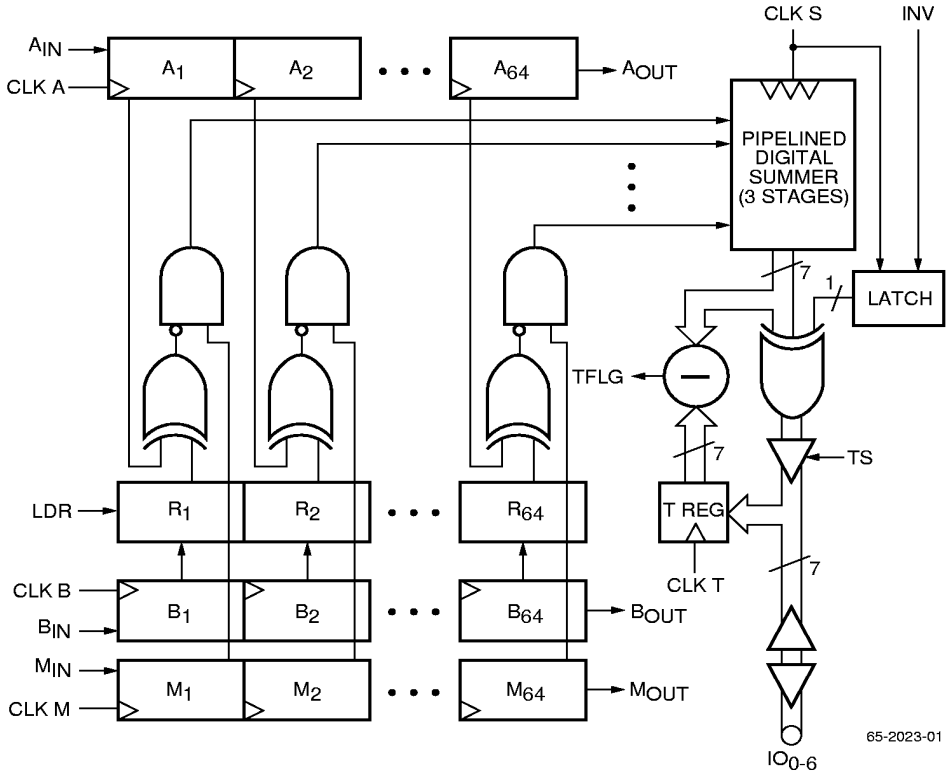
The TMC2023 is a monolithic 64-bit correlator with a 7-bit three-state buffered digital output. This device consists of three 64-bit independently clocked shift registers, one 64-bit reference holding latch, and a 64-bit independently clocked digital summing network. The device is available in versions capable of 25, 30, 35, and 50 MHz parallel correlation rates.

The 7-bit threshold register allows the user to preload a binary number from 0 to 64. Whenever the correlation is equal to or greater than the number in the threshold register, the threshold flag goes HIGH.

The 64-bit shift mask register (M register) allows the user to mask or selectively to choose “no compare” bit positions, thereby accomodating any desired word length.

The reference word is serially shifted into the B register. Bringing LDR HIGH parallel loads the data into the R reference latch. This allows the user to serially preload a new reference word into the B register while correlation is taking

Block Diagram



Rev. 1.0.0

Description (cont.)

place between the A register and the R latch. The two words are continually compared bit-by-bit by exclusive-OR circuits. Each exclusive-OR provides one bit to the digital summer. The output is a 7-bit word representing the number of positions which agree at any one time between the A register and R latch. A control provides either true or inverted binary output formats.

Built with Fairchild Semiconductor's one-micron double level metal OMICRONC™ low power CMOS process, the TMC2023 is available in a 24-pin ceramic side brazed package, 24-pin Plastic Dual-In-Line Package, 28-contact plastic leadless chip carrier and 28-contact chip carrier. The CMOS TMC2023 is pin compatible with the bipolar TDC1023.

Functional Description

General Information

The TMC2023 consists of an input section and an output section. The input section contains the A, B, and M registers, an R latch, XOR/AND logic and a pipelined summer network. The output section consists of threshold, inversion and three-state logic.

Continuous Correlation

The TMC2023 contains three 1 x 64 serial shift registers (A, B, and M). The operation of these registers is identical and each has its own input, output, and clock. As shown in the Timing Diagrams, valid data is loaded into register A (B, M) on the rising edge of CLK A (CLK B, CLK M). Data is valid if present at the input for a setup time of at least t_{SSR} before and a hold time of t_H after the rising clock edge.

The summing process is initiated when the comparison result between the A register and R latch is clocked into the summing network by a rising edge of CLK S. Typically, CLK A and CLK S are tied together so that a new correlation score is computed for each new alignment of the A register and R latch. When LDR goes HIGH, the contents of register B are copied into the R latch. With LDR LOW, a new template may be entered serially into register B, while parallel correlation takes place between register A and the R latch. In the case of continuous correlation, LDR is held HIGH so that the R latch contents continuously track those of the B register.

The summing network consists of three pipelined stages. Therefore, the total correlation score for a given set of A and B register contents appears at the summer output three CLK S cycles later. Data on the output pins IO_{0-6} is available after an additional propagation delay, denoted t_{DCOR} on the Timing Diagrams.

The correlation result is compared with the contents of the threshold register. TFLG goes HIGH if the correlation equals or exceeds the threshold value. TFLG is valid after a delay of t_{DF} from the third CLK S rising edge.

Applications (cont.)

- Radar signature recognition
- Video frame synchronization
- Electro-optical navigation
- Pattern and character recognition
- Cross-correlation control systems
- Error correction coding
- Asynchronous communication
- Matched filtering

Cross-Correlation

When LDR goes HIGH, the B register contents are copied into the reference latch (R latch). This useful feature allows correlation to take place between data in the R latch and the A register while a new reference is being serially clocked into the B register. If the new reference is n bits long, it requires n rising edges of CLK to load this data into the B register. For the timing diagram, n = 64. LDR is set HIGH during the final (n^{th}) CLK B cycle, so that the new reference word is copied into the R latch. The minimum LOW and HIGH level pulse widths for LDR are shown as t_{PWL} and t_{PWH}, respectively.

After the new reference is loaded, the data to be correlated is clocked through the A register. Typically, CLK A and CLK S can be tied together. This allows a new correlation score to be computed for each shift of the A register data relative to the fixed reference word in the R latch. The digital summer is internally partitioned into three pipelined stages. Therefore, a correlation score for a particular alignment of the A register data and the R latch reference appears at the summer output three CLK S cycles later. After an additional output delay of t_{DCOR}, the correlation data is valid at the output pins (IO_{0-6}). If this correlation result is equal to or exceeds the value in the threshold register, then TFLG goes HIGH. TFLG is valid t_{DF} after the third rising edge of CLK S.

Threshold Register Load

The timing sequence for loading the threshold (T) register is shown in the Timing Diagrams. The T register holds the 7-bit threshold value to be compared with each correlation result. The rising edge of CLK T loads the data present on the IO_{0-6} pins into the T register. T flag logic is pipelined 3 stages, with the summer. The new value loaded into the threshold register will affect the TFLG on the third CLK S (plus an output delay t_{DF}) following the T register load.

The output buffers must be in a high-impedance state (disabled) when the T register is programmed from an external source. After a delay of t_{DIS} from the time TS goes HIGH, the output buffers are disabled. The data pins IO_{0-6} may then be driven externally with the new threshold data. The data must be present for a setup time of t_{SCOR} before

and t_H after the rising edge of CLK T for correct operation. The minimum LOW and HIGH level pulse widths for CLK T are shown below as t_{PWL} and t_{PWH} respectively.

After TS is set LOW, there is an enable delay of t_{ENA} before the internal correlation data is available at pins IO_{0-6}.

Invert Control Timing

Most applications will tie the INVERT control HIGH or LOW depending on system requirements. In the few situations in which the control is used dynamically, the user must observe special timing constraints.

Because INVERT governs logic located between the master and slave latches of the data output register, its setup and hold requirements differ from those of the data and other controls. The device will respond to changes on INV whenever CLOCK is HIGH and will ignore it when CLOCK is LOW. To minimize the data output delay and to avoid inducing errors, the user should observe the following timing constraints:

1. Set INVERT to the desired state for the next output on or before the rising edge of CLOCK. If INVERT is asserted a few nanoseconds after the rising edge, the data output may be similarly delayed.

2. More importantly, keep INVERT in the desired state until after the falling edge of CLOCK, to avoid corrupting the output data. If INVERT is changed several nanoseconds before the falling edge of CLOCK, the data will likewise change. If it is changed just before the falling edge, an indeterminate output may result.

Mask Register

In addition to the A and B shift references, the TMC2023 has another independently clocked register: the M, or mask register. The M register functions identically to the A and B register, except that its parallel outputs are ANDed with the exclusive-ORed outputs from the A register and R latch.

Many uses of the TMC2023 digital correlator require disabling the correlation between certain bit positions (A_i and R_i) of input words A and R. While correlation data is being clocked into the A and/or B register, a mask word may be entered into the M register. Where no comparison is to be made, zeroes are entered in those M register positions. The exclusive-OR result between each bit position is ANDed with a bit from the M register. Thus, if a particular mask bit (M_i) is zero, the output correlation between A and B for that bit position will be disabled. Consequently, a zero correlation is presented to the digital summer for each masked bit position.

The Mask register is useful for changing correlation word length and location within the registers. Where a word is undefined or no correlation is to take place, the M register should contain a zero. Conversely, it must be loaded with a one in each position where correlation is desired

The M register is useful for building logic functions. Note that for each bit A_i and R_i, the correlation logic is:

$$A_i + R_i = A_i \overline{R_i} + \overline{A_i} R_i \text{ } (A_i \text{ exclusive-OR } R_i)$$

This result is complemented at the input of the AND gates and ANDed with the mask bit (M_i) resulting in:

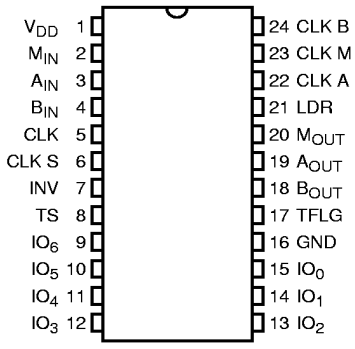
$$\overline{[A_i \overline{R_i} + \overline{A_i} R_i]} * M_i$$

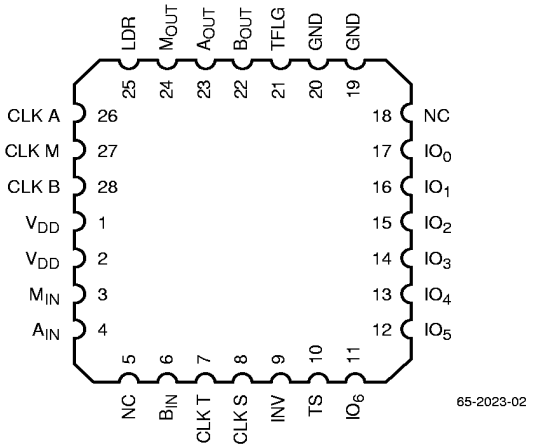
The last step, performed in the digital summer, is to sum the above result over all bit positions simultaneously for a correlation at time n:

$$C(n+3) = \sum_{i=n-63}^{n} [(A_i \text{ XNOR } B_i) \text{AND } M_i]$$

where i = 1, 2, 3... and n = correlation word length

Pin Assignments





Pin Descriptions

Pin Name	J2, J7 Package	C3, R3 Package	Function
Power			
GND	16	19, 20	Ground
V_{DD}	1	1, 2	**Supply Voltage.** The TMC2023 operates from a single +5V supply. All V_{DD} and GND pins must be connected.
Control			
INV			**Inverter Output.** Control that inverts the 7-bit digital output. When a HIGH level is applied to this pin, the outputs IO_{0-6} are logically inverted. See the Timing Diagrams for setup and hold requirements.
TS		10	**Three-State Enable.** The three-state control enables and disables the output buffers. A HIGH level applied to this pin forces outputs into the high impedance state. This control also allows loading of the internal threshold register.
LDR	21	25	**Load Reference.** Control that allows parallel data to be loaded from the B register into the reference latch for correlation. If LDR is held HIGH, the R latch is transparent.
Clocks			
CLK A	22	26	**A Register Clock.** Input clocks. Clock input pins for the A register. Each register may be independently clocked.
CLK M	23	27	**M Register Clock.** Input clocks. Clock input pins for the M register. Each register may be independently clocked.
CLK B	24	28	**B Register Clock.** Input clocks. Clock input pins for the B register. Each register may be independently clocked.
CLK T	5	7	**Threshold Register.** Threshold register clock. Clock input used to load the T register.
CLK S	6	8	**Digital Summer Clock.** Clock input that allows independent clocking of the pipelined summer network.
Inputs			
M_{IN}	2	3	**Mask Register.** Mask register input. Allows the user to choose “no-compare” bit positions. A “0” in any bit location will result in a no-compare state for that location (bit position masked).
A_{IN}		4	**Shift Register.** Shift register inputs to the A 64-bit serial register.
B_{IN}		6	**Shift Register.** Shift register inputs to the B 64-bit serial register.
Outputs			
IO_{6-0}	9,10,11, 12,13, 14,15	11,12, 13,14, 15,16,17	**Correlation Score.** Bidirectional data pins. When outputs are enabled (TS LOW), data is a 7-bit binary representation of the correlation between the unmasked portions of the R latch and the A register. IO_6 is the MSB. These pins also serve as parallel inputs to load the threshold register. Data present one setup time before CLK T goes HIGH will be latched into the threshold register.
TFLG	17	21	**Threshold Flag.** The TFLG output goes HIGH whenever the correlation score is equal to or greater than the number loaded into the T register (0 to 64).
B_{OUT}	18	22	**Shift Register B.** Outputs of shift registers B, A, and M, respectively. These may be used to cascade multiple devices.
A_{OUT}	23	19	**Shift Register A.**
M_{OUT}	24	20	**Shift Register M.**
No Connect			
NC	None	5,18	**No Connect.** These pins should be left unconnected.

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min.	Typ.	Max.	Units
Power Supply Voltage	-0.5		+7.0	V
Input Voltage	-0.5		V_{DD}+0.5	V
Outputs				
Applied Voltage[2]	-0.5		V_{DD}+0.5	V
Forced Current[3,4]	-3.0		6.0	mA
Short Circuit Duration				
(Single output in HIGH state to GND)			1 second	
Temperature				
Operating, Case	-60		+130	°C
Operating, Junction			+175	°C
Lead, Soldering (10 seconds)			+300	°C
Storage	-65		+150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

Operating Conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min.	Nom.	Max.	Min.	Nom.	Max.	
V_{DD}	Power Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	Volts
t_{PWL}	Clock Pulse Width, LOW							
	TMC2023	15			15			ns
	TMC2023-1, -2	12			14			ns
	TMC2023-3	8			10			ns
t_{PWH}	Clock Pulse Width, HIGH							
	TMC2023	15			15			ns
	TMC2023-1, -2	12			14			ns
	TMC2023-3	8			8			ns
t_{SCOR}	Data Setup Time, Correlator							
	TMC2023	12			14			ns
	TMC2023-1, -2	10			10			ns
	TMC2023-3	9			10			ns
t_{SSR}	Data Setup Time, Shift Register (A_{IN}, B_{IN}, M_{IN})							
	TMC2023	12			13			ns
	TMC2023-1, -2	8			10			ns
	TMC2023-3	7			9			ns

Operating Conditions (continued)

Parameter		Temperature Range						Units
		Standard			Extended			
		Min.	Nom.	Max.	Min.	Nom.	Max.	
t_H	Data Input Hold Time, Correlator and Shift Register							
	All grades	0			0			ns
f_{CLK}	CLK Frequency, Correlator, Shift Register and Flag Sections							
	TMC2023			25			25	MHz
	TMC2023-1			30			30	MHz
	TMC2023-2			35			35	MHz
	TMC2023-3			50			50	MHz
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
V_{IHC}	Input Voltage, Logic HIGH, A,B,M,S CLKS	2.0			2.4			V
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
I_{OH}	Output Current, Logic HIGH			-2.0			-2.0	mA
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				-55		125	°C

Electrical Characteristics

Parameter		Conditions	Temperature Range				
			Standard		Extended		
			Min.	Max.	Min.	Max.	Units
I_{DDQ}	Power Supply Current, Quiescent	V_{DD} = Max, V_{IN} = LOW, T_S = HIGH		5		10	mA
I_{DDU}	Power Supply Current, Unloaded	V_{DD} = Max, T_S = HIGH					
		TMC2023, f_{CLK} = 25 MHz		55		55	mA
		TMC2023-1, f_{CLK} = 30 MHz		75		75	mA
		TMC2023-2, f_{CLK} = 35 MHz		75		75	mA
		TMC2023-3, f_{CLK} = 50 MHz		100		100	mA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		+10		+10	µA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V		-10		-10	µA
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
I_{OZH}	Output Leakage Current, HIGH[1]	V_{DD} = Max, V_{IN} = VDD		+40		+40	µA
I_{OZL}	Output Leakage Current, LOW[1]	V_{DD} = Max, V_{IN} = GND		-40		-40	µA
I_{OS}	Short Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration		-100		-100	mA
C_I	Input Capacitance	T_A = 25°C, f = 1 MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1 MHz		10		10	pF

Note:
1. These values are the I_{IL} and I_{IH} for the T Register.

Switching Characteristics

Parameter		Conditions	Temperature Range				
			Standard		Extended		
			Min.	Max.	Min.	Max.	Units
t_{DCOR}	Output Delay, Correlator	V_{DD} = Min. C_{LOAD} = 40 pF					
	TMC2023			22		22	ns
	TMC2023-1, -2			19		20	ns
	TMC2023-3			17		18	ns
t_{DSR}	Output Delay, Shift Register	V_{DD} = Min. C_{LOAD} = 40 pF					
	TMC2023			22		25	ns
	TMC2023-1, -2			20		22	ns
	TMC2023-3			18		20	ns
t_{DF}	Output Delay, Flags	V_{DD} = Min. C_{LOAD} = 40 pF					
	TMC2023			20		22	ns
	TMC2023-1, -2			17		19	ns
	TMC2023-3			15		17	ns
t_{HO}	Output Hold Time All Grades	V_{DD} = Min. C_{LOAD} = 40 pF		4		4	ns
t_{ENA}	Three-State Output Enable Delay	V_{DD} = Min. C_{LOAD} = 40 pF					
	TMC2023			20		25	ns
	TMC2023-1, -2			16		20	ns
	TMC2023-3			15		18	ns
t_{DIS}	Three-State Output Disable Delay	V_{DD} = Min. C_{LOAD} = 40 pF					
	TMC2023			20		24	ns
	TMC2023-1, -2			16		18	ns
	TMC2023-3			14		16	ns

Application Notes

The TMC2023 can be cascaded to implement correlations of more than 64 bits. Typically, all clocks are tied together and the A, B, and M outputs of preceding stages are connected to the respective inputs of subsequent stages. An external summer is required to generate the composite correlation score. Use of the T register and TFLG require additional hardware for this configuration. The TMC2221 correlator provides 128 taps.

When comparing a multi-bit word to a single-bit reference, the outputs from the individual correlators must be appropriately weighted. This weighting reflects the relative importance of the different bit positions. Normally simple shifts division by 2, 4, 8… provide the required weighting. The TMC2220 correlator provides 32-tap 4x1 correlation.

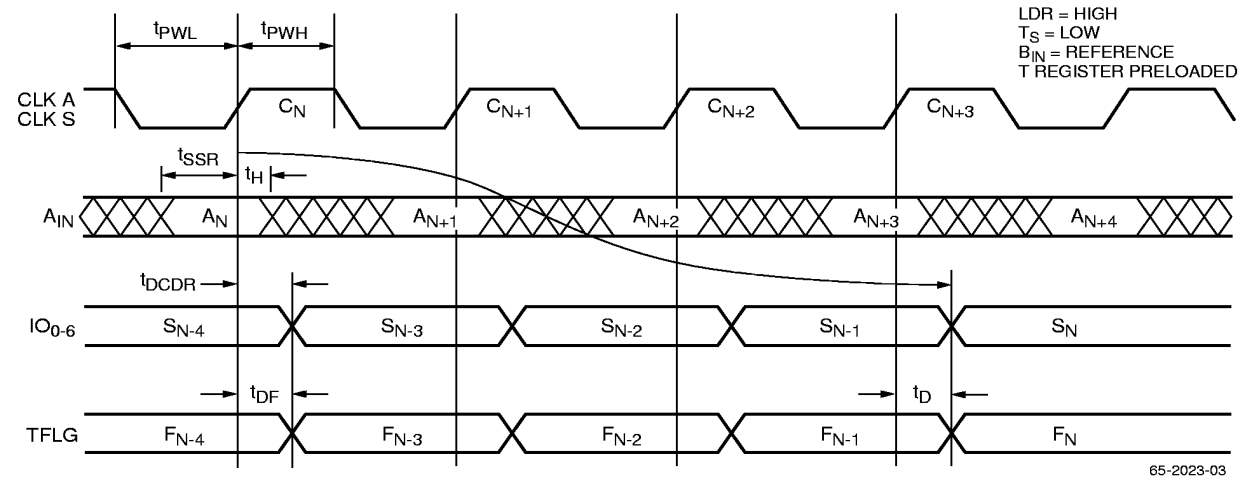


Figure 1. Continuous Correlation

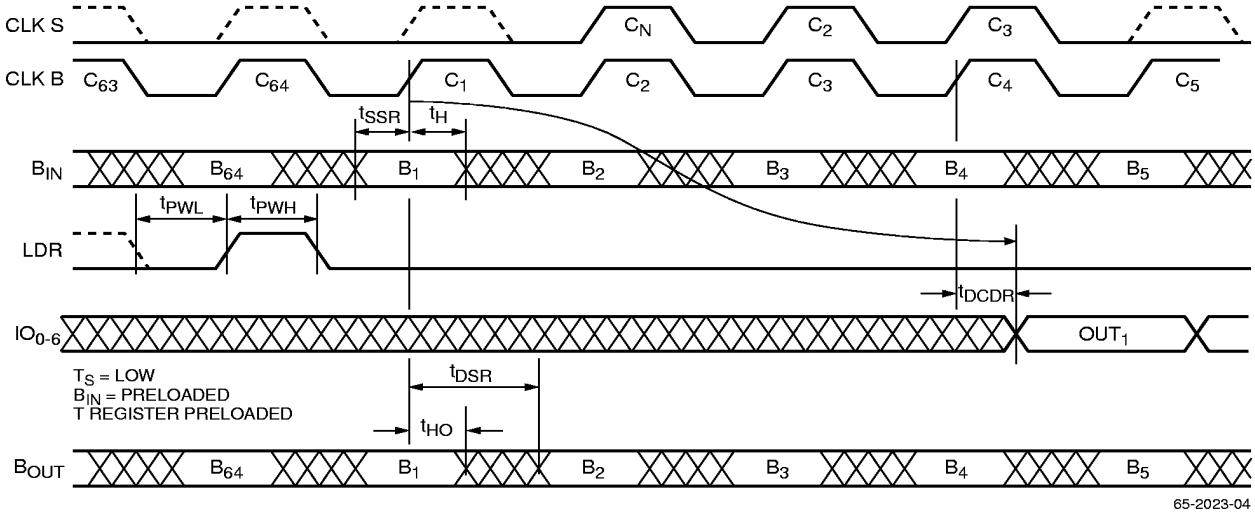


Figure 2. Cross-Correlation

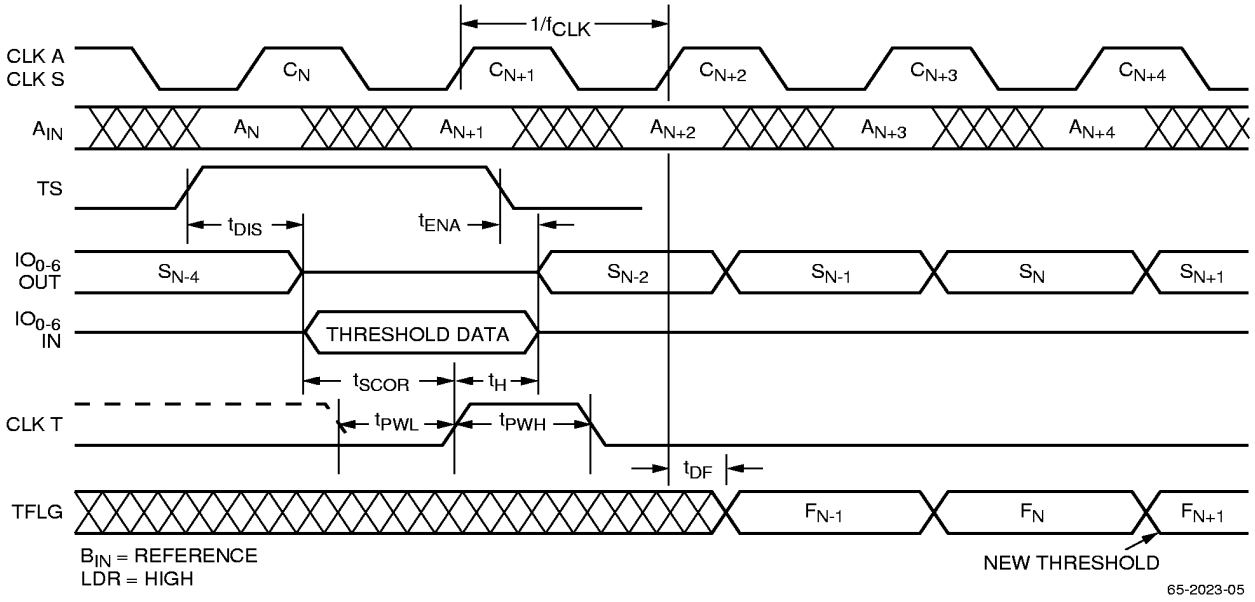


Figure 3. Threshold Register Loading

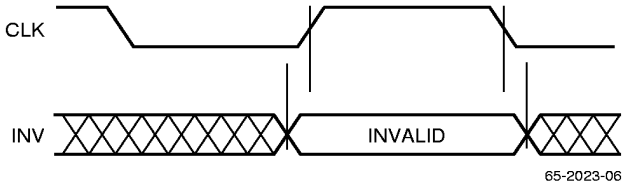


Figure 4. Invert Control Timing

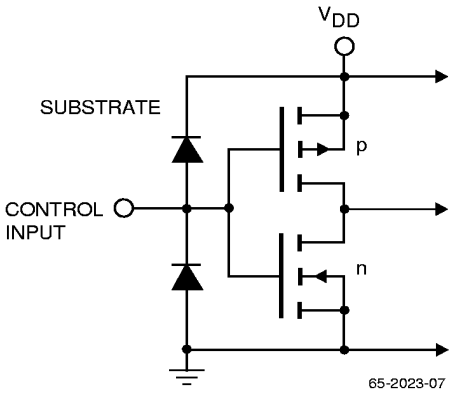


Figure 5. Equivalent Input Circuit

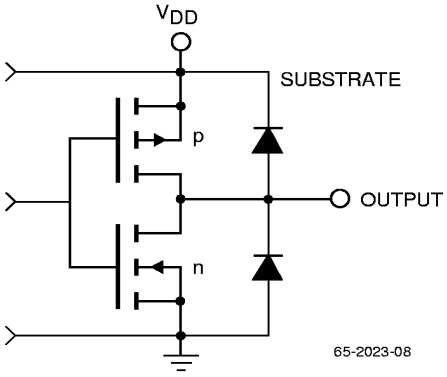


Figure 6. Equivalent Output Circuit

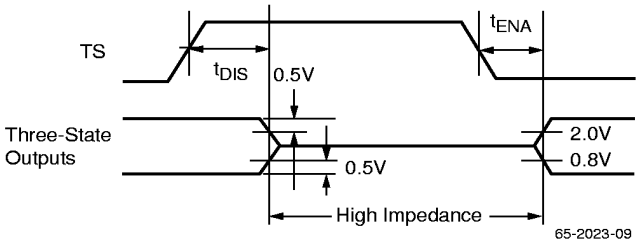


Figure 7. Threshold Levels for Three-State Measurements

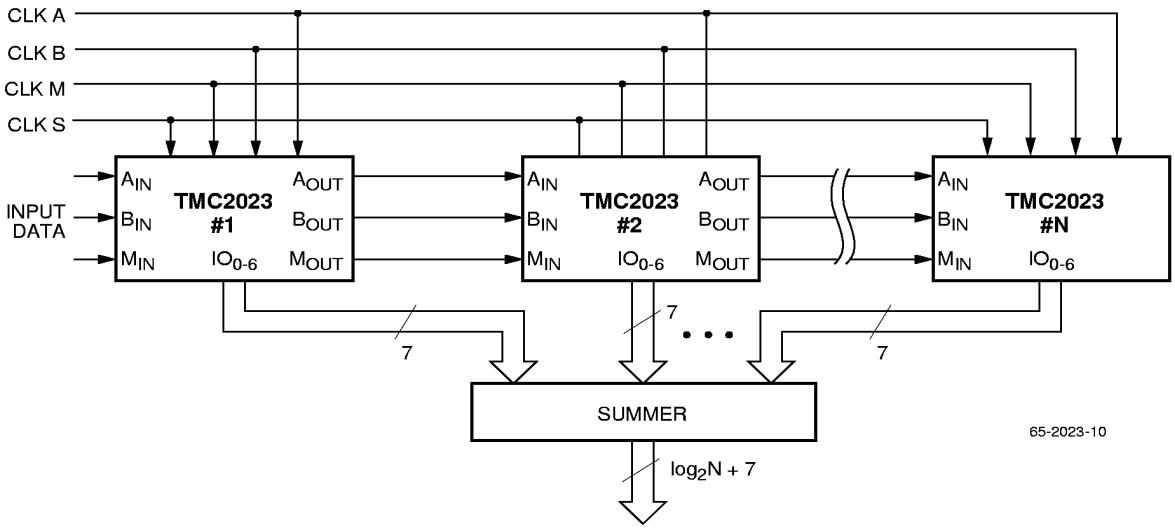


Figure 8. Cascading for Extended-Length Correlation

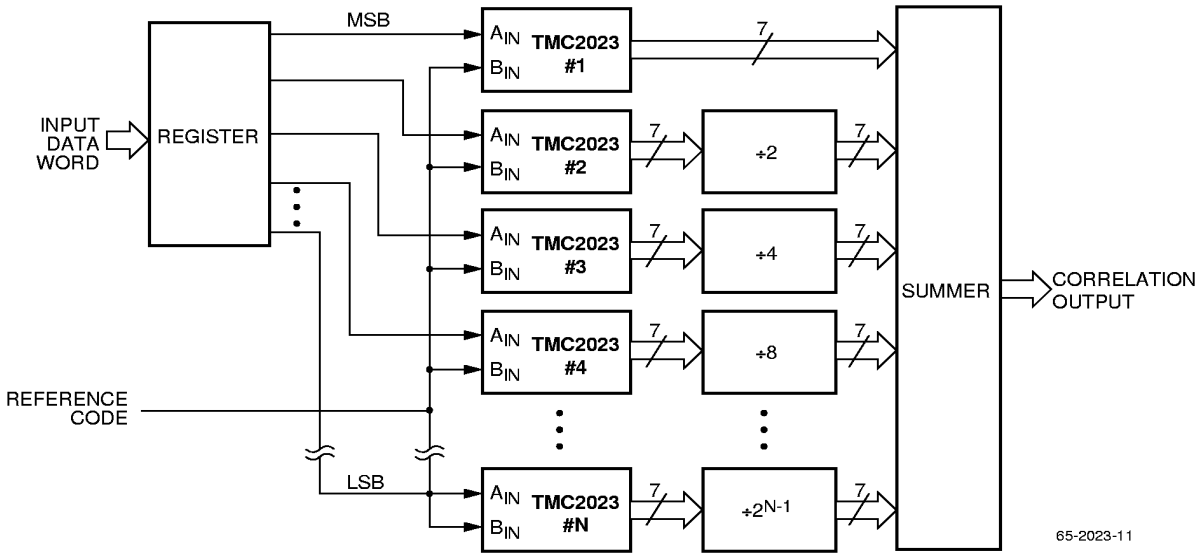


Figure 9. Multi-Bit x 1-Bit Correlation

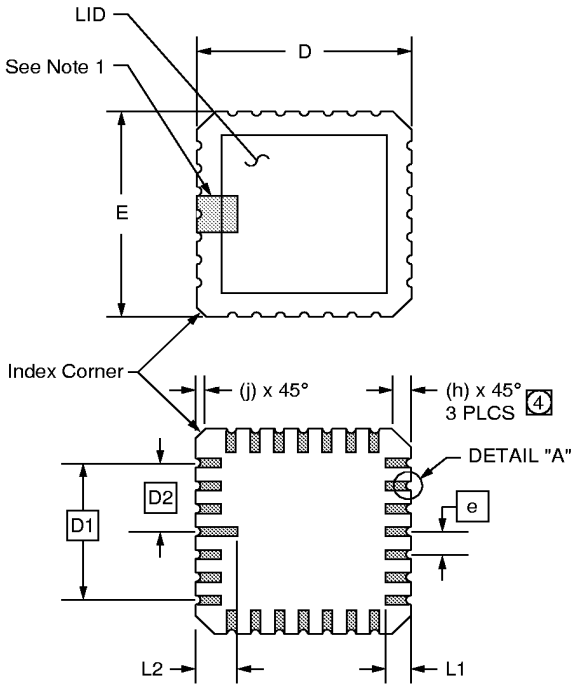
Mechanical Dimensions

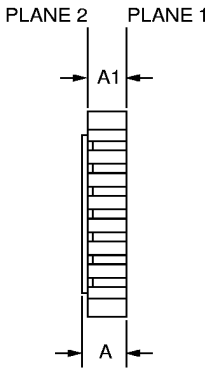
28-Lead LCC Package

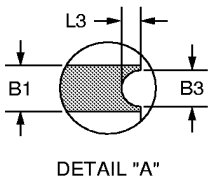
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.060	.100	1.52	2.54	3, 6
A1	.050	.088	1.27	2.24	3, 6
B1	.022	.028	.56	.71	2
B3	.006	.022	.15	.56	2, 5
D/E	.442	.460	11.23	11.68	
D1/E1	.300 BSC		7.62 BSC		
D2/E2	.150 BSC		3.81 BSC		
e	.050 BSC		1.27 BSC		
h	.040 REF		1.02 REF		4
j	.020 REF		.51 REF		4
L1	.045	.055	1.14	1.40	
L2	.075	.095	1.91	2.41	
L3	.003	.015	.08	.38	5
ND/NE	7		7		
N	28		28		

Notes:

1. The index feature for terminal 1 identification, optical orientation or handling purposes, shall be within the shaded index areas shown on planes 1 and 2. Plane 1 terminal 1 identification may be an extension of the length of the metallized terminal which shall not be wider than the B1 dimension.
2. Unless otherwise specified, a minimum clearance of .015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.).
3. Dimension "A" controls the overall package thickness. The maximum "A" dimension is the package height before being solder dipped.
4. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing. The index corner shall be clearly unique.
5. Dimension "B3" minimum and "L3" minimum and the appropriately derived castellation length define an unobstructed three dimensional space traversing all of the ceramic layers in which a castellation was designed. Dimension "B3" maximum and "L3" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dripping.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.







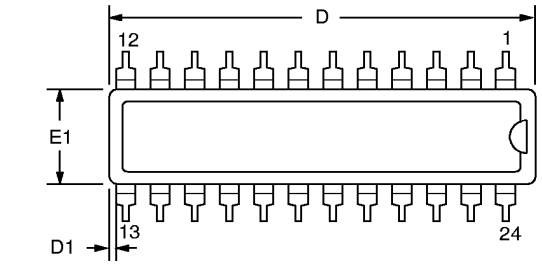
Mechanical Dimensions (continued)

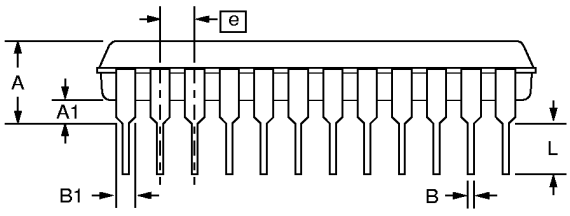
24-Lead Plastic DIP .300" Package

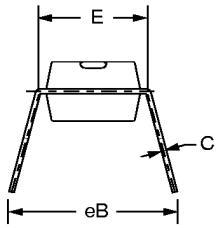
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.53	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	1.125	1.275	28.58	32.39	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	24		24		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







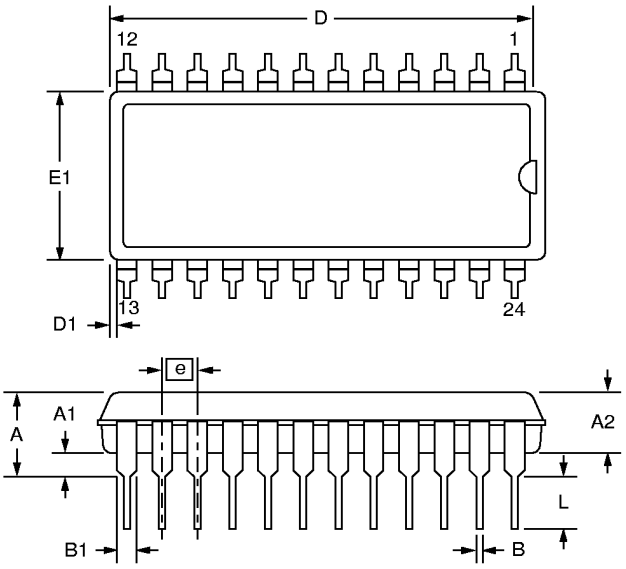
Mechanical Dimensions (continued)

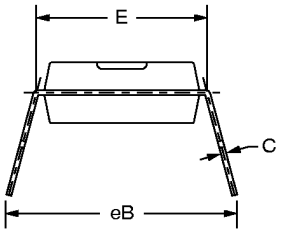
24-Lead Plastic DIP .600" Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.250	—	6.35	
A1	.015	—	.38	—	
A2	.125	.195	3.18	4.95	
B	.014	.022	.36	.56	
B1	.030	.070	.76	1.78	
C	.008	.015	.20	.38	4
D	1.150	1.290	29.21	32.77	2
D1	.005	—	.13	—	
E	.600	.625	15.24	15.88	
E1	.485	.580	12.32	14.73	2
e	.100 BSC		2.54 BSC		
eB	—	.700	—	17.78	
L	.115	.200	2.92	5.08	
N	24		24		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.





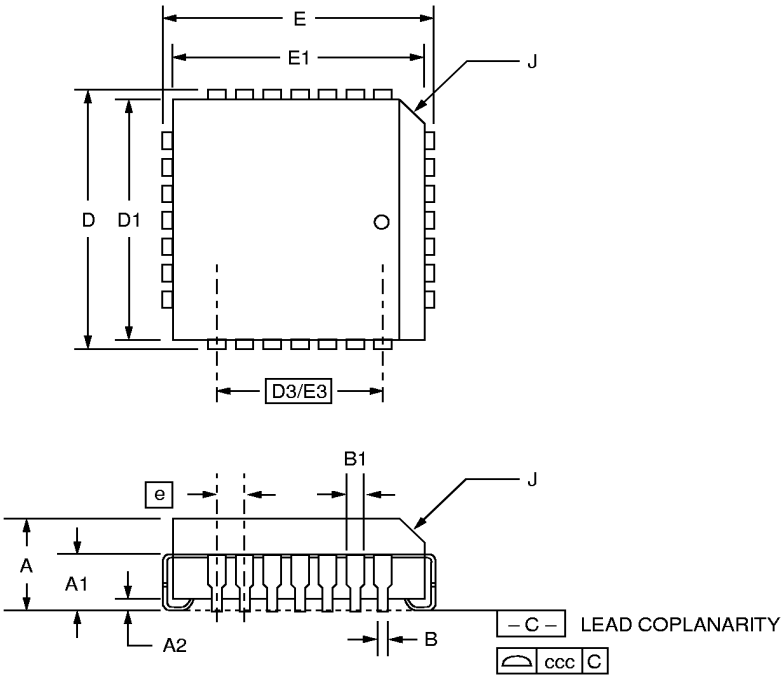
Mechanical Dimensions (continued)

28-Lead PLCC Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	3
D3/E3	.300 BSC		7.62 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	2
ND/NE	7		7		
N	28		28		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Corner and edge chamfer (J) = 45°.
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm).



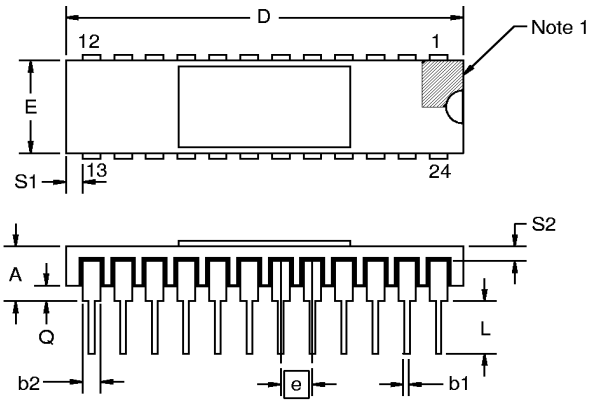
Mechanical Dimensions (continued)

24-Lead Side Brazed DIP Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.120	.175	3.05	4.44	
b1	.014	.023	.36	.58	7
b2	.040	.065	1.02	1.65	2
c1	.008	.015	.20	.38	7
D	1.180	1.220	29.97	30.99	
E	.575	.610	14.60	15.49	
e	.100 BSC		2.54 BSC		4, 8
eA	.600 BSC		15.24 BSC		6
L	.125	.200	3.18	5.08	
Q	.025	.060	0.63	1.52	3
S1	.005	—	0.13	—	5
S2	.005	—	0.13	—	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 12, 13, and 24 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 24.
5. Applies to all four corners (leads number 1, 12, 13, and 24).
6. "eA" shall be measured at the centerline of the leads.
7. All leads - Increase maximum limit by .003(.08mm) measured at the center of the flat when lead finish is applied.
8. Twenty-two spaces.



Standard Military Drawing

These devices are also available as products manufactured, tested, and screened in compliance with Standard Military Drawings (SMD). The nearest vendor equivalent product is shown in the table; however, the applicable SMD is the sole controlling document defining the SMD product.

SMD	Product Number	Speed	Package
5962-89711 01JA	TMC2023J7V	25MHz	24 Pin Side Brazed DIP 0.6" Wide
5962-89711 02JA	TMC2023J7V1	30MHz	24 Pin Side Brazed DIP 0.6" Wide
5962-89711 01LA	TMC2023J2V	25MHz	24 Pin Side Brazed DIP 0.3" Wide
5962-89711 02LA	TMC2023J2V1	30MHz	24 Pin Side Brazed DIP 0.3" Wide
5962-89711 013A	TMC2023C3V	25MHz	28 Contact Chip Carrier
5962-89711 023A	TMC2023C3V1	30MHz	28 Contact Chip Carrier

Ordering Information

Product Number	fCLK (MHz)	Temperature	Screening	Package	Package Marking
TMC2023N2C	25	STD: T_A = 0 to 70°C	Commercial	24-pin 0.3" Plastic DIP	2023J2C
TMC2023N2C1	30	STD: T_A = 0 to 70°C	Commercial	24-pin 0.3" Plastic DIP	2023J2C1
TMC2023N2C2	35	STD: T_A = 0 to 70°C	Commercial	24-pin 0.3" Plastic DIP	2023J2C2
TMC2023N2C3	50	STD: T_A = 0 to 70°C	Commercial	24-pin 0.3" Plastic DIP	2023J2C3
TMC2023J2V	25	EXT: T_C = -55 to 125°C	MIL-STD-883	24-pin 0.3" Ceramic Side Brazed DIP	2023J2V
TMC2023J2V1	30	EXT: T_C = -55 to 125°C	MIL-STD-883	24-pin 0.3" Ceramic Side Brazed DIP	2023J2V1
TMC2023J2V2	35	EXT: T_C = -55 to 125°C	MIL-STD-883	24-pin 0.3" Ceramic Side Brazed DIP	2023J2V2
TMC2023J2V3	50	EXT: T_C = -55 to 125°C	MIL-STD-883	24-pin 0.3" Ceramic Side Brazed DIP	2023J2V3
TMC2023N7C	25	STD: T_A = 0 to 70°C	Commercial	24-pin 0.6" Plastic DIP	2023N7C
TMC2023N7C1	30	STD: T_A = 0 to 70°C	Commercial	24-pin 0.6" Plastic DIP	2023N7C1
TMC2023N7C2	35	STD: T_A = 0 to 70°C	Commercial	24-pin 0.6" Plastic DIP	2023N7C2
TMC2023N7C3	50	STD: T_A = 0 to 70°C	Commercial	24-pin 0.6" Plastic DIP	2023N7C3
TMC2023J7V	25	EXT: T_C = -55 to 125°C	MIL-STD-883	24-pin 0.6" Ceramic Side Brazed DIP	2023J7V
TMC2023J7V1	30	EXT: T_C = -55 to 125°C	MIL-STD-883	24-pin 0.6" Ceramic Side Brazed DIP	2023J7V1
TMC2023J7V2	35	EXT: T_C = -55 to 125°C	MIL-STD-883	24-pin 0.6" Ceramic Side Brazed DIP	2023J7V2
TMC2023J7V3	50	EXT: T_C = -55 to 125°C	MIL-STD-883	24-pin 0.6" Ceramic Side Brazed DIP	2023J7V3
TMC2023R3C	25	STD: T_A = 0 to 70°C	Commercial	28 Lead PLCC	2023R3C
TMC2023R3C1	30	STD: T_A = 0 to 70°C	Commercial	28 Lead PLCC	2023R3C1
TMC2023R3C2	35	STD: T_A = 0 to 70°C	Commercial	28 Lead PLCC	2023R3C2
TMC2023R3C3	50	STD: T_A = 0 to 70°C	Commercial	28 Lead PLCC	2023R3C3
TMC2023C3V	25	EXT: T_C = -55 to 125°C	MIL-STD-883	28-Contact Hermetic Ceramic Chip Carrier	2023C3V
TMC2023C3V1	30	EXT: T_C = -55 to 125°C	MIL-STD-883	28-Contact Hermetic Ceramic Chip Carrier	2023C3V1
TMC2023C3V2	35	EXT: T_C = -55 to 125°C	MIL-STD-883	28-Contact Hermetic Ceramic Chip Carrier	2023C3V2
TMC2023C3V3	50	EXT: T_C = -55 to 125°C	MIL-STD-883	28-Contact Hermetic Ceramic Chip Carrier	2023C3V3

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