

DATA SHEET

CBT3857

10-bit bus switch with 10 k Ω pull-down
termination resistors

Product specification
Supersedes data of 1998 Dec 10

1999 Sep 14

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CBT3857

FEATURES

- Enable signal is SSTL_2 compatible
- Optimized for use in Double Data Rate (DDR) SDRAM applications
- Flow-through architecture optimizes PCB layout
- Designed to be used with 200 Mbps
- Switch on resistance is designed to eliminate the need for series resistor to DDR SDRAM
- Internal 10 kΩ pull-down resistors on B port
- Internal 50 kΩ pull-up resistor on output enable input
- Full DDR solution provided when used with SSTL16857 and PCK857
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

DESCRIPTION

This 10-bit bus switch is designed for 3 V to 3.6 V V_{CC} operation and SSTL_2 output enable (\overline{OE}) input levels.

When \overline{OE} is LOW, the 10-bit bus switch is on and port A is connected to port B. When \overline{OE} is HIGH, the switch is open, and a high-impedance state exists between the two ports.

The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The CBT3857 is characterized for operation from 0°C to +85°C.

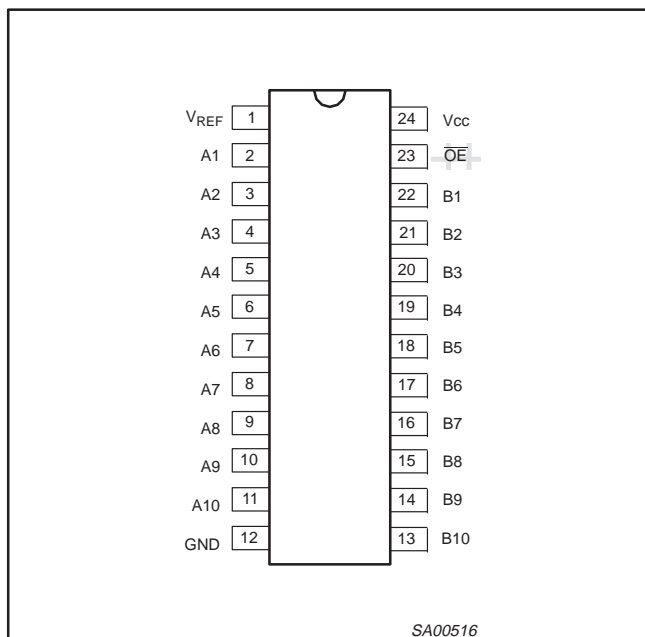
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0 \text{ V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	$C_L = 30 \text{ pF}; V_{CC} = 3.3 \text{ V}$	720	ps
C_{IN}	Input capacitance	$V_I = 0 \text{ V or } V_{CC}$	2.8	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_O = 0 \text{ V or } V_{CC}$	6.4	pF
I_{CCZ}	Total supply current	$V_{CC} = 3.6 \text{ V}$	1	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
24-Pin Plastic TSSOP Type I	0°C to +85°C	CBT3857 PW	SOT355-1

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	V_{REF}	Reference output voltage
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	A1–A10	Inputs
12	GND	Ground (V)
22, 21, 20, 19, 18, 17, 16, 15, 14, 13	B1–B10	Outputs
23	\overline{OE}	Output enable
24	V_{CC}	Positive supply voltage

FUNCTION TABLE

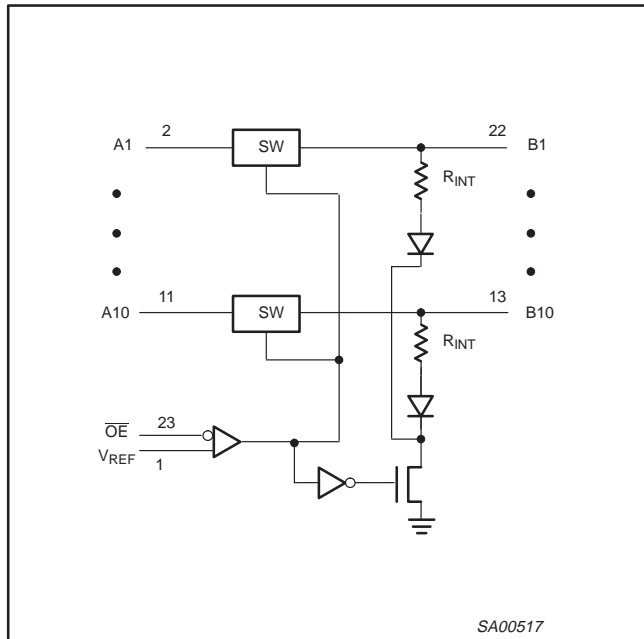
INPUT \overline{OE}	FUNCTION
L	A port = B port
H	Disconnect

H = High voltage level
L = Low voltage level

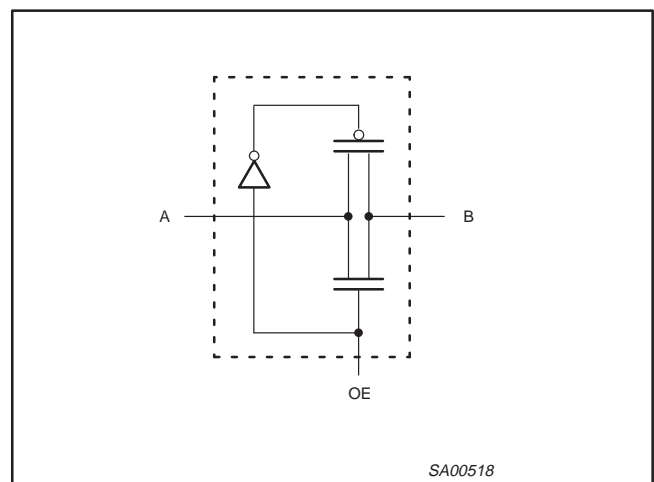
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CBT3857

LOGIC DIAGRAM (POSITIVE LOGIC)



SIMPLIFIED SCHEMATIC, EACH FET SWITCH



ABSOLUTE MAXIMUM RATINGS^{1, 3}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input clamp current	$V_{I/O} < 0$	-50	mA
V_I	DC input voltage range (\overline{OE} only) ²		$V_{CC} + 0.5$	V
T_{stg}	Storage temperature range		-65 to 150	°C
V_I	DC input voltage range (except \overline{OE}) ²		-0.5 to 4.6	V

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- The package thermal impedance is calculated in accordance with JESD 51.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	DC supply voltage	3	3.3	3.6	V
V_{REF}	Reference voltage ($0.38 \times V_{CC}$)	1.15	1.25	1.35	V
V_{IH}	AC high-level input voltage	$V_{REF} + 350 \text{ mV}$			V
V_{IL}	AC low-level Input voltage			$V_{REF} - 350 \text{ mV}$	V
V_{IH}	DC high-level input voltage	$V_{REF} + 180 \text{ mV}$			V
V_{IL}	DC low-level Input voltage			$V_{REF} - 180 \text{ mV}$	V
T_{amb}	Operating free-air temperature range	0		+85	°C

NOTE:

- All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

10-bit bus switch with 10 kΩ pull-down termination resistors

CBT3857

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
			T _{amb} = 0°C to +85°C				
			Min	Typ ¹	Max		
V _{IK}	Input clamp voltage	V _{CC} = 3 V; I _I = -18 mA			-1.2	V	
I _I	Input leakage current	V _{CC} = 3.6 V; V _I = V _{CC} or GND	OE		±0.73	±500	μA
			A Port		±0.1	±1	μA
			B Port		±20	±500	μA
			V _{REF}		±0.1	±1	μA
I _{CC}	Quiescent supply current	V _{CC} = 3.6 V; I _O = 0, V _I = V _{CC} or GND		0.7	1.5	mA	
C _I	Control pins	V _I = 3 V or 0		2.8		pF	
C _{IO(OFF)}	Power-off leakage current	V _O = 3 V or 0; OE = V _{CC}		6.4		pF	
r _{on} ²	On-resistance	V _{CC} = 3 V to 3.6 V; V _A = 0.8 V; V _B = 1.15 V	20	24	30	Ω	
		V _{CC} = 3 V to 3.6 V; V _A = 1.7 V; V _B = 1.35 V	20	24	30		
		V _{CC} = 3 V to 3.6 V; V _I = 1.25 V; I _I = ±10 mA	20	24	30		
r _{off} ²	Off-resistance	V _{CC} = 3 V to 3.6 V; V _I = 1.65 V	1			MΩ	

NOTES:

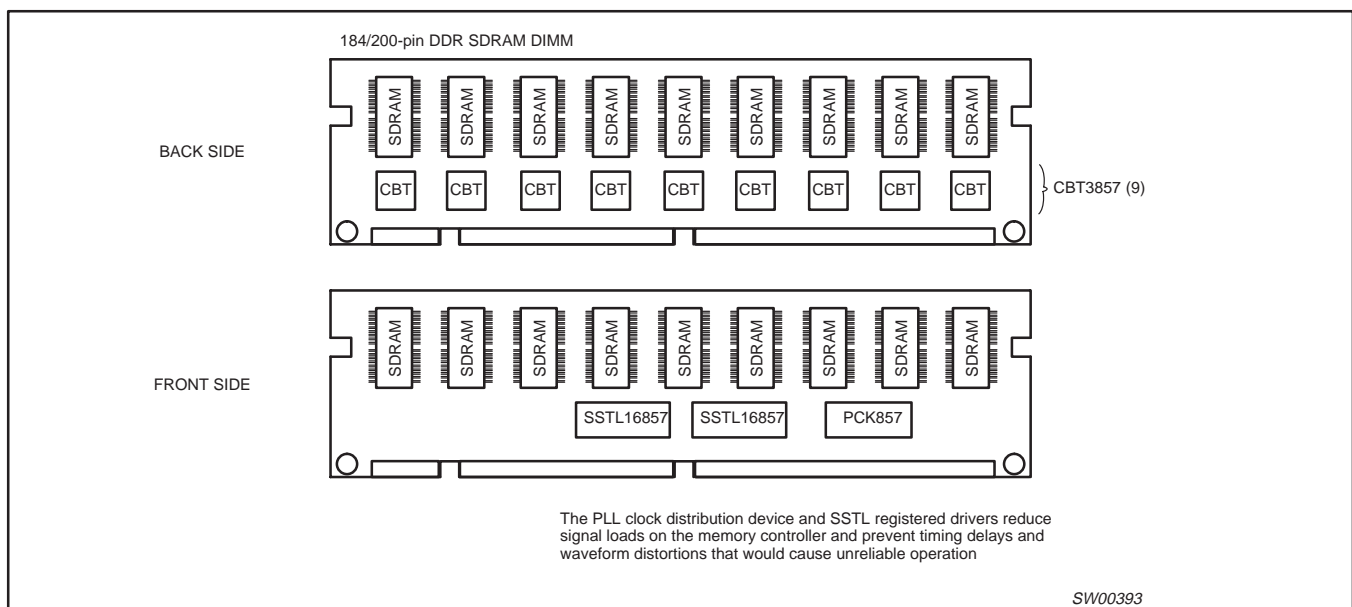
- All typical values are at V_{CC} = 3.3 V, T_{amb} = 25°C
- Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

AC CHARACTERISTICS

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = +3.3 V ±0.3 V		UNIT
				Min	Max	
t _{pd}	Propagation delay ¹	A or B	B or A		750	ps
t _{en}	enable	OE	A or B	1	3	ns
t _{dis}	disable	OE	A or B	1	3	ns

NOTE:

- The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance, when driven by an ideal voltage source (zero output impedance); 24 Ω × 30 pF.

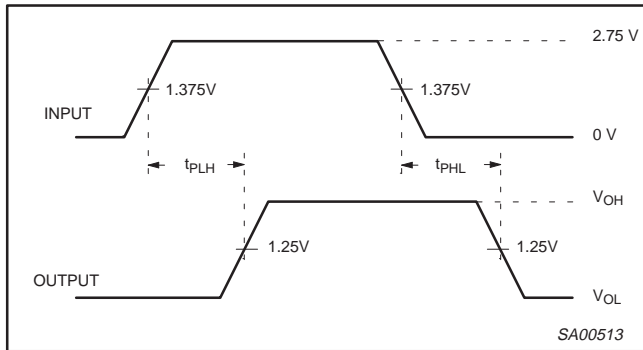


10-bit bus switch with 10 kΩ pull-down termination resistors

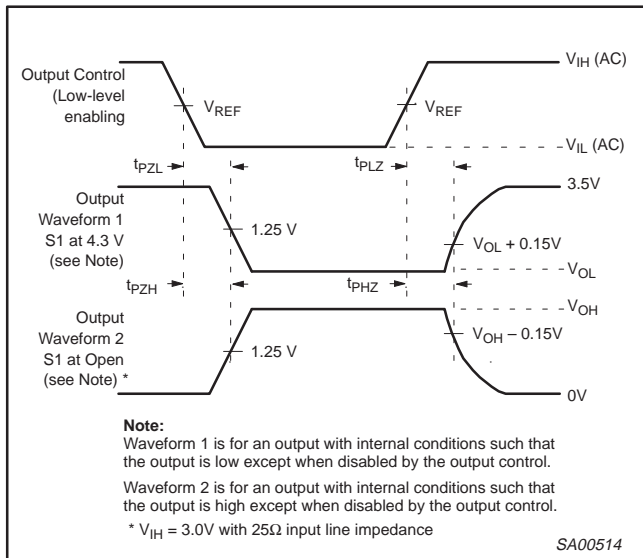
CBT3857

AC WAVEFORMS

$V_M = 1.5\text{ V}$, $V_{IN} = \text{GND to } 3.0\text{ V}$

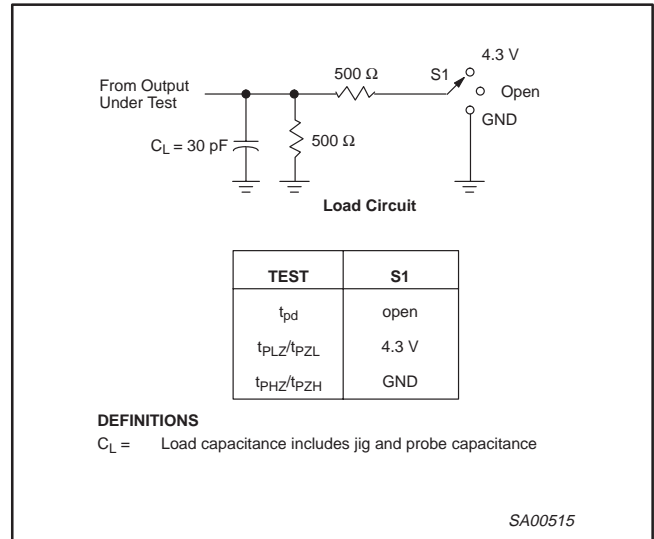


Waveform 1. Input (An) to Output (Yn) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



NOTES:

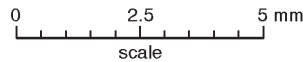
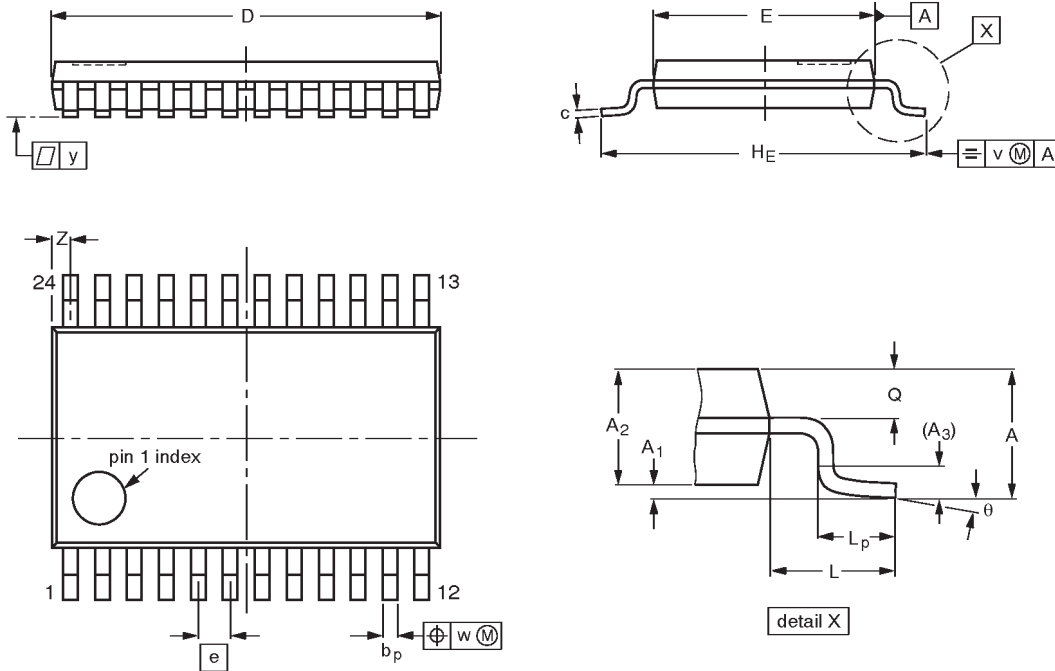
1. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
2. The outputs are measured one at a time with one transition per measurement.

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CBT3857

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				-93-06-16 95-02-04

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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