

# 16K x 16 Reprogrammable PROM

#### **Features**

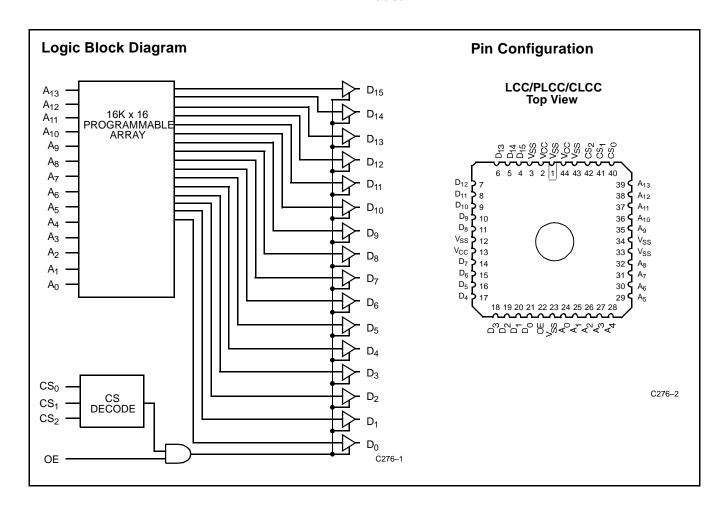
- 0.8-micron CMOS for optimum speed/power
- High speed (for commercial and military)
  - 25-ns access time
- 16-bit-wide words
- . Three programmable chip selects
- · Programmable output enable
- 44-pin PLCC and 44-pin LCC packages
- · 100% reprogrammable in windowed packages
- TTL-compatible I/O
- Capable of withstanding greater than 2001V static discharge

#### **Functional Description**

The CY7C276 is a high-performance 16K-word by 16-bit CMOS PROM. It is available in a 44-pin PLCC/CLCC and a 44-pin LCC packages, and is 100% reprogrammable in windowed packages. The memory cells utilize proven EPROM floating gate technology and word-wide programming algorithms.

The CY7C276 allows the user to independently program the polarity of each chip select (CS<sub>2</sub>–CS<sub>0</sub>). This provides on-chip decoding of up to eight banks of PROM. The polarity of the asynchronous output enable pin (OE) is also programmable.

In order to read the CY7C276, all three chip selects must be active and OE must be asserted. The contents of the memory location addressed by the address lines  $(A_{13}-A_0)$  will become available on the output lines  $(D_{15}-D_0)$ . The data will remain on the outputs until the address changes or the outputs are disabled.





#### **Selection Guide**

		CY7C276-25	CY7C276-30	CY7C276-35
Maximum Access Time (ns)		25	30	35
Maximum Operating	Commercial	175	175	175
Current (mA)	Military	200	200	200

### **Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.) Storage Temperature ......-65°C to+150°C Ambient Temperature with Power Applied......-55°C to+125°C Supply Voltage to Ground Potential .....-0.5V to+7.0V DC Voltage Applied to Outputs in High Z State ......-0.5V to+7.0V DC Input Voltage......-3.0V to +7.0V

DC Program Voltage ......13.0V UV Erasure ......7258 Wsec/cm<sup>2</sup>

Static Discharge Voltage	.>2001V
(per MIL-STD-883, Method 3015)	
Latch-Up Current	>200 mA

# **Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ±10%
Industrial <sup>[1]</sup>	-40°C to +85°C	5V ±10%
Military <sup>[2]</sup>	–55°C to +125°C	5V ±10%

## Electrical Characteristics<sup>[3, 4]</sup>

				CY7C276-25 CY7C276-30 CY7C276-35		
Parameter	Description	Test Conditions		Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	$V_{CC} = Min., I_{OH} = -2.0 \text{ mA}$		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA (6.0 mA Mil)			0.4	V
V <sub>IH</sub>	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for A	2.0	V <sub>CC</sub>	V	
V <sub>IL</sub>	Input LOW Level	Guaranteed Input Logical LOW Voltage for A	-3.0	0.8	V	
I <sub>IX</sub>	Input Leakage Current	$GND \le V_{IN} \le V_{CC}$		-10	+10	μΑ
V <sub>CD</sub>	Input Clamp Diode Voltage			Not	te 3	μΑ
I <sub>OZ</sub>	Output Leakage Current	$V_{CC} = Max., V_{OL} \le V_{OUT} \le V_{OH},$ Output Disabled		-40	+40	μΑ
los	Output Short Circuit Current	$V_{CC} = Max., V_{OUT} = 0.0V^{[5]}$		-20	-90	mA
Icc	Power Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0.0 mA Com'l			175	mA
			Military		200	mA

## Capacitance<sup>[3]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	$T_A = 25^{\circ}C, f = 1 \text{ MHz},$	10	pF
C <sub>OUT</sub>	Output Capacitance	$V_{CC} = 5.0V$	10	pF

#### Notes:

- Contact a Cypress representative for industrial temperature range specifications.

  T<sub>A</sub> is the "instant on" case temperature

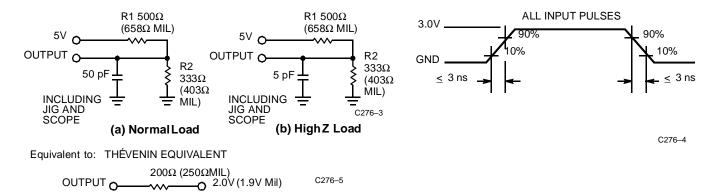
  See Introduction to CMOS PROMs in this Data Book for general information on testing.

  See the last page of this specification for Group A subgroup testing information.

  For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.



#### **AC Test Loads and Waveforms**



# Switching Characteristics Over the Operating Range<sup>[3,4]</sup>

		CY7C	276-25	CY7C	276-30	CY7C	276-35	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t <sub>AA</sub>	Address to Output Data Valid		25		30		35	ns
t <sub>CSOV</sub>	CS Active to Output Valid		13		15		18	ns
t <sub>CSOZ</sub>	CS Inactive to High Z Output		13		15		18	ns
t <sub>OEV</sub>	OE Active to Output Valid		11		12		15	ns
t <sub>OEZ</sub>	OE Inactive to High Z Output		11		12		15	ns

## **Erasure Characteristics**

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm2. For an ultraviolet lamp with a 12 mW/cm² power rating the exposure time would be approximately 35 minutes. The 7C276 needs to be within 1 inch of the lamp during erasure. Permanent dam-

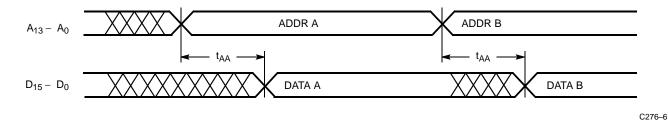
age may result if the EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm<sup>2</sup> is the recommended maximum dosage.

Wavelengths of light less than 4000 Angstroms begin to erase the 7C276 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

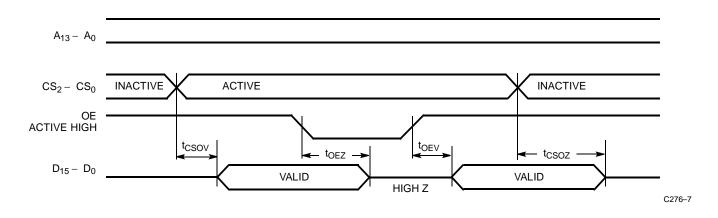


## **Switching Waveforms**

## Read Operation Timing Diagram [6]



## **Chip Select and Output Enable Timing Diagrams**



#### Notes:

6.  $CS_2 - CS_0$ , OE assumed active.

#### **Architecture Configuration Bits**

The CY7C276 has four user-programmable options in addition to the reprogrammable data array. For detailed programming information contact your local Cypress representative.

The programmable options determine the active polarity for the three chip selects (CS2 - CS0) and OE. When these control bits are programmed with a 0 the inputs are active LOW. When these control bits are programmed with a 1 the inputs are active HIGH.

### **Programming Information**

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.



**Table 1. Control Word for Architecture Configuration** 

		Control Word	
<b>Control Option</b>	Bit	Programmed Level	Function
OE	D <sub>0</sub>	0=Default 1=Programmed	OE Active LOW OE Active HIGH
CS <sub>0</sub>	D <sub>12</sub>	0=Default 1=Programmed	CS <sub>0</sub> Active LOW CS <sub>0</sub> Active HIGH
CS <sub>1</sub>	D <sub>13</sub>	0=Default 1=Programmed	CS <sub>1</sub> Active LOW CS <sub>1</sub> Active HIGH
CS <sub>2</sub>	D <sub>14</sub>	0=Default 1=Programmed	CS <sub>2</sub> Active LOW CS <sub>2</sub> Active HIGH

# Bit Map

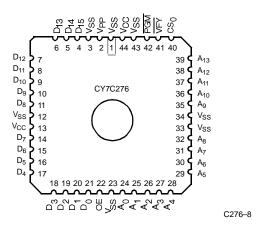
Programmer Address (Hex)	RAM Data
0000	Data
•	
•	•
3FFF	Data
4000	Control Word

Table 2. Program Mode Table

Mode	V <sub>PP</sub>	PGM	VFY	$D_0-D_{15}$
Program Inhibit	$V_{PP}$	$V_{IHP}$	$V_{IHP}$	High Z
Program Enable	$V_{PP}$	$V_{ILP}$	$V_{IHP}$	Data
Program Verify	V <sub>PP</sub>	$V_{IHP}$	$V_{\rm ILP}$	Data

**Table 3. Configuration Mode Table** 

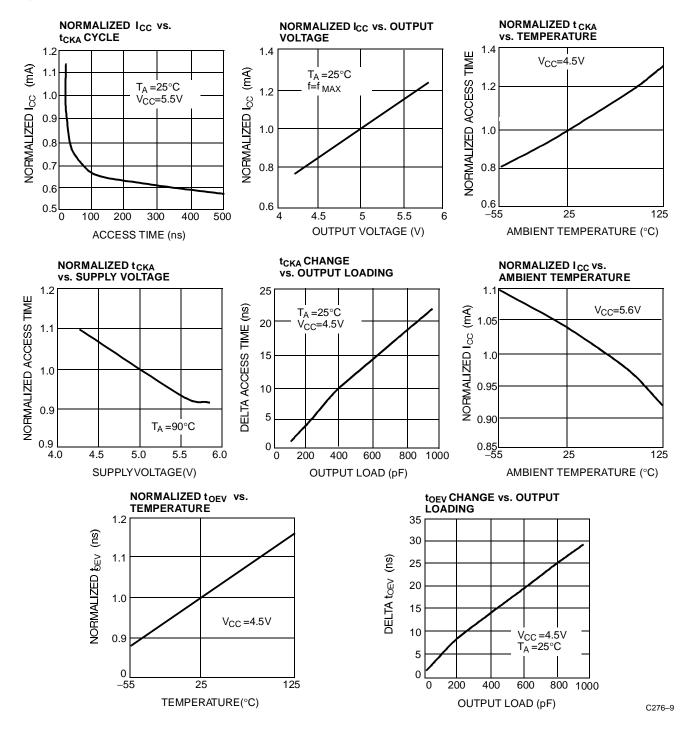
Mode	V <sub>PP</sub>	PGM	VFY	A <sub>2</sub>	D <sub>0</sub> – D <sub>15</sub>
Program Inhibit	$V_{PP}$	V <sub>IHP</sub>	$V_{IHP}$	$V_{PP}$	High Z
Program Control Word	V <sub>PP</sub>	V <sub>ILP</sub>	$V_{IHP}$	V <sub>PP</sub>	Control Word
Verify Control Word	$V_{PP}$	V <sub>IHP</sub>	$V_{ILP}$	$V_{PP}$	Control Word



**Figure 1. Programming Pinout** 



# **Typical DC and AC Characteristics**





# Ordering Information<sup>[7]</sup>

Speed (ns)	Ordering Code	Pack- age Name	Package Type	Operating Range
25	CY7C276-25HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C276-25JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C276-25HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C276-25QMB	Q67	44-Pin Windowed Leadless Chip Carrier	
30	CY7C276-30HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C276-30JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C276-30HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C276-30QMB	Q67	44-Pin Windowed Leadless Chip Carrier	
35	CY7C276-35HC	H67	44-Pin Windowed Leaded Chip Carrier	Commercial
	CY7C276-35JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C276-35HMB	H67	44-Pin Windowed Leaded Chip Carrier	Military
	CY7C276-35QMB	Q67	44-Pin Windowed Leadless Chip Carrier	

#### Notes:

## MILITARY SPECIFICATIONS Group A Subgroup Testing

## **DC Characteristics**

Parameter	Subgroups
V <sub>OH</sub>	1, 2, 3
V <sub>OL</sub>	1, 2, 3
V <sub>IH</sub>	1, 2, 3
V <sub>IL</sub>	1, 2, 3
I <sub>IX</sub>	1, 2, 3
I <sub>OZ</sub>	1, 2, 3
I <sub>CC</sub>	1, 2, 3

# **Switching Characteristics**

Parameter	Subgroups
i ai ailietei	Gubgroups
t <sub>AA</sub>	7, 8, 9, 10, 11
t <sub>CSOV</sub>	7, 8, 9, 10, 11
t <sub>OEV</sub>	7, 8, 9, 10, 11

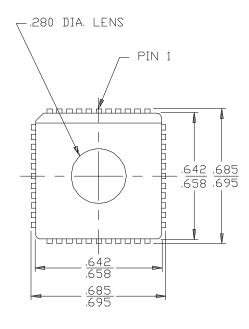
Document #: 38-00183-D

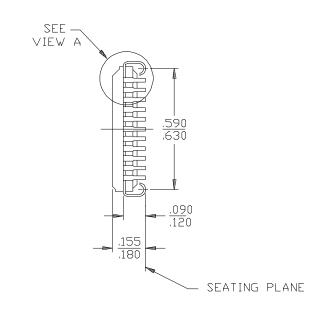
<sup>7.</sup> Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

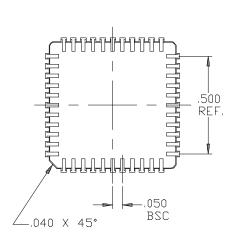


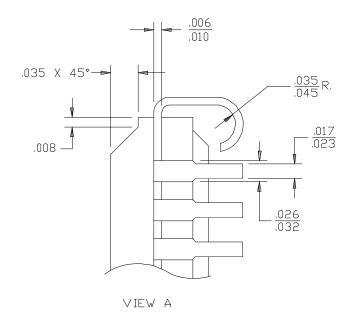
# **Package Diagrams**

### 44-Pin Windowed Leaded Chip Carrier H67





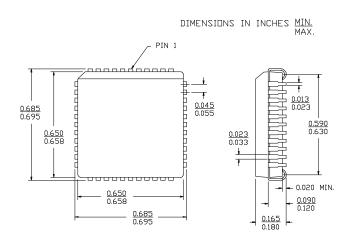




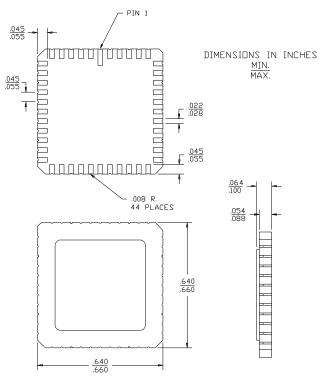


## Package Diagrams (continued)

## 44-Lead Plastic Leaded Chip Carrier J67

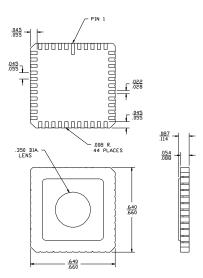


#### 44-Square Leadless Chip Carrier L67 MIL-STD-1835 C-5



#### 44-Pin Windowed Leadless Chip Carrier Q67

#### MIL-STD-1835 C-5



<sup>©</sup> Cypress Semiconductor Corporation, 1993. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress Semiconductor product. Nor does it convey or imply any license under patent or other rights. Cypress Semiconductor does not authorize its products for use as critical components in life-support systems where a malfurnion or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress Semiconductor products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress Semiconductor against all charges.