REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change to table I, parameter t_{PWC}. Removed programming requirements. Editorial changes throughout.	89-09-11	Michael A. Frye
B	Changes in accordance with NOR 5962-R006-91	91-09-24	Michael A. Frye
C	Changes in accordance with NOR 5962-R229-93	93-09-21	Michael A. Frye
D	Drawing updated to reflect current requirements. Removed programming logic from truth table. Editorial changes throughout. - gap	01-01-05	Raymond Monnin
E	5 year review and update. Changed input and output capacitance from 6 pF to 10 pF and 8 pF to 10 pF respectively. ksr	06-06-06	Raymond Monnin

THE FRONT PAGE OF THIS DRAWING HAS BEEN REPLACED

REV																			
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REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

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DRAWING APPROVAL DATE
89-01-13

REVISION LEVEL
E

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 2K X 8 BIT, ONE TIME PROGRAMMABLE (OTP) REGISTERED PROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-88735**

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-88735	01	L	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	7C245	2K X 8-bit registered PROM	45 ns
02	7C245	2K X 8-bit registered PROM	35 ns
03	7C245A	2K X 8-bit registered PROM	35 ns
04	7C245A	2K X 8-bit registered PROM	25 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or CDFP3-F24	24	Flat package
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line package
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs in high Z state	-0.5 V dc to +7.0 V dc
DC program voltage (V_{PP}):	
Device types 01 and 02	14.0 V dc
Device types 03 and 04	13.0 V dc
DC input voltage	-3.0 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Power dissipation (P_D) 2/	1.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J) 3/	+150°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Unless otherwise specified, all voltages are referenced to ground.
2/ Must withstand the added P_D due to short-circuit test; e.g., I_{OS}.
3/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C inspection (see 4.3), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern or similar pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Processing options. Since the PROM is an unprogrammed memory capable of being programmed by either the manufacturer or the user to result in a wide variety of PROM configurations, two processing options are provided for selection in the contract using an altered item drawing.

3.6.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 4.3.1. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.6.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing shall be satisfied by the manufacturer prior to delivery.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.10 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) TA = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input or output capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 4.4). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than four total device failures allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than four total device failures allowable.

e. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} = \le 5.5\ V$ GND = 0 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input leakage current	I_{LI}	V_{IN} = 5.5 V and GND	1, 2, 3	All		±10	µA
Output leakage current 1/	I_{LO}	V_{OUT} = 5.5 V and GND output disabled	1, 2, 3	All		±40	µA
Operating supply current (active)	I_{CC}	$\overline{E}/\overline{E}_S = V_{IL}$, $\overline{INIT} = V_{IH}$ addresses cycling between 0 V and 3 V; $f = \frac{1}{2t_{PWC}}$	1, 2, 3	All		120	mA
Input low voltage 2/	V_{IL}	V_{CC} = 4.5 V and 5.5 V	1, 2, 3	All		0.8	V
Input high voltage 2/	V_{IH}	V_{CC} = 4.5 V and 5.5 V	1, 2, 3	All	2.0		V
Output low voltage	V_{OL}	I_{OL} = 16 mA, V_{CC} = 4.5 V V_{IL} = 0.8 V, V_{IH} = 2.0 V	1, 2, 3	All		0.4	V
Output high voltage	V_{OH}	I_{OH} = -4 mA, V_{CC} = 4.5 V V_{IL} = 0.8 V, V_{IH} = 2.0 V	1, 2, 3	All	2.4		V
Output short circuit Current 3/ 4/	I_{OS}	V_O = GND	1, 2, 3	All	-20	-125	mA
Input capacitance 4/	C_{IN}	V_{IN} = 0 V, V_{CC} = 5.5 V, f = 1.0 MHz, T_C = +25°C, see 4.3.1c	4	All		10	pF
Output capacitance 4/	C_{OUT}	V_{OUT} = 0 V, V_{CC} = 5.5 V, f = 1.0 MHz, T_C = +25°C, see 4.3.1c	4	All		10	pF
Address setup to clock high	t_{SA}	See figures 3 and 4	9, 10, 11	01	45		ns
				02, 03	35		
				04	25		
Address hold from clock high	t_{HA}		9, 10, 11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ GND = 0 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Clock high to valid output	t_{CO}	See figures 3 and 4	9, 10, 11	01		25	ns
				02, 03		15	
				04		12	
Clock pulse width 4/	t_{PWC}		9, 10, 11	01, 02, 03	20		ns
				04	15		
($\overline{E}_S$) Setup to clock high 4/	t_{SES}		9, 10, 11	01, 02, 03	15		ns
				04	12		
($\overline{E}_S$) Hold from clock high 4/	t_{HES}		9, 10, 11	All	5		ns
Delay from $\overline{INIT}$ to valid output 4/	t_{DI}		9, 10, 11	01		35	ns
				02, 03, 04		20	
$\overline{INIT}$ recovery to clock high 4/	t_{RI}		9, 10, 11	01, 02, 03	20		ns
				04	15		
$\overline{INIT}$ pulse width 4/	t_{PWI}		9, 10, 11	01	25		ns
				02, 03	20		
				04	15		
Valid output from clock high 4/, 5/	t_{COS}		9, 10, 11	01		30	ns
				02, 03		20	
				04		15	
Inactive output from clock high 4/, 5/, 6	t_{HZC}		9, 10, 11	01		30	ns
				02, 03		20	
				04		15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ GND = 0 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Valid output from $\overline{E}$ low 4/, 7/	t_{DOE}	See figures 3 and 4	9, 10, 11	01		30	ns
				02, 03		20	
				04		15	
Inactive output from $\overline{E}$ high 4/, 6/, 7/	t_{HZE}		9, 10, 11	01		30	ns
				02, 03		20	
				04		15	

1/ For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.

2/ These are absolute voltages with respect to device ground pin and include all over shoots due to system or tester noise.

3/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

4/ This parameter tested initially and after any design or process changes which may affect this parameter, therefore, shall be guaranteed to the limits specified in table I.

5/ Applies only when the synchronous ($\overline{E}_S$) function is used.

6/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input with loads shown on figure 3, circuit B.

7/ Applies only when the synchronous ($\overline{E}$) function is used.

TABLE II. Electrical test requirements. 1/, 2/, 3/, 4/

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004) for unprogrammed devices	1*, 2, 3, 7*, 8
Final electrical test parameters (method 5004) for programmed devices	1*, 2, 3, 7*, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8

1/ * PDA applies to subgroup 1 and 7.

2/ ** See 4.3.1c.

3/ Any subgroups at the same temperature may be combined when using a multifunction tester.

4/ For all electrical tests, the device shall be programmed to the pattern specified.

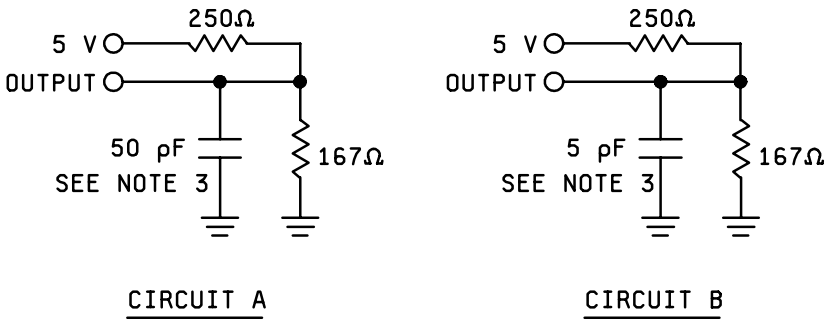
Device types	01 - 04	
Case outlines	K, L	3
Terminal number	Terminal symbol	
1	A_7	NC
2	A_6	A_7
3	A_5	A_6
4	A_4	A_5
5	A_3	A_4
6	A_2	A_3
7	A_1	A_2
8	A_0	A_1
9	0_0	A_0
10	0_1	NC
11	0_2	0_0
12	GND	0_1
13	0_3	0_2
14	0_4	GND
15	0_5	NC
16	0_6	0_3
17	0_7	0_4
18	CP	0_5
19	$\overline{E}/\overline{E}_S$	0_6
20	$\overline{INIT}$	0_7
21	A_{10}	NC
22	A_9	CP
23	A_8	$\overline{E}/\overline{E}_S$
24	V_{CC}	$\overline{INIT}$
25	---	A_{10}
26	---	A_9
27	---	A_8
28	---	V_{CC}

FIGURE 1. Terminal connections.

Pin functions				
Mode	CP	$\overline{E}$ / $\overline{E}_S$	$\overline{INIT}$	Outputs
Read (see notes 2 and 3)	X	V_{IL}	V_{IH}	Data out
Output disable (see note 4)	X	V_{IH}	V_{IH}	High - Z

NOTES:
1. X = Don't care.
2. During read operation, the output latches are loaded on a "0" to "1" transition of CP.
3. In the synchronous mode, pin $\overline{E}_S$ must be low prior to the "0" to "1" transition on CP that loads the register.
4. In the synchronous mode, pin $\overline{E}_S$ must be high prior to the "0" to "1" transition on CP that loads the register.

FIGURE 2. Truth table.



NOTES:
1. Circuit A is for all switching characteristics except t_{HZC} and t_{HZE}.
2. Circuit B is for t_{HZC} and t_{HZE}.
3. Minimum, including jig and scope.

FIGURE 3. Output load circuits.

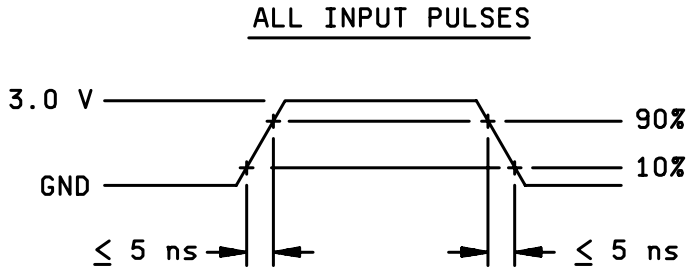
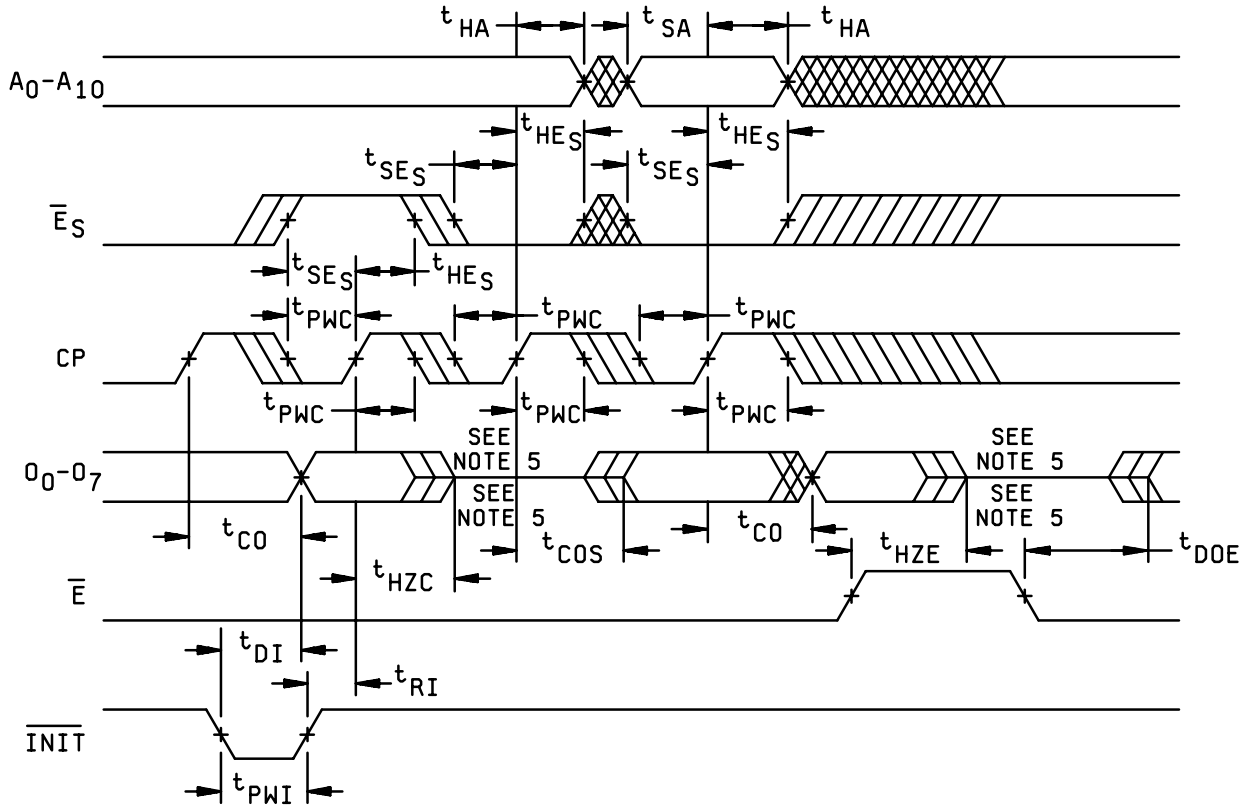


FIGURE 4. Switching waveforms,



NOTES:

1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1 μF or larger capacitor and a 0.01 μF or smaller capacitor, placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any input disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under ac conditions. Large amplitude fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5 V reference levels.
5. Transition is measured at steady-state high level –500 mV or steady-state low level +500 mV on output from the 1.5 V level on inputs with load shown on figure 3.
6. Tests are performed with rise and fall times of 5 ns or less.
7. See above waveform for t_{HZC} and t_{HZE}.
8. All device test loads should be located within two inches of device outputs.

FIGURE 4. Switching waveforms - Continued.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.7 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-06-06

Approved sources of supply for SMD 5962-88735 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8873501KA	3/ 0C7V7 0C7V7	CY7C245-45KMB QP7C245A-45KMB WS57C45-45HMB
5962-8873501LA	3/ 0C7V7 0C7V7	CY7C245-45DMB QP7C245A-45DMB WS57C45-45KMB
5962-88735013A	3/ 0C7V7 0C7V7	CY7C245-45LMB QP7C245A-45LMB WS57C45-45ZMB
5962-88735013C	0C7V7	WS57C45-45ZMB
5962-8873502KA	3/ 0C7V7 0C7V7	CY7C245-35KMB QP7C245A-35KMB WS57C45-35HMB
5962-8873502LA	3/ 0C7V7 0C7V7	CY7C245-35DMB QP7C245A-35DMB WS57C45-35KMB
5962-88735023A	3/ 0C7V7 0C7V7	CY7C245-35LMB QP7C245A-35LMB WS57C45-35ZMB
5962-88735023C	0C7V7	WS57C45-35ZMB
5962-8873503KA	3/ 0C7V7 0C7V7	CY7C245A-35KMB QP7C245A-35KMB WS57C45-35HMB
5962-8873503LA	3/ 0C7V7 0C7V7	CY7C245A-35DMB QP7C245A-35DMB WS57C45-35KMB
5962-88735033A	3/ 0C7V7 0C7V7	CY7C245A-35LMB QP7C245A-35LMB WS57C45-35ZMB
5962-88735033C	0C7V7	WS57C45-35ZMB

See notes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8873504KA	3/ 0C7V7 0C7V7	CY7C245A-25KMB QP7C245A-25KMB WS57C45-25HMB
5962-8873504LA	65786 0C7V7 0C7V7	CY7C245A-25DMB QP7C245A-25DMB WS57C45-25KMB
5962-88735043A	3/ 0C7V7 0C7V7	CY7C245A-25LMB QP7C245A-25LMB WS57C45-25ZMB
5962-88735043C	0C7V7	WS57C45-25ZMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No longer available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051
65786	Cypress Semiconductor Inc. 3901 North First Street San Jose, CA 94134-1506

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