| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Added four device types and updated format. Added two vendors CAGE 1FN41 and 34649. | 91-03-27 | M. A. Frye |
| B | Changes in accordance with NOR 5962-R212-92. | 92-05-15 | M. A. Frye |
| C | Changes in accordance with NOR 5962-R301-92. | 92-09-05 | M. A. Frye |
| D | Changes in accordance with NOR 5962-R227-94. | 94-07-05 | M. A. Frye |
| E | Updated format to include QML vendor paragraphs. ksr | 00-07-24 | Raymond Monnin |
| F | Boilerplate update, part of 5 year review. ksr | 06-05-31 | Raymond Monnin |

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN CHANGED

| | | | | | | | | | | | | | | | | | | | | |
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| REV | | | | | | | | | | | | | | | | | | | | |
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| REV STATUS | | | | REV | | | F | F | F | F | F | F | F | F | F | F | F | F | F | F |
| OF SHEETS | | | | SHEET | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

PREPARED BY
Kenneth Rice

**DEFENSE SUPPLY CENTER COLUMBUS**
**COLUMBUS, OHIO 43218-3990**
**http://www.dscc.dla.mil**

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Raymond Monnin

APPROVED BY
Michael A Frye

DRAWING APPROVAL DATE
26 MAY89

REVISION LEVEL
F

# MICROCIRCUIT, MEMORY, DIGITAL, CMOS 64K X 16 UV EPROM, MONOLITHIC SILICON

| SIZE | CAGE CODE | |
|---|---|---|
| A | **67268** | **5962-86805** |

SHEET 1 OF 14

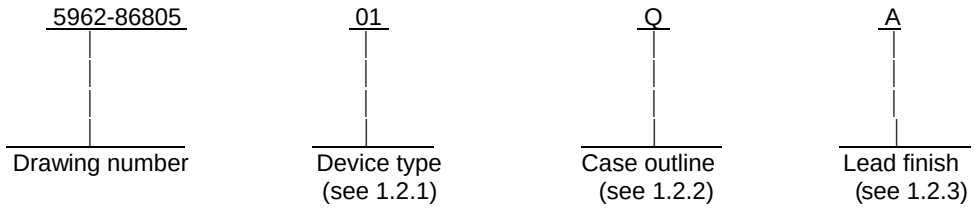
DSCC FORM 2233
APR 97

5962-E451-06

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:




1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number 1/ | Circuit function | Access time |
|---|---|---|---|
| 01 | | 64K x 16-bit UVEPROM | 300 ns |
| 02 | | 64K x 16-bit UVEPROM | 250 ns |
| 03 | | 64K x 16-bit UVEPROM | 200 ns |
| 04 | | 64K x 16-bit UVEPROM | 170 ns |
| 05 | | 64K x 16-bit UVEPROM | 150 ns |
| 06 | | 64K x 16-bit UVEPROM | 120 ns |
| 07 | | 64K x 16-bit UVEPROM | 90 ns |
| 08 | | 64K x 16-bit UVEPROM | 70 ns |

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| Q | GDIP1-T40 or CDIP2-T40 | 40 | dual-in-line package 2/ |
| X | CQCC1-N44 | 44 | square chip carrier package 2/ |

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

| | |
|---|---|
| Storage temperature range | -65°C to +150°C |
| All input or output voltage with respect to ground | -0.6 V dc to $V_{CC}$ +0.5 V dc |
| Voltage on pin $A_9$ with respect to ground | -0.6 V dc to +13.5 V dc |
| Power dissipation ($P_D$) 3/ | 330 mW |
| Lead temperature (soldering, 10 seconds) | +300°C |
| Thermal resistance, junction-to-case ($\theta_{JC}$) | See MIL-STD-1835 |
| Junction temperature ($T_J$) 4/ | +150°C |
| Data retention | 10 years, minimum |
| Endurance | 50 cycles byte, minimum |

1.4 Recommended operating conditions.

| | |
|---|---|
| Case operating temperature range ($T_C$) | -55°C to +125°C |
| Supply voltage range ($V_{CC}$) | +4.5 V dc to +5.5 V dc |

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535 and MIL-HDBK-103.
2/ Lid shall be transparent to permit ultraviolet light erasure.
3/ Must withstand the added $P_D$ due to short-circuit test; e.g., $I_{OS}$.
4/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s).

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C inspection (see 4.3), the devices shall be programmed by the manufacturer prior to test in a checkerboard or similar pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.3.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing EPROMs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EPROMs. When specified, devices shall be erased in accordance with the procedure and characteristics specified in 4.4 herein.

3.10.2 Programmability of EPROMs. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 herein.

3.10.3 Verification of erasure and/or programmability of EPROMs. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions<br>$-55°C < T_C < +125°C$<br>$V_{SS} = 0$ V;<br>$4.5 V < V_{CC} < 5.5$ V<br>unless otherwise specified | Group A subgroups | Device types | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Input leakage current | $I_{LI}$ | $V_{IN} = 0$ V to 5.5 V | 1, 2, 3 | All | -5 | +5 | µA |
| Output leakage current | $I_{LO}$ 1/ | $V_{OUT} = 0$ V to 5.5 V | 1, 2, 3 | All | -10 | +10 | µA |
| Operating current | $I_{CC1}$ | $V_{CC} = V_{PP} = 5.5$ V<br>$\overline{CE} = \overline{OE} = V_{IL}$<br>$0_{0-15} = 0$ mA<br>$f = 1/t_{AVQV}$ (maximum) | 1, 2, 3 | 01-06, 07 | | 60 | mA |
| | | | | 08 | | 90 | |
| Standby current (TTL inputs) | $I_{CC2}$ | $V_{CC} = 5.5$ V<br>$\overline{CE} = V_{IH}$ | 1, 2, 3 | 01-06 | | 1 | mA |
| | | | | 07-08 | | 20 | |
| Standby current (CMOS inputs) | $I_{CC3}$ | $V_{CC} = 5.5$ V<br>$\overline{CE} = V_{CC} \pm 0.3$ V | 1, 2, 3 | 01-06 | | 120 | µA |
| | | | | 07-08 | | 10 | mA |
| $V_{PP}$ supply current (read) | $I_{PP}$ | $V_{PP} = 5.5$ V | 1, 2, 3 | All | | 100 | µA |
| Input low voltage (TTL) | $V_{IL}$ 2/ | | 1, 2, 3 | All | -0.1 3/ | 0.8 | V |
| Input high voltage (TTL) | $V_{IH}$ 2/ | | 1, 2, 3 | All | 2.0 | $V_{CC}$ +0.5 3/ | V |
| Output low voltage | $V_{OL}$ | $I_{OL} = 2.1$ mA<br>$V_{IL} = 0.8$ V, $V_{IH} = 2.0$ V | 1, 2, 3 | All | | 0.45 | V |
| Output high voltage | $V_{OH}$ | $I_{OH} = -400$ µA<br>$V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V | 1, 2, 3 | All | 2.4 | | V |
| Output short-circuit | $I_{OS}$ 3/ | $V_O = 0$ V | 1, 2, 3 | All | -200 | +200 | mA |
| Input capacitance | $C_{IN}$ 4/ 5/ | $V_{IN} = 0$ V, $T_C = +25°C$<br>f = 1 MHz<br>See 4.3.1c | 4 | All | | 25 | pF |
| Output capacitance | $C_{OUT}$ 4/ 5/ | $V_{OUT} = 0$ V, $T_C = +25°C$<br>f = 1 MHz<br>See 4.3.1c | 4 | All | | 25 | pF |
| Functional tests | | See 4.3.1e | 7, 8 | All | | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions<br>$-55°C < T_C < +125°C$<br>$V_{SS} = 0$ V;<br>$4.5 V < V_{CC} < 5.5$ V<br>unless otherwise specified | Group A subgroups | Device types | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Address to output delay | $t_{AVQV}$ | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$ 6/<br>See figures 3 and 4 as applicable | 9, 10, 11 | 01 | | 300 | ns |
| | | | | 02 | | 250 | |
| | | | | 03 | | 200 | |
| | | | | 04 | | 170 | |
| | | | | 05 | | 150 | |
| | | | | 06 | | 120 | |
| | | | | 07 | | 90 | |
| | | | | 08 | | 70 | |
| $\overline{CE}$ to output delay | $t_{ELQV}$ | $\overline{OE}$ = $V_{IL}$ 6/<br>See figures 3 and 4 as applicable | 9, 10, 11 | 01 | | 300 | ns |
| | | | | 02 | | 250 | |
| | | | | 03 | | 200 | |
| | | | | 04 | | 170 | |
| | | | | 05 | | 150 | |
| | | | | 06 | | 120 | |
| | | | | 07 | | 90 | |
| | | | | 08 | | 70 | |
| $\overline{OE}$ to output delay | $t_{OLQV}$ | $\overline{CE}$ = $V_{IL}$ 6/<br>See figures 3 and 4 as applicable | 9, 10, 11 | 01 | | 120 | ns |
| | | | | 02 | | 100 | |
| | | | | 03 | | 75 | |
| | | | | 04,05 | | 65 | |
| | | | | 06 | | 50 | |
| | | | | 07, 08 | | 30 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions<br>$-55°C < T_C < +125°C$<br>$V_{SS} = 0$ V;<br>$4.5 V < V_{CC} < 5.5 V$<br>unless otherwise specified | Group A subgroups | Device types | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| $\overline{CE}$ and $\overline{OE}$ high to output float | $t_{EHQZ}$<br>$t_{OHQZ}$<br>4/ | See figures 3 and 4 as applicable | 9, 10, 11 | 01 | | | ns |
| | | | | 02 | | 60 | |
| | | | | 03 | | | |
| | | | | 04,05, 06 | | 50 | |
| | | | | 07 | | 20 | |
| | | | | 08 | | 15 | |
| Output hold from address $\overline{CE}$ or $\overline{OE}$ whichever occurred first | $t_{AXQX}$<br>3/ | See figures 3 and 4 as applicable | 9, 10, 11 | All | 0 | | ns |

1/ Connect all address inputs and $\overline{OE}$ to $V_{IH}$ and measure $I_{LO}$ with the output under test connected to $V_{OUT}$.

2/ Test for all input and control pins.

3/ May not be tested, but shall be guaranteed to the limits specified in table I.

4/ Tested initially and after any design changes that affect this parameter, and therefore shall be guaranteed to the limits specified in table I.

5/ All pins not being tested shall be grounded.

6/ Equivalent ac test conditions (actual load conditions vary by tester):

Output load = See figure 3.

Input rise and fall times $\leq$ 20 ns.

Input pulse levels: 0.45 V and 2.4 V.

Timing measurement reference levels:

Inputs = 0.8 V and 2.0 V

Outputs = 0.8 V and 2.0 V

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps performed in the listed sequence.

Margin test method A. (Steps 1 through 4 may be performed at the wafer level.)

(1) Program at +25°C with a greater than 95 percent pattern (example, diagonal "1's")(see 3.10.2 and 3.10.3).

(2) Unbiased bake for 24 hours at +175°C.

(3) Test at $T_C$ = +25°C minimum (see 3.10.3), including a margin test at Vm = +6 V and loose timing (i.e., $t_{AVQV}$ = 1 µs).

(4) Erase.

(5) Program at +25°C with a checkerboard pattern (see 3.10.2 and 3.10.3)

(6) Test at $T_C$ = +25°C (minimum), including a margin test at Vm = +6 V and loose timing (i.e., $t_{AVQV}$ = 1 µs).

(7) Burn-in (see 4.2A).

(8) Test at $T_C$ = +25°C (see 3.10.3), including a margin test at Vm = +6 V and loose timing (i.e., $t_{AVQV}$ = 1 µs).

(9) Test at $T_C$ = +125°C (minimum), including a margin test at Vm = +6 V and loose timing (i.e., $t_{AVQV}$ = 1 µs).

(10) Test at $T_C$ = -55°C, including a margin test at Vm = +6 V and loose timing (i.e., $t_{AVQV}$ = 1 µs).

(11) Erase (see 3.10.1). Devices may be submitted for groups A, B, C, and D testing prior to erasure provided the devices have been 100 percent seal tested in accordance with method 5004 of MIL-STD-883.

(12) Verify erasure at +25°C (see 3.10.3).

Margin test method B. (Steps 1 through 3 may be performed at the wafer level.)

(1) At +25°C program greater than 95 percent of the bit locations, including the slowest programming cell.

(2) Bake unbiased for 72 hours at +140°C or for 48 hours at 150°C or for 8 hours at 200°C or, for unassembled devices only, 72 hours at 225°C. The maximum unbiased bake temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.

(3) At +25°C perform a margin test using $V_M$= +5.8 V to loose timing (i.e., $t_{AA}$ = 1µs).

(4) Perform dynamic burn-in in accordance with 4.2a.

(5) At +25°C perform a margin test using $V_M$= +5.8 V to loose timing (i.e., $t_{AA}$ = 1µs).

(6) Perform electrical test in accordance with 4.2b.

(7) Repeat steps 5 and 6 at $T_C$ = 125°C and -55°C.

(8) Erase per 3.10.1. Devices may be submitted to quality conformance inspection.

(9) Verify erasure in accordance with 3.10.3.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 ($C_{IN}$ and $C_{OUT}$ measurements) shall be measured only for the initial test and after process or design changes which may affect input or output capacitance. Sample size is 15 devices, all input and output terminals tested and no failures.

d. All devices selected for testing shall have the EPROM programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups B, C, and D testing).

e. Subgroups 7 and 8 shall consist of verifying the EPROM pattern specified in 4.3.1d.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. A reprogrammability test shall be added to group C inspection prior to performing the steady-state life test (see 4.3.2b). The devices to be submitted to the steady-state life testing shall be subjected to the following tests and examinations. Each device in the sample shall be subjected to a minimum 50-program and erase cycles.

(1) All devices selected for testing shall be programmed with a checkerboard pattern or equivalent.

(2) Verify patterns (see 3.10.3).

(3) Erase (see 3.10.1).

(4) Verify pattern erasure (see 3.10.3).

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to short-wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for exposure should be a minimum of 15 $Ws/cm^2$. The erasure time with this dosage is approximately 25 minutes using an ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 $Ws/cm^2$ (1 week at 12000 $\mu W/cm^2$). Exposure of EPROMs to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

| Device types | 01 through 08 | | | Device types | 01 through 08 | |
|---|---|---|---|---|---|---|
| Case outlines | Q | X | | Case outlines | Q | X |
| Terminal number | Terminal symbol | | | Terminal number | Terminal symbol | |
| 1 | $V_{PP}$ | NC | | 23 | $A_2$ | NC |
| 2 | $\overline{CE}$ | $V_{PP}$ | | 24 | $A_3$ | $A_0$ |
| 3 | $I/O_{15}$ | $\overline{CE}$ | | 25 | $A_4$ | $A_1$ |
| 4 | $I/O_{14}$ | $I/O_{15}$ | | 26 | $A_5$ | $A_2$ |
| 5 | $I/O_{13}$ | $I/O_{14}$ | | 27 | $A_6$ | $A_3$ |
| 6 | $I/O_{12}$ | $I/O_{13}$ | | 28 | $A_7$ | $A_4$ |
| 7 | $I/O_{11}$ | $I/O_{12}$ | | 29 | $A_8$ | $A_5$ |
| 8 | $I/O_{10}$ | $I/O_{11}$ | | 30 | $V_{SS}$ | $A_6$ |
| 9 | $I/O_{09}$ | $I/O_{10}$ | | 31 | $A_9$ | $A_7$ |
| 10 | $I/O_{08}$ | $I/O_{09}$ | | 32 | $A_{10}$ | $A_8$ |
| 11 | $V_{SS}$ | $I/O_{08}$ | | 33 | $A_{11}$ | NC |
| 12 | $I/O_{07}$ | $V_{SS}$ | | 34 | $A_{12}$ | $V_{SS}$ |
| 13 | $I/O_{06}$ | NC | | 35 | $A_{13}$ | $A_9$ |
| 14 | $I/O_{05}$ | $I/O_{07}$ | | 36 | $A_{14}$ | $A_{10}$ |
| 15 | $I/O_{04}$ | $I/O_{06}$ | | 37 | $A_{15}$ | $A_{11}$ |
| 16 | $I/O_{03}$ | $I/O_{05}$ | | 38 | NC | $A_{12}$ |
| 17 | $I/O_{02}$ | $I/O_{04}$ | | 39 | $\overline{PGM}$ | $A_{13}$ |
| 18 | $I/O_{01}$ | $I/O_{03}$ | | 40 | $V_{CC}$ | $A_{14}$ |
| 19 | $I/O_0$ | $I/O_{02}$ | | 41 | --- | $A_{15}$ |
| 20 | $\overline{OE}$ | $I/O_{01}$ | | 42 | --- | NC |
| 21 | $A_0$ | $I/O_0$ | | 43 | --- | $\overline{PGM}$ |
| 22 | $A_1$ | $\overline{OE}$ | | 44 | --- | $V_{CC}$ |

FIGURE 1. Terminal connections.

| Mode | Pin function | | | | | |
|---|---|---|---|---|---|---|
| | $\overline{CE}$ | $\overline{OE}$ | $\overline{PGM}$ | $A_9$ | $V_{PP}$ | Outputs |
| Read | L | L | X | X | $V_{CC}$ | Data out |
| Output disable | L | H | X | X | X | High Z |
| Standby | H | X | X | X | X | High Z |
| Program | L | X | L | X | $V_{PP}$ | Data in |
| Program verify | L | L | H | X | $V_{PP}$ | Data out |
| Program inhibit | H | X | X | X | $V_{PP}$ | High Z |
| Auto select | L | L | X | $V_H$ | X | Code |

H = $V_{IH}$

L = $V_{IL}$

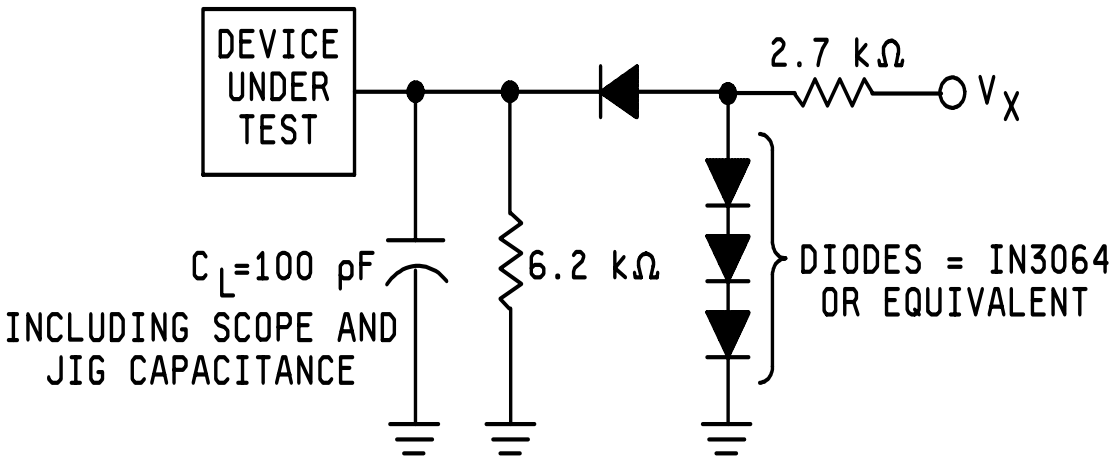
X = $V_{IH}$ or $V_{IL}$

$V_H$ = 12.0 ±0.5 V

$V_{CC}$ = +4.5 V dc to 5.5 V dc

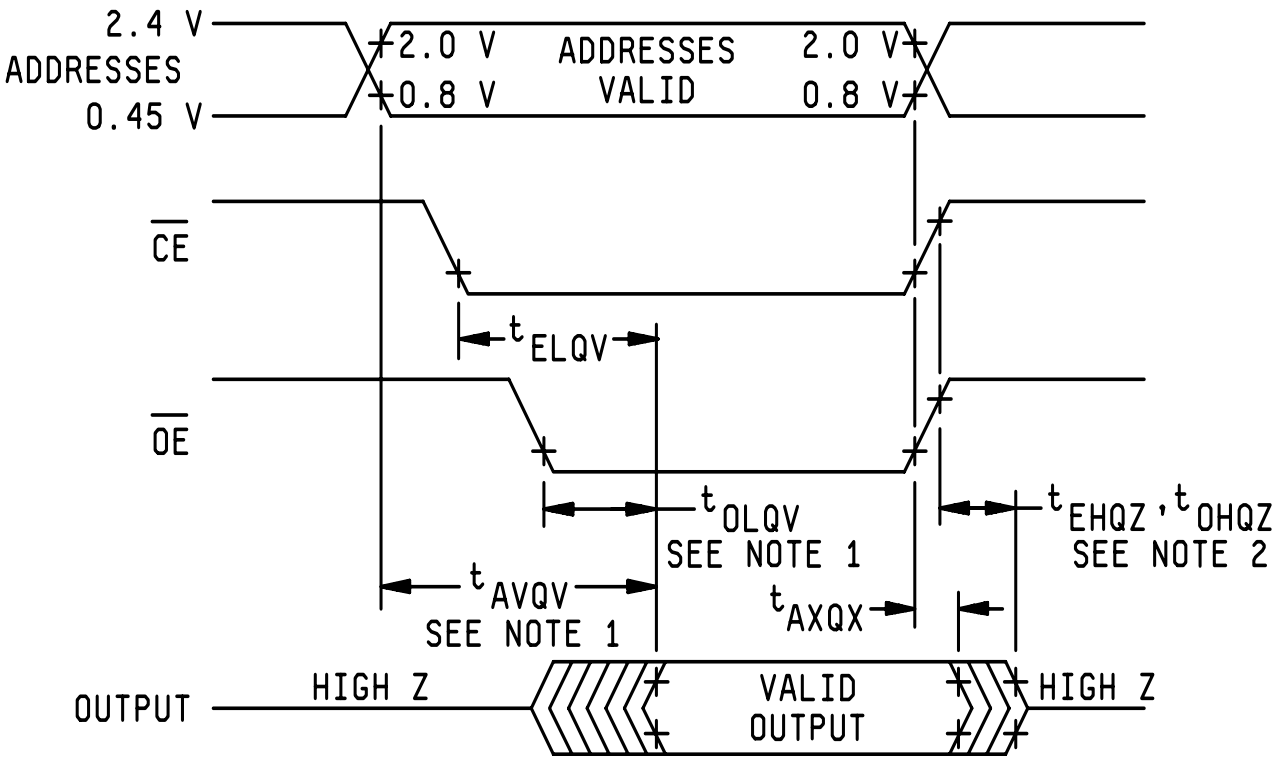
$V_{PP}$ = See 4.5

FIGURE 2. Truth table




$V_X$ = voltage required to supply 2.1 mA ($I_{OL}$) when the output of the device under test (DUT) is in the "0" state.

FIGURE 3. Switching times test circuit ( or equivalent).




NOTES:

1. $\overline{OE}$ may be delayed up to $t_{ELQV}$ - $t_{OLQV}$ after the falling edge of $\overline{CE}$ without impact on $t_{ELQV}$.
2. $t_{OHQZ}$ or $t_{EHQZ}$ is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

FIGURE 4. Read cycle waveforms.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/ 5/

| MIL-STD-883 test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) |
|---|---|
| Interim electrical parameters (method 5004) | - - - |
| Final electrical test parameters (method 5004) | 1*, 2, 3, 7*,8A,8B, 9, 10, 11 |
| Group A test requirements (method 5005) 5/ | 1, 2, 3, 4***, 7,8A, 8B,9 10**, 11** |
| Groups C and D end-point electrical parameters (method 5005) | 2, 3, 7,8A,8B |

1/ (*) indicates PDA applies to subgroups 1 and 7.
2/ (***) see 4.3.1c.
3/ Any subgroups at the same temperature may be combined when using a multifunction tester.
4/ (**) indicates that subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.
5/ Subgroups 7, 8A, and 8B shall consist of verifying the applicable data pattern, see 4.3.1e.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-05-31

Approved sources of supply for SMD 5962-86805 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

| Standard Microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-8680501QA | 3/<br>3/<br>0C7V7 | AM27C1024-300/BQA<br>AT27C1024-30DM/883<br>AT27C1024-30/QA |
| 5962-8680501XA | 3/<br>3/<br>0C7V7 | AM27C1024-300/BUA<br>AT27C1024-30LM/883<br>AT27C1024-30/XA |
| 5962-8680502QA | 3/<br>3/<br>3/<br>3/<br>0C7V7 | 27C1024MQB/C25<br>AM27C1024-250/BQA<br>AT27C1024-25DM/883<br>MD27C210-25/B<br>AT27C1024-25/QA |
| 5962-8680502XA | 3/<br>3/<br>3/<br>3/<br>0C7V7 | 27C1024MEQ1B/C25<br>AM27C1024-250/BUA<br>AT27C1024-25LM/883<br>MR27C210-25/B<br>AT27C1024-25/XA |
| 5962-8680503QA | 3/<br>3/<br>3/<br>3/<br>0C7V7 | 27C1024MQB/C20<br>AM27C1024-200/BQA<br>AT27C1024-20DM/883<br>MD27C210-20/B<br>AT27C1024-20/QA |
| 5962-8680503XA | 3/<br>3/<br>3/<br>3/<br>0C7V7 | 27C1024MEQ1B/C20<br>AM27C1024-200/BUA<br>AT27C1024-20LM/883<br>MR27C210-20/B<br>AT27C1024-20/XA |
| 5962-8680504QA | 3/<br>3/<br>3/<br>0C7V7 | AM27C1024-170/BQA<br>AT27C1024-17DM/883<br>MD27C210-17/B<br>AT27C1024-17/QA |
| 5962-8680504XA | 3/<br>3/<br>3/<br>0C7V7 | AM27C1024-170/BUA<br>AT27C1024-17LM/883<br>MR27C210-17/B<br>AT27C1024-17/XA |
| 5962-8680504XC | 0C7V7 | AT27C1024-17/XC |

See footnotes at end of table.

| Standard Microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-8680505QA | 3/<br>3/<br>3/<br>3/<br>0C7V7 | 27C1024MQB/C15<br>AM27C1024-150/BQA<br>AT27C1024-15DM/883<br>MD27C210-15/B<br>AT27C1024-15/QA |
| 5962-8680505XA | 3/<br>3/<br>3/<br>3/<br>0C7V7 | 27C1024MEQ1B/C15<br>AM27C1024-150/BUA<br>AT27C1024-15LM/883<br>MR27C210-15/B<br>AT27C1024-15/XA |
| 5962-8680506QA | 3/<br>3/<br>3/<br>0C7V7 | 27C1024MQB/C12<br>AM27C1024-120/BQA<br>AT27C1024-12DM/883<br>AT27C1024-12/QA |
| 5962-8680506XA | 3/<br>3/<br>3/<br>0C7V7 | 27C1024MEQ1B/C12<br>AM27C1024-120/BUA<br>AT27C1024-12LM/883<br>AT27C1024-12/XA |
| 5962-8680507QA | 3/<br>3/<br>0C7V7 | 27C1024MQB/C90<br>AT27HC1024-90DM/883<br>AT27C1024-90/QA |
| 5962-8680507XA | 3/<br>3/<br>0C7V7 | 27C1024MEQ1B/C90<br>AT27HC1024-90LM/883<br>AT27C1024-90/XA |
| 5962-8680508QA | 3/<br>0C7V7 | AT27HC1024-70DM/883<br>AT27HC1024-70/QA |
| 5962-8680508XA | 3/<br>0C7V7 | AT27HC1024-70LM/883<br>AT27HC1024-70/XA |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 0C7V7 | QP Semiconductor<br>2945 Oakmead Village Court<br>Santa Clara, CA 95051 |

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.