STK16C88-3

256 Kbit (32K x 8) AutoStore+ nvSRAM

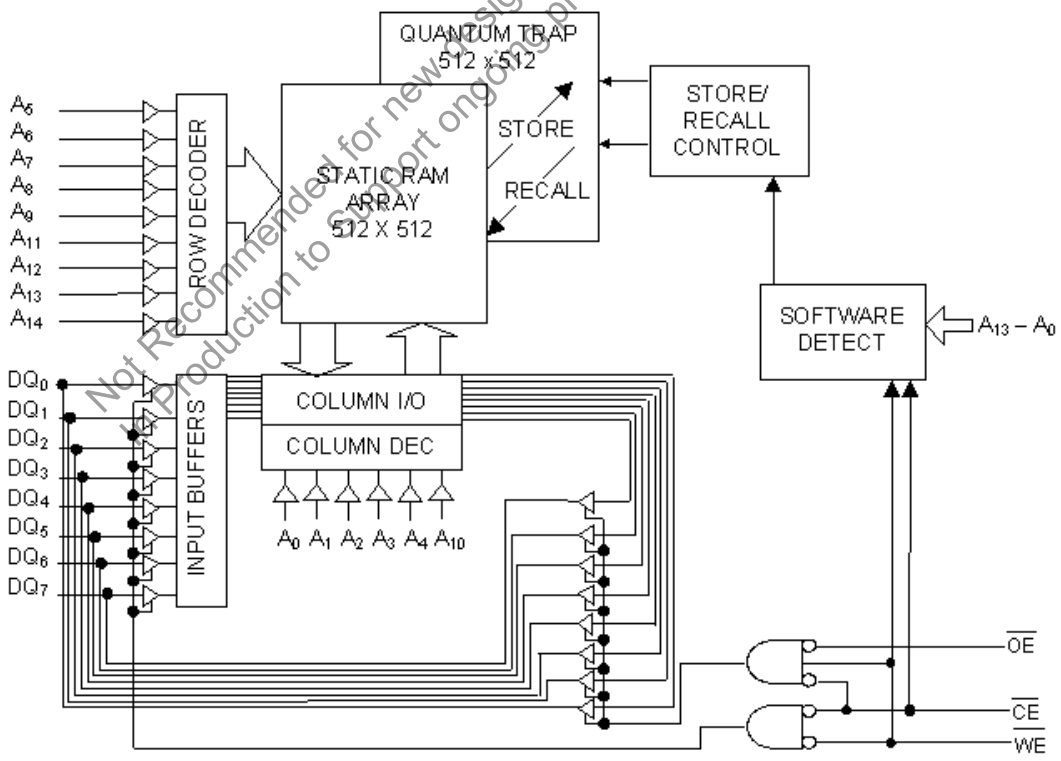
Features

- Fast 35 ns Read Access and R/W Cycle Time
- Directly replaces Battery-backed SRAM Modules such as Dallas/Maxim DS1230W
- Automatic Nonvolatile STORE on Power Loss
- Nonvolatile STORE under Software Control
- Automatic RECALL to SRAM on power up
- Unlimited Read/Write Endurance
- 1,000,000 STORE Cycles
- 100 year Data Retention
- Single 3.3V±0.3V Power Supply
- Commercial and Industrial Temperatures
- 28-pin (600 mil) PDIP package
- RoHS Compliance

Functional Description

The Cypress STK16C88-3 is a 256Kb fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent, nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power down. On power up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

Logic Block Diagram



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Pin Configurations

Figure 1. Pin Diagram - 28-Pin PDIP

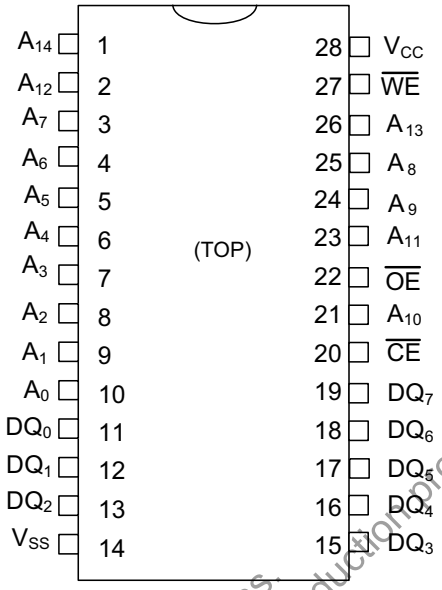


Table 1. Pin Definitions - 28-Pin PDIP

Pin Name	Alt	I/O Type	Description
A_0–A_{14}		Input	**Address Inputs.** Used to select one of the 32,768 bytes of the nvSRAM.
DQ_0-DQ_7		Input or Output	**Bidirectional Data I/O lines**. Used as input or output lines depending on operation.
$\overline{WE}$	$\overline{W}$	Input	**Write Enable Input, Active LOW**. When the chip is enabled and $\overline{WE}$ is LOW, data on the I/O pins is written to the specific address location.
$\overline{CE}$	$\overline{E}$	Input	**Chip Enable Input, Active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	$\overline{G}$	Input	**Output Enable, Active LOW**. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the I/O pins to tristate.
V_{SS}		Ground	**Ground for the Device**. The device is connected to ground of the system.
V_{CC}		Power Supply	**Power Supply Inputs to the Device**.

Device Operation

The AutoStore+ STK16C88-3 is a fast 32K x 8 SRAM that does not lose its data on power down. The data is preserved in integral QuantumTrap non-volatile storage elements when power is lost. Automatic STORE on power down and automatic RECALL on power up guarantee data integrity without the use of batteries.

SRAM Read

The STK16C88-3 performs a READ cycle whenever $\overline{CE}$ and $\overline{OE}$ are LOW while $\overline{WE}$ is HIGH. The address specified on pins $A_{0–14}$ determines the 32,768 data bytes accessed. When the READ is initiated by an address transition, the outputs are valid after a delay of t_{AA} (READ cycle 1). If the READ is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at t_{ACE} or at t_{DOE}, whichever is later (READ cycle 2). The data outputs repeatedly respond to address changes within the t_{AA} access time without the need for transitions on any control input pins, and remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH.

SRAM Write

A WRITE cycle is performed whenever $\overline{CE}$ and $\overline{WE}$ are LOW. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common I/O pins $DQ_{0–7}$ are written into the memory if it has valid t_{SD}, before the end of a $\overline{WE}$ controlled WRITE or before the end of an $\overline{CE}$ controlled WRITE. Keep $\overline{OE}$ HIGH during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{OE}$ is left LOW, internal circuitry turns off the output buffers t_{HZWE} after $\overline{WE}$ goes LOW.

AutoStore+ Operation

The STK16C88-3's automatic STORE on power down is completely transparent to the system. The STORE initiation takes less than 500 ns when power is lost (V_{CC}<V_{SWITCH}) at which point the part depends only on its internal capacitor for STORE completion.

If the power supply drops faster than 20 µs/volt before Vcc reaches Vswitch, then a 2.2 ohm resistor should be inserted between Vcc and the system supply to avoid a momentary excess of current between Vcc and internal capacitor.

In order to prevent unneeded STORE operations, automatic STOREs are ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether or not a WRITE operation has taken place.

Hardware RECALL (Power Up)

During power up or after any low power condition (V_{CC}<V_{RESET}), an internal RECALL request is latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete.

If the STK16C88-3 is in a WRITE state at the end of power up RECALL, the SRAM data is corrupted. To help avoid this situation, a 10 Kohm resistor is connected either between $\overline{WE}$ and system V_{CC} or between $\overline{CE}$ and system V_{CC}.

Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. The STK16C88-3 software STORE cycle is initiated by executing sequential $\overline{CE}$ controlled READ cycles from six specific address locations in exact order. During the STORE cycle, an erase of the previous nonvolatile data is first performed followed by a program of the nonvolatile elements. When a STORE cycle is initiated, input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence. If they intervene, the sequence is aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following READ sequence is performed:

1. Read address 0x0E38, Valid READ
2. Read address 0x31C7, Valid READ
3. Read address 0x03E0, Valid READ
4. Read address 0x3C1F, Valid READ
5. Read address 0x303F, Valid READ
6. Read address 0x0FC0, Initiate STORE cycle

The software sequence is clocked with $\overline{CE}$ controlled READs. When the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. It is important that READ cycles and not WRITE cycles are used in the sequence. It is not necessary that $\overline{OE}$ is LOW for a valid sequence. After the t_{STORE} cycle time is fulfilled, the SRAM is again activated for READ and WRITE operation.

Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of $\overline{CE}$ controlled READ operations is performed:

1. Read address 0x0E38, Valid READ
2. Read address 0x31C7, Valid READ
3. Read address 0x03E0, Valid READ
4. Read address 0x3C1F, Valid READ
5. Read address 0x303F, Valid READ
6. Read address 0x0C63, Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared, and then the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is once again ready for READ and WRITE operations. The RECALL operation does not alter the data in the nonvolatile elements. The nonvolatile data can be recalled an unlimited number of times.

Hardware Protect

The STK16C88-3 offers hardware protection against inadvertent STORE operation and SRAM WRITEs during low voltage conditions. When V_{CAP}<V_{SWITCH}, all externally initiated STORE operations and SRAM WRITEs are inhibited.

Noise Considerations

The STK16C88-3 is a high speed memory. It must have a high frequency bypass capacitor of approximately 0.1 µF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high speed CMOS ICs, careful routing of power, ground, and signals helps prevent noise problems.

Low Average Active Power

CMOS technology provides the STK16C88-3 the benefit of drawing significantly less current when it is cycled at times longer than 50 ns. Figure 2 and Figure 3 shows the relationship between I_{CC} and READ or WRITE cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, VCC = 5.5V, 100% duty cycle on chip enable). Only standby current is drawn when the chip is disabled. The overall average current drawn by the STK16C88-3 depends on the following items:

1. The duty cycle of chip enable
2. The overall cycle rate for accesses
3. The ratio of READs to WRITEs
4. CMOS versus TTL input levels
5. The operating temperature
6. The V_{CC} level
7. I/O loading

Figure 2. Current Versus Cycle Time (READ)

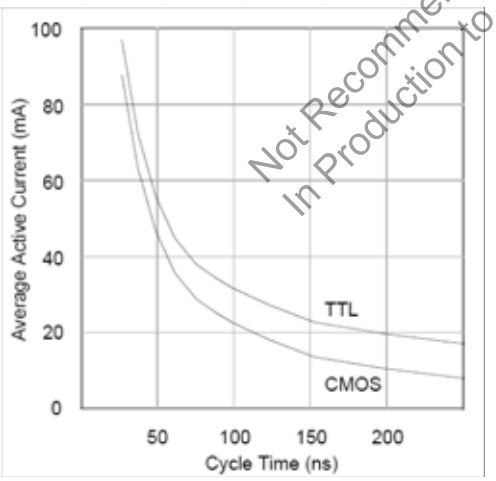
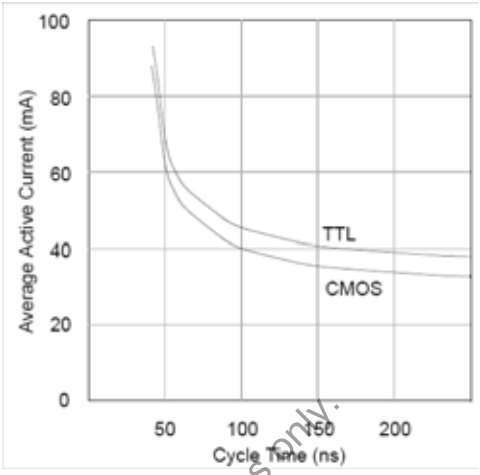


Figure 3. Current Versus Cycle Time (WRITE)



Best Practices

nvSRAM products have been used effectively for over 15 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The nonvolatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites will sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume a NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration and cold or warm boot status, should always program a unique NV pattern (for example, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power up boot firmware routines should rewrite the nvSRAM into the desired state. While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently (program bugs or incoming inspection routines).

Table 2. Software STORE/RECALL Mode Selection

$\overline{CE}$	$\overline{WE}$	$A_{13} - A_0$	Mode	I/O	Notes
L	H	0x0E38 0x31C7 0x03E0 0x3C1F 0x303F 0x0FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output Data Output Data Output Data Output Data Output Data Output Data	[1, 2]
L	H	0x0E38 0x31C7 0x03E0 0x3C1F 0x303F 0x0C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output Data Output Data Output Data Output Data Output Data Output Data	[1, 2]

Notes
1. The six consecutive addresses must be in the order listed. $\overline{WE}$ must be high during all six consecutive $\overline{CE}$ controlled cycles to enable a nonvolatile cycle.
2. While there are 15 addresses on the STK16C88-3, only the lower 14 are used to control software modes.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Temperature under bias..... –55°C to +125°C

Supply Voltage on V_{CC} Relative to GND .....–0.5V to 4.5V

Voltage on Input Relative to Vss..... –0.6V to V_{CC} + 0.5V

Voltage on DQ_{0-7} .....–0.5V to Vcc + 0.5V

Power Dissipation 1.0W

DC output Current (1 output at a time, 1s duration) .... 15 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.0V to 3.6V
Industrial	-40°C to +85°C	3.0V to 3.6V

DC Electrical Characteristics

Over the operating range (V_{CC} = 3.0V to 3.6V)

Parameter	Description	Test Conditions		Min	Max	Unit
I_{CC1}	Average V_{CC} Current	t_{RC} = 35 ns Dependent on output loading and cycle rate. Values obtained without output loads. I_{OUT} = 0 mA.	Commercial		50	mA
			Industrial		52	mA
I_{CC2}	Average V_{CC} Current during STORE	All Inputs Do Not Care, V_{CC} = Max Average current for duration t_{STORE}			3	mA
I_{CC3}	Average V_{CC} Current at t_{RC}= 200 ns, 5V, 25°C Typical	$\overline{WE} \geq (V_{CC} - 0.2V)$. All other inputs cycling. Dependent on output loading and cycle rate. Values obtained without output loads.			8	mA
I_{SB1} [3]	Average V_{CC} Current (Standby, Cycling TTL Input Levels)	t_{RC}=35ns, $\overline{CE} \geq V_{IH}$	Commercial		18	mA
			Industrial		19	mA
I_{SB2}[3]	V_{CC} Standby Current (Standby, Stable CMOS Input Levels)	$\overline{CE} \geq (V_{CC} - 0.2V)$. All others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$.			1	mA
I_{IX}	Input Leakage Current	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$		-1	+1	µA
I_{OZ}	Off State Output Leakage Current	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$, $\overline{CE}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$		-1	+1	µA
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			V_{SS} – 0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OUT} = –4 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OUT} = 8 mA			0.4	V

Data Retention and Endurance

Parameter	Description	Min	Unit
$DATA_R$	Data Retention	100	Years
NV_C	Nonvolatile STORE Operations	1,000	K

Note

3. $\overline{CE} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.

Capacitance

In the following table, the capacitance parameters are listed.[4]

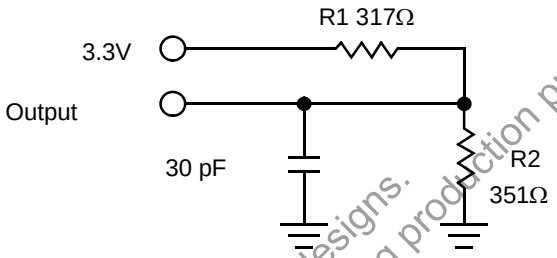
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 0 to 3.0 V	5	pF
C_{OUT}	Output Capacitance		7	pF

Thermal Resistance

In the following table, the thermal resistance parameters are listed.[4]

Parameter	Description	Test Conditions	28-PDIP	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		TBD	°C/W

Figure 4. AC Test Loads



AC Test Conditions

Input Pulse Levels ..... 0 V to 3 V
Input Rise and Fall Times (10% - 90%) ..... ≤5 ns
Input and Output Timing Reference Levels ..... 1.5 V

Note
4. These parameters are guaranteed by design and are not tested.

AC Switching Characteristics

SRAM Read Cycle

Parameter		Description	35 ns		Unit
Cypress Parameter	Alt		Min	Max	
t_{ACE}	t_{ELQV}	Chip Enable Access Time		35	ns
t_{RC} [5]	t_{AVAV}, t_{ELEH}	Read Cycle Time	35		ns
t_{AA} [6]	t_{AVQV}	Address Access Time		35	ns
t_{DOE}	t_{GLQV}	Output Enable to Data Valid		15	ns
t_{OHA} [6]	t_{AXQX}	Output Hold After Address Change	5		ns
t_{LZCE} [7]	t_{ELQX}	Chip Enable to Output Active	5		ns
t_{HZCE} [7]	t_{EHQZ}	Chip Disable to Output Inactive		13	ns
t_{LZOE} [7]	t_{GLQX}	Output Enable to Output Active	0		ns
t_{HZOE} [7]	t_{GHQZ}	Output Disable to Output Inactive		13	ns
t_{PU} [4]	t_{ELICCH}	Chip Enable to Power Active	0		ns
t_{PD} [3, 4]	t_{EHICCL}	Chip Disable to Power Standby		35	ns

Switching Waveforms

Figure 5. SRAM Read Cycle 1: Address Controlled [5, 6]

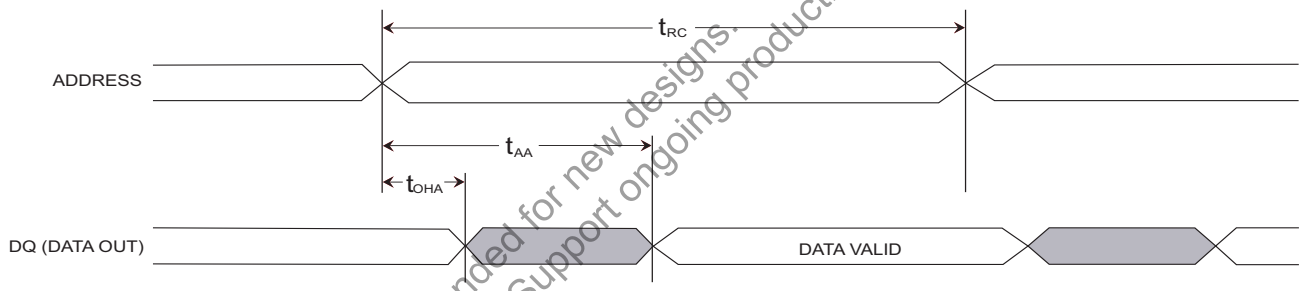
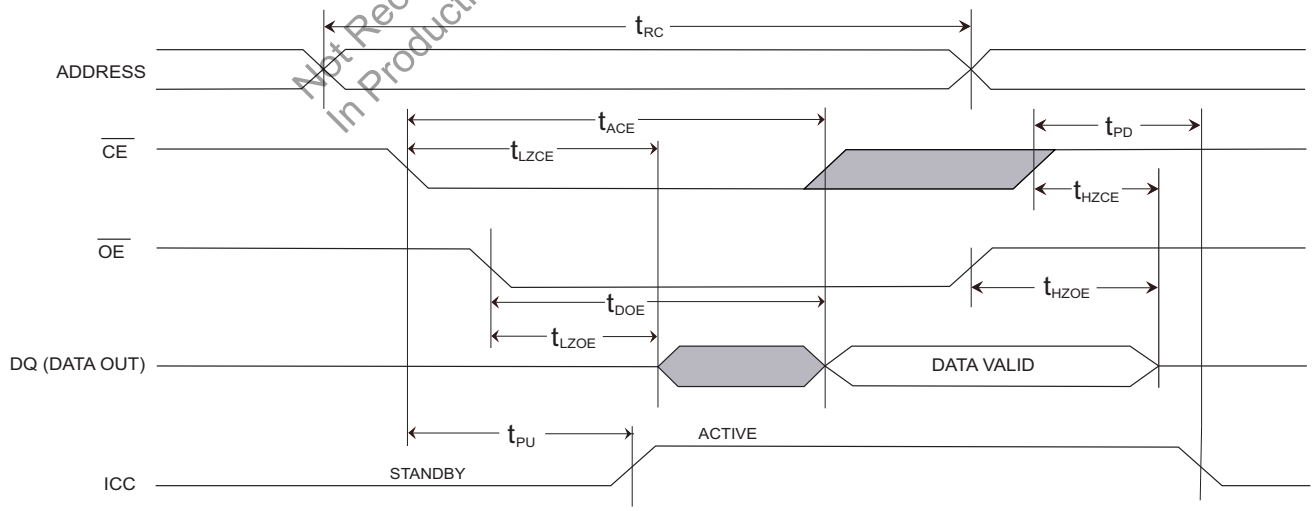


Figure 6. SRAM Read Cycle 2: $\overline{CE}$ and $\overline{OE}$ Controlled [5]



Notes
5. $\overline{WE}$ must be HIGH during SRAM Read Cycles.
6. I/O state assumes $\overline{CE}$ and $\overline{OE} \leq V_{IL}$ and $\overline{WE} \geq V_{IH}$; device is continuously selected.
7. Measured ±200 mV from steady state output voltage.

Table 3. SRAM Write Cycle

Parameter		Description	35 ns		Unit
Cypress Parameter	Alt		Min	Max	
t_{WC}	t_{AVAV}	Write Cycle Time	35		ns
t_{PWE}	t_{WLWH}, t_{WLEH}	Write Pulse Width	25		ns
t_{SCE}	t_{ELWH}, t_{ELEH}	Chip Enable To End of Write	25		ns
t_{SD}	t_{DVWH}, t_{DVEH}	Data Setup to End of Write	12		ns
t_{HD}	t_{WHDX}, t_{EHDX}	Data Hold After End of Write	0		ns
t_{AW}	t_{AVWH}, t_{AVEH}	Address Setup to End of Write	25		ns
t_{SA}	t_{AVWL}, t_{AVEL}	Address Setup to Start of Write	0		ns
t_{HA}	t_{WHAX}, t_{EHAX}	Address Hold After End of Write	0		ns
t_{HZWE} [7,8]	t_{WLQZ}	Write Enable to Output Disable		13	ns
t_{LZWE} [7]	t_{WHQX}	Output Active After End of Write	5		ns

Switching Waveforms

Figure 7. SRAM Write Cycle 1: $\overline{WE}$ Controlled [9]

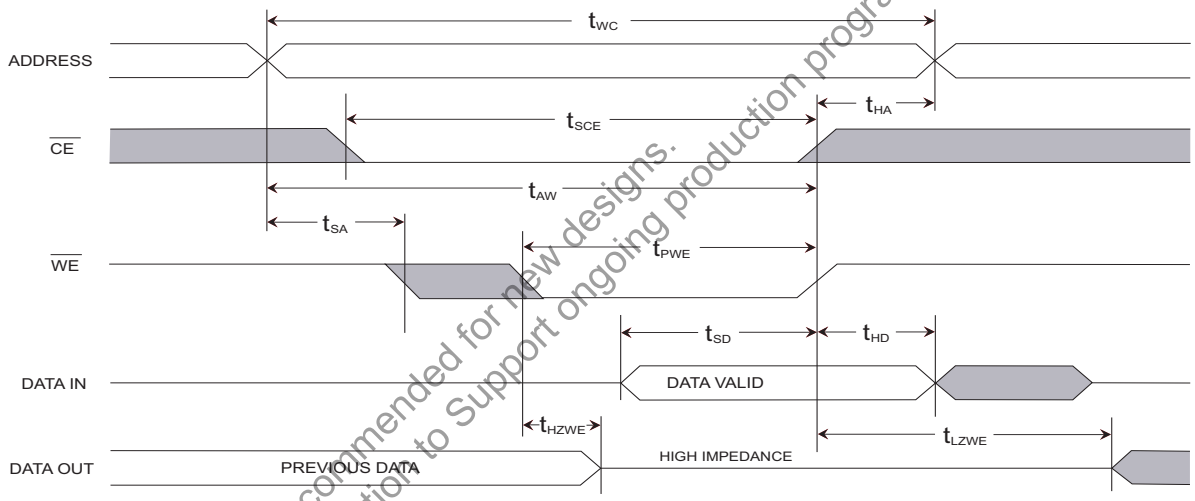
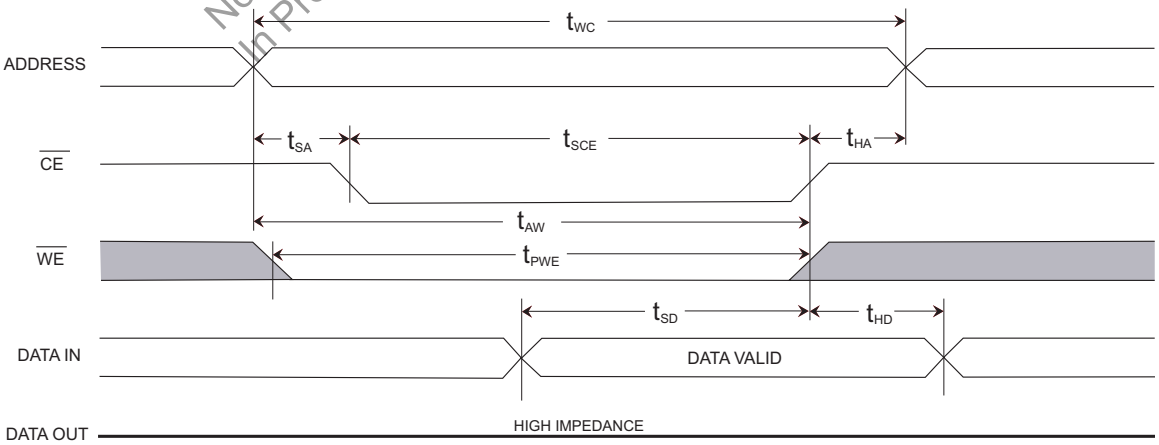


Figure 8. SRAM Write Cycle 2: $\overline{CE}$ Controlled [9]



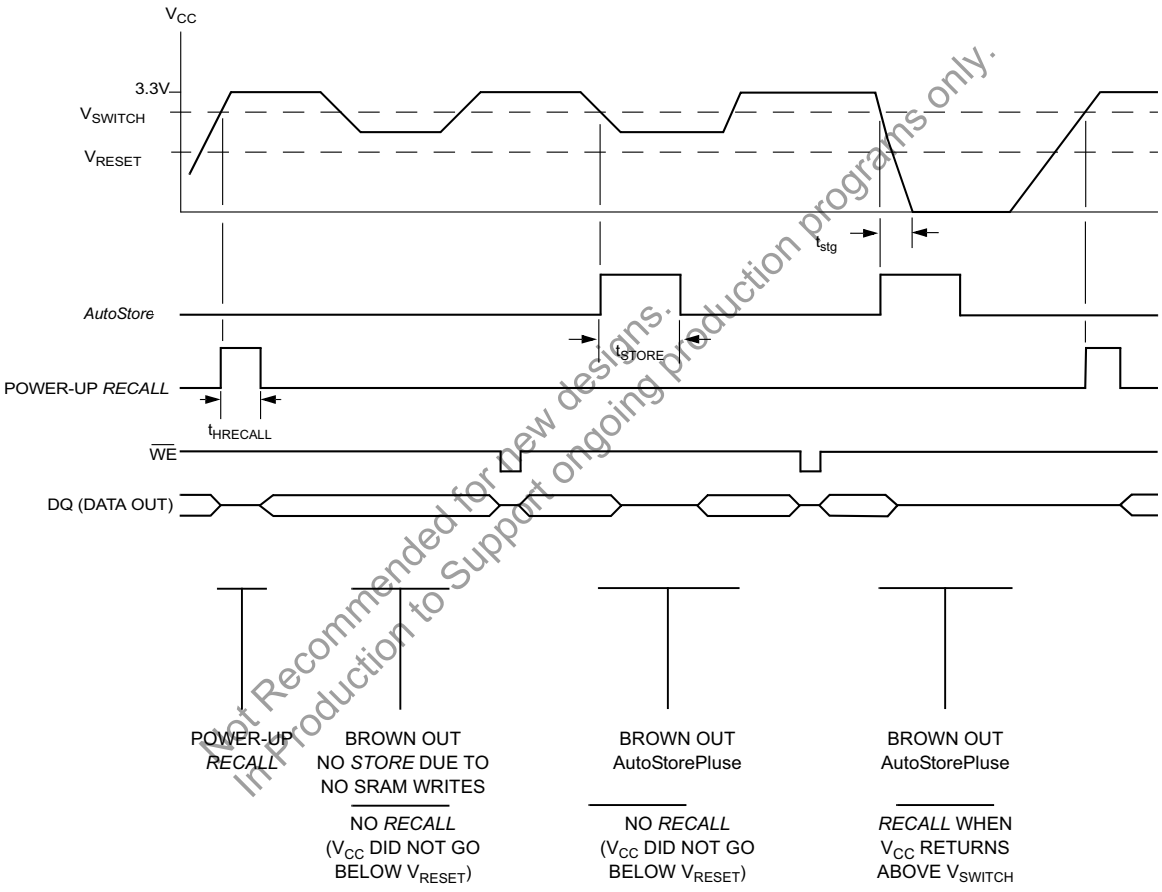
Notes
8. If $\overline{WE}$ is Low when $\overline{CE}$ goes Low, the outputs remain in the high impedance state.
9. $\overline{CE}$ or $\overline{WE}$ must be greater than V_{IH} during address transitions.

AutoStorePlus or Power Up RECALL

Parameter	Alt	Description	STK16C88-3		Unit
			Min	Max	
$t_{HRECALL}$ [10]	$t_{RESTORE}$	Power up RECALL Duration		550	µs
t_{STORE}	t_{HLHZ}	STORE Cycle Duration		10	ms
t_{stg} [4, 6]		Power-down AutoStore Slew Time to Ground	500		ns
V_{RESET}		Low Voltage Reset Level		2.4	V
V_{SWITCH}		Low Voltage Trigger Level	2.7	2.95	V

Switching Waveforms

Figure 9. AutoStorePlus/Power Up RECALL



Note
10. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.

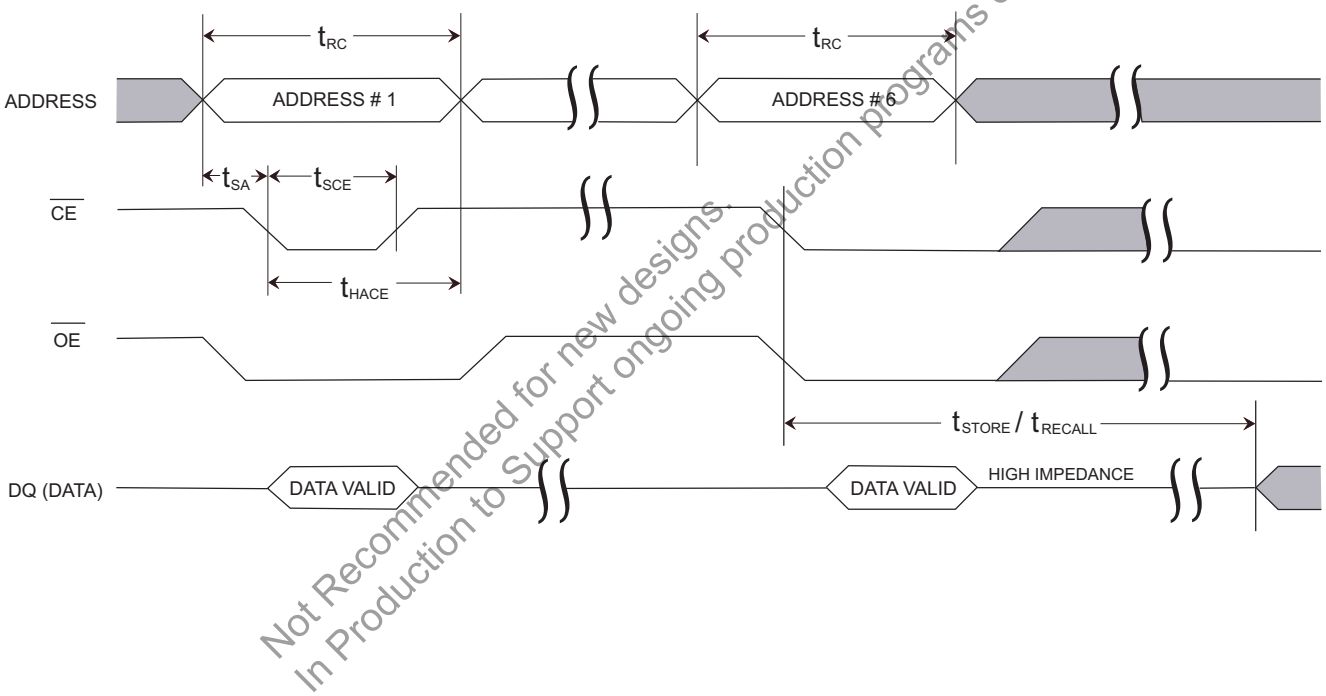
Software Controlled STORE/RECALL Cycle

The software controlled STORE/RECALL cycle follows. [11, 12]

Parameter	Alt	Description	35 ns		Unit
			Min	Max	
t_{RC}	t_{AVAV}	STORE/RECALL Initiation Cycle Time	35		ns
t_{SA}[11]	t_{AVEL}	Address Setup Time	0		ns
t_{CW}[11]	t_{ELEH}	Clock Pulse Width	25		ns
t_{HACE}[7, 11]	t_{ELAX}	Address Hold Time	20		ns
t_{RECALL}		RECALL Duration		20	µs

Switching Waveforms

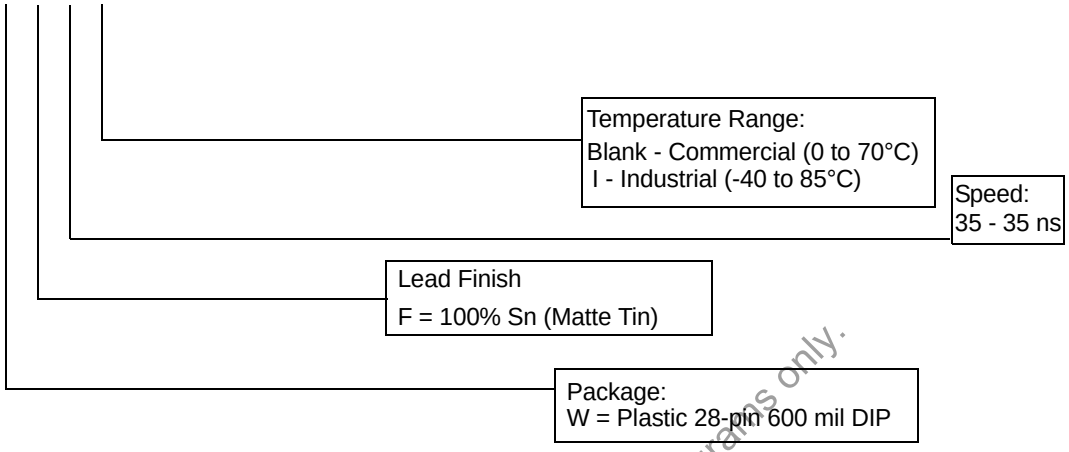
Figure 10. $\overline{CE}$ Controlled Software STORE/RECALL Cycle [12]



Notes
11. The software sequence is clocked on the falling edge of $\overline{CE}$ without involving $\overline{OE}$ (double clocking will abort the sequence).
12. The six consecutive addresses must be read in the order listed in the Mode Selection table. $\overline{WE}$ must be HIGH during all six consecutive cycles.

Part Numbering Nomenclature

STK16C88 - 3W F 35 I



Ordering Information

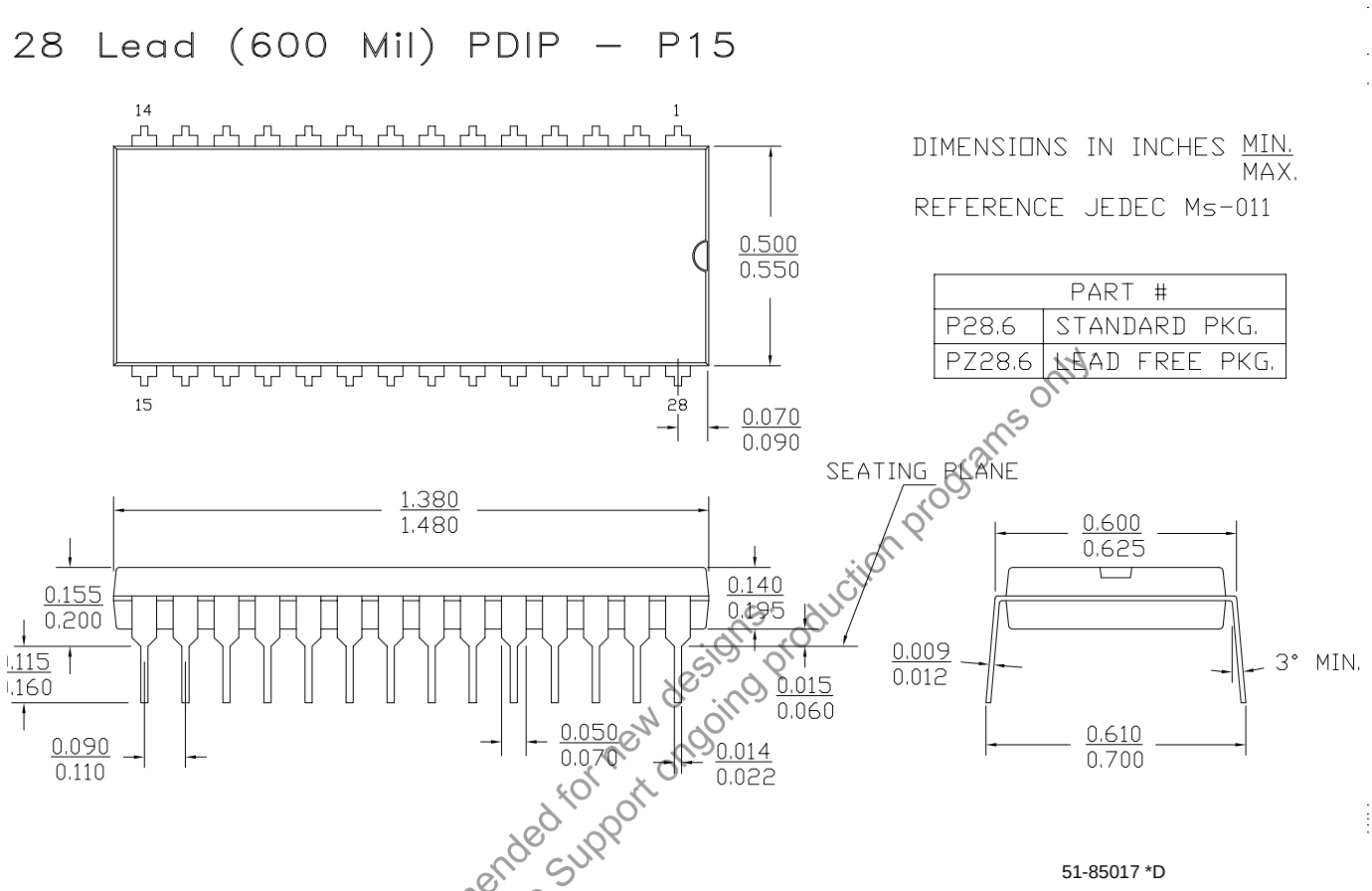
These parts are not recommended for new designs. They are in production to support ongoing production programs only.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
35	STK16C88-3WF35I	51-85017	28-pin PDIP	Industrial

All parts are Pb-free. The above table contains Final information. Please contact your local Cypress sales representative for availability of these parts

Package Diagram

Figure 11. 28-Pin (600 Mil) PDIP (51-85017)



Document History Page

Document Title: STK16C88-3 256 Kbit (32K x 8) AutoStore+ nvSRAM Document Number: 001-50594				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2625096	GVCH/PYRS	12/19/08	New data sheet
*A	2826441	GVCH	12/11/2009	Added following text in the Ordering Information section: “These parts are not recommended for new designs. In production to support ongoing production programs only.” Added watermark in PDF stating “Not recommended for new designs. In production to support ongoing production programs only.” Added Contents on page 2.
*B	2909328	GVCH	04/09/10	Removed inactive part. Updated package diagram.

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