

54ACT283 4-Bit Binary Full Adder with Fast Carry

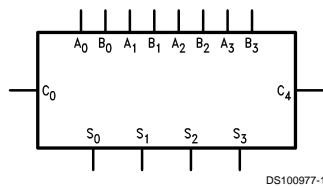
General Description

The 'ACT283 high-speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary words (A_0 – A_3 , B_0 – B_3) and a Carry input (C_0). It generates the binary Sum outputs (S_0 – S_3) and the Carry output (C_4) from the most significant bit. The 'ACT283 will operate with either active HIGH or active LOW operands (positive or negative logic).

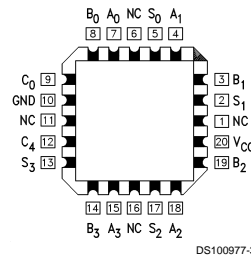
Features

- Guaranteed 4000V minimum ESD protection
- Outputs source/sink 24 mA
- TTL-compatible inputs
- Available to Mil-Std-883

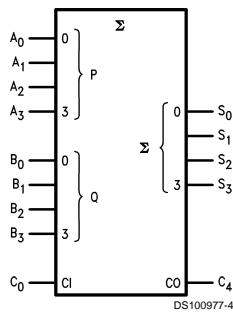
Logic Symbols



Pin Assignment for LCC



IEEE/IEC



Functional Description

The 'ACT283 adds two 4-bit binary words (A plus B) plus the incoming Carry (C_0). The binary sum appears on the Sum (S_0 – S_3) and outgoing carry (C_4) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$$2^0 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1) + 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3) = S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$

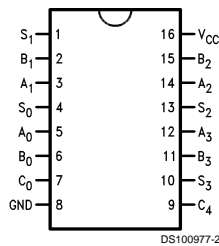
Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus C_0 , A_0 , B_0 can be arbitrarily assigned to pins 5, 6 and 7 for DIPs, and 7, 8 and 9 for chip carrier packages. Due to the symmetry of the binary add function, the 'ACT283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). See Figure 1. Note that if C_0 is not used it must be tied LOW for active HIGH logic or tied HIGH for active LOW logic.

Due to pin limitations, the intermediate carries of the 'ACT283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. Figure 2 shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A_3 , B_3) LOW makes S_3 dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, Figure 3 shows a way of dividing the 'ACT283 into a 2-bit and a 1-bit adder. The third stage adder (A_2 , B_2 , S_2) is used merely as a means of getting a carry (C_{10}) signal into the fourth stage (via A_2 and B_2) and bringing out the carry from the second stage on S_2 .

Connection Diagrams

Pin Assignment for DIP and Flatpak



Functional Description (Continued)

Note that as long as A_2 and B_2 are the same, whether HIGH or LOW, they do not influence S_2 . Similarly, when A_2 and B_2 are the same the carry into the third stage does not influence the carry out of the third stage. *Figure 4* shows a method of implementing a 5-input encoder, where the inputs are

equally weighted. The outputs S_0 , S_1 and S_2 present a binary number equal to the number of inputs I_1 – I_5 that are true. *Figure 5* shows one method of implementing a 5-input majority gate. When three or more of the inputs I_1 – I_5 are true, the output M_5 is true.

	C_0	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	S_0	S_1	S_2	S_3	C_4
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH: $0 + 10 + 9 = 3 + 16$ Active LOW: $1 + 5 + 6 = 12 + 0$

FIGURE 1. Active HIGH versus Active LOW Interpretation

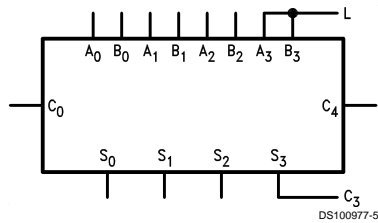


FIGURE 2. 3-Bit Adder

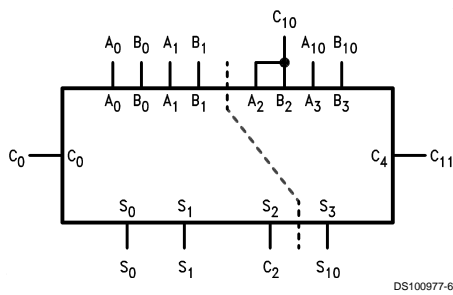


FIGURE 3. 2-Bit and 1-Bit Adders

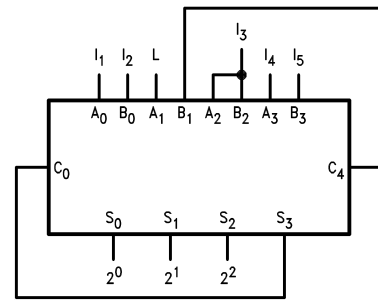


FIGURE 4. 5-Input Encoder

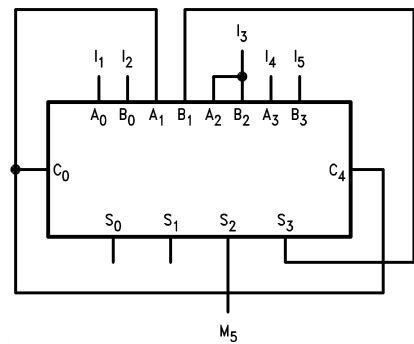
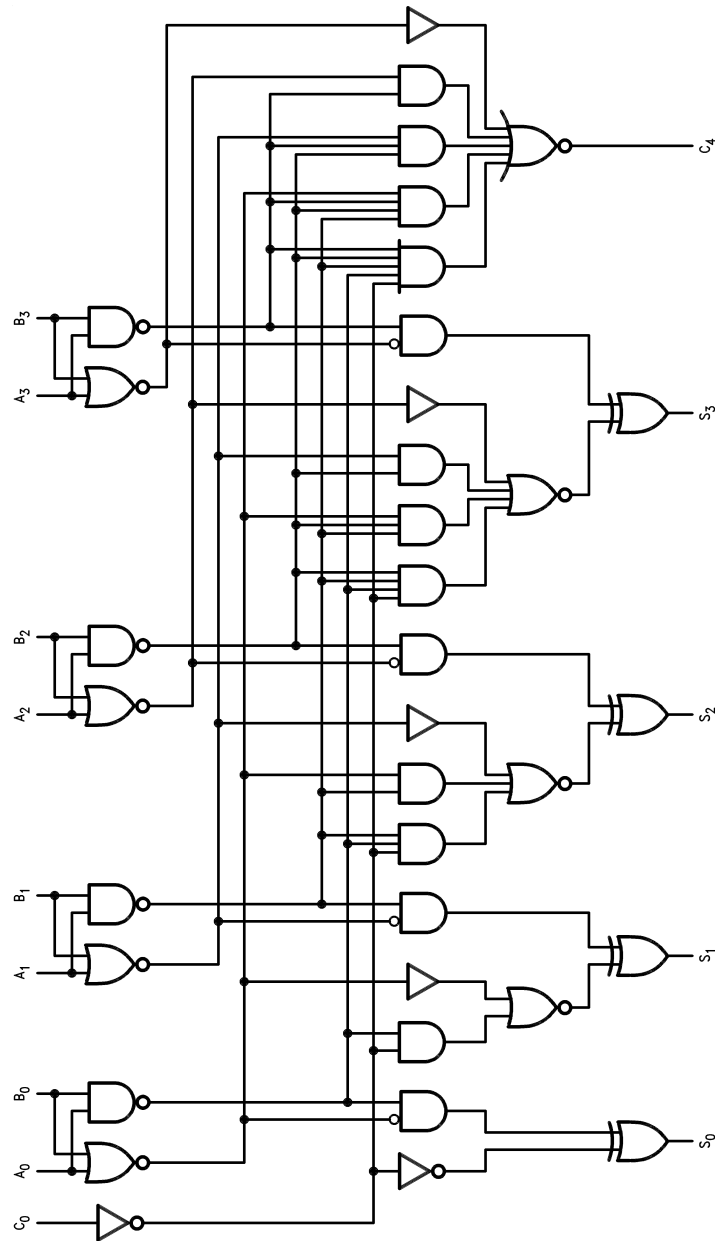


FIGURE 5. 5-Input Majority Gate

Logic Diagram



DS10077-9

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}

3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics for 'ACT Family Devices

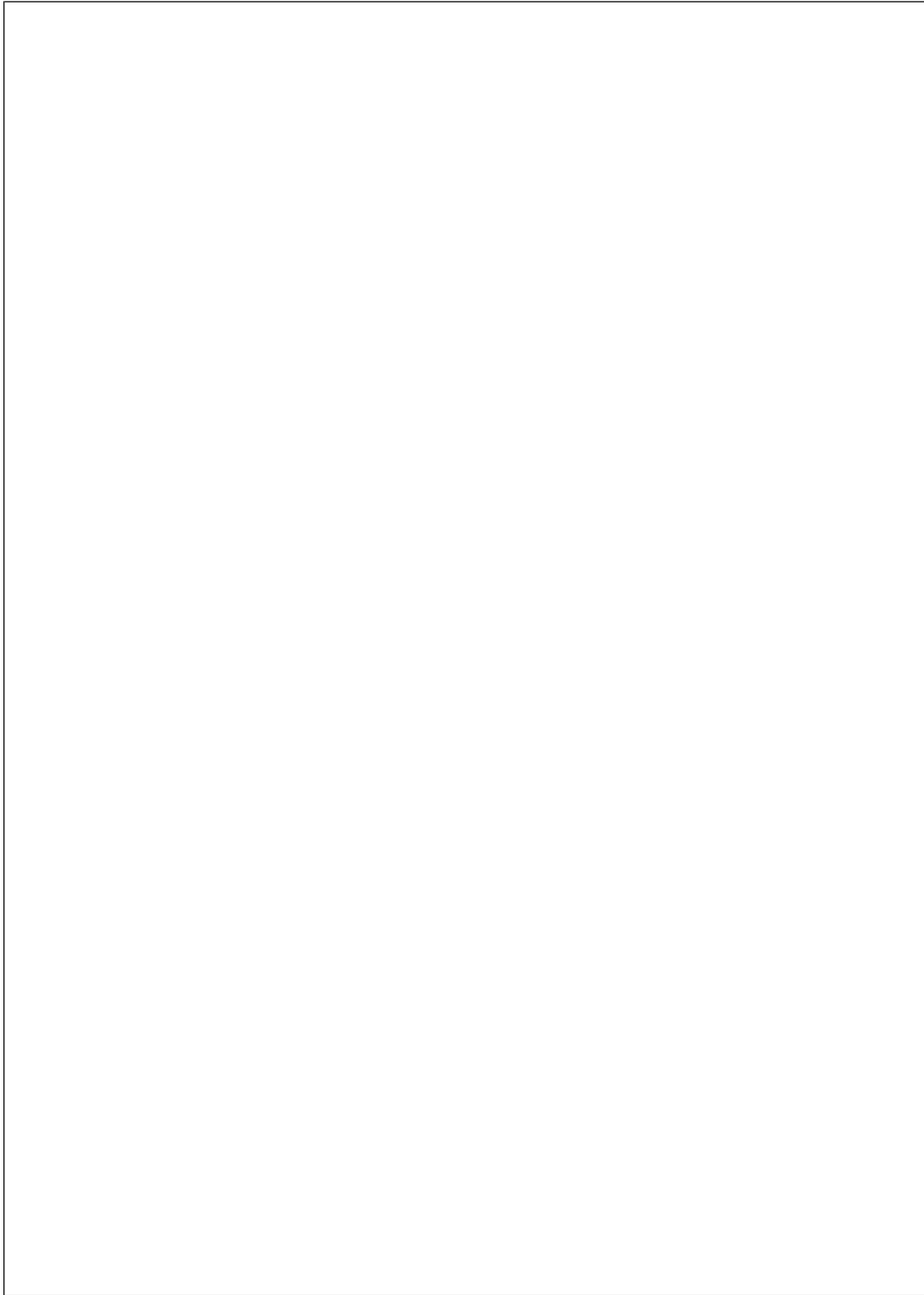
Symbol	Parameter	V _{CC} (V)	T _A = -55°C to +125°C	Units	Conditions	
			Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	4.5	2.0	V	V _{OUT} = 0.1V or V _{CC} - 0.1V	
		5.5	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	0.8	V	V _{OUT} = 0.1V or V _{CC} - 0.1V	
		5.5	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.4	V	I _{OUT} = -50 μA	
		5.5	5.4			
			4.5	3.7	V	V _{IN} = V _{IL} or V _{IH} I _{OH} = -24 mA I _{OH} = -24 mA (Note 3)
			5.5	4.7		
V _{OL}	Maximum Low Level Output Voltage	4.5	0.1	V	I _{OUT} = 50 μA	
		5.5	0.1			
			4.5	0.5	V	V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA I _{OL} = 24 mA (Note 3)
			5.5	0.5		
I _{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	V _I = V _{CC} , GND	
I _{CCT}	Maximum I _{CC} /Input	5.5	1.6	mA	V _I = V _{CC} - 2.1V	
I _{OLD}	Minimum Dynamic Output Current (Note 4)	5.5	50	mA	V _{OLD} = 1.65V Max	
I _{OHD}		5.5	-50	mA	V _{OHD} = 3.85V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5	160.0	μA	V _{IN} = V _{CC} or GND	

Note 3: All outputs loaded; thresholds on input associated with output under test.

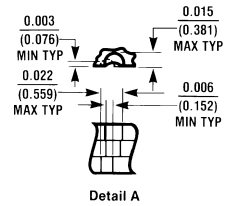
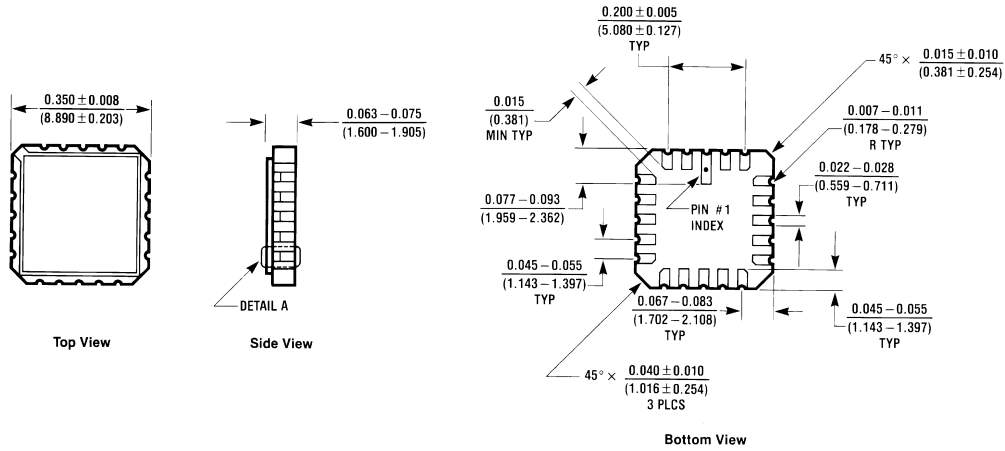
Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for 'ACT Family Devices

Symbol	Parameter	54ACT		Units
		T _A , V _{CC} = Mil C _L = 50 pF		
		Min	Max	
t _{PLH}	Propagation Delay	2.5	14.0	ns
t _{PHL}	C ₀ to S _n	2.5	14.0	
t _{PLH}	Propagation Delay	2.0	17.0	ns
t _{PHL}	A _n or B _n to S _n	2.0	17.0	
t _{PLH}	Propagation Delay	2.5	10.0	ns
t _{PHL}	C ₀ to C ₄	2.5	11.0	
t _{PLH}	Propagation Delay	2.5	10.5	ns
t _{PHL}	A _n or B _n to C ₄	2.5	11.5	

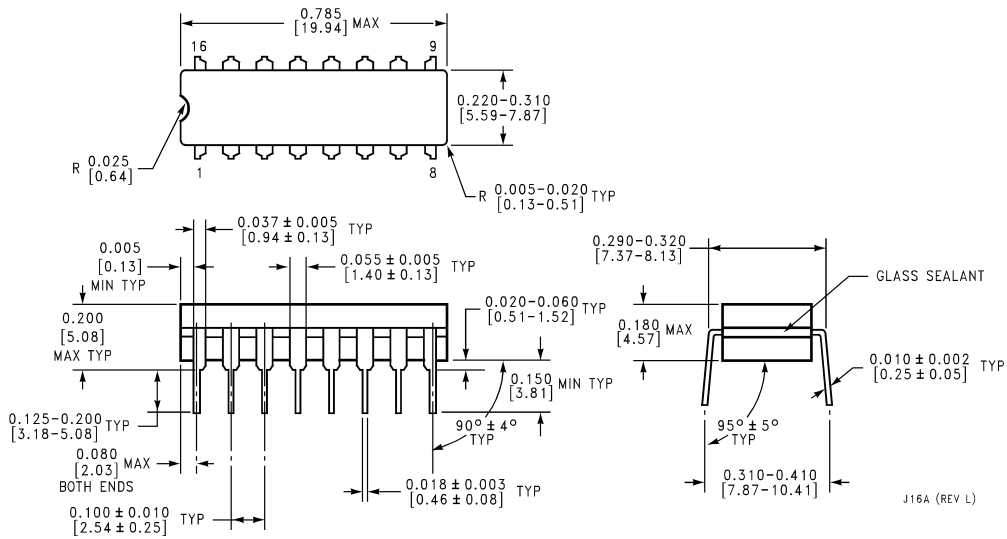


Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Ceramic Leadless Chip Carrier (L)
Package Number E20A**

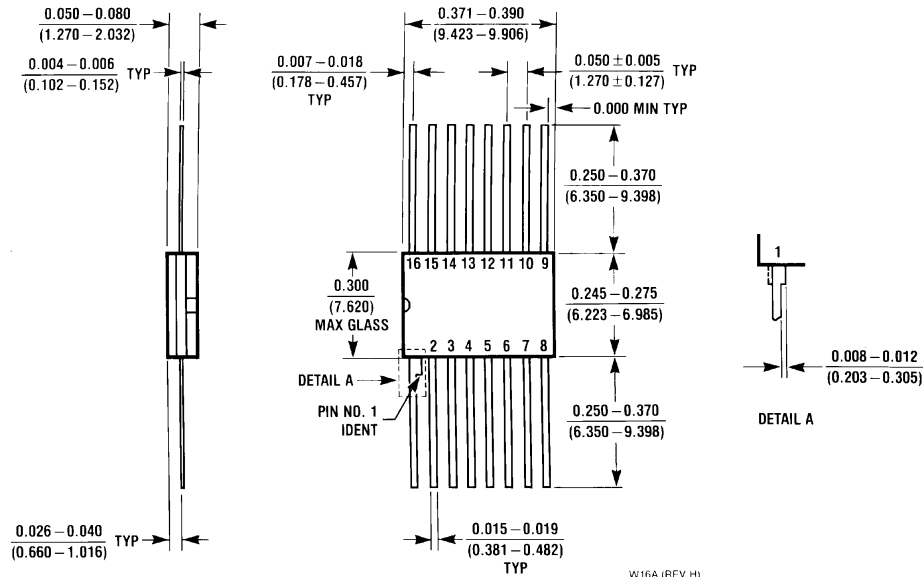
E20A (REV. D)



**16-Lead Ceramic Dual-In-Line Package (D)
Package Number J16A**

J16A (REV. L)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Ceramic Flatpak (F)
Package Number W16A**

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