Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
2. Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons.   It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products.   Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake.   Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.

HD74AC283/HD74ACT283
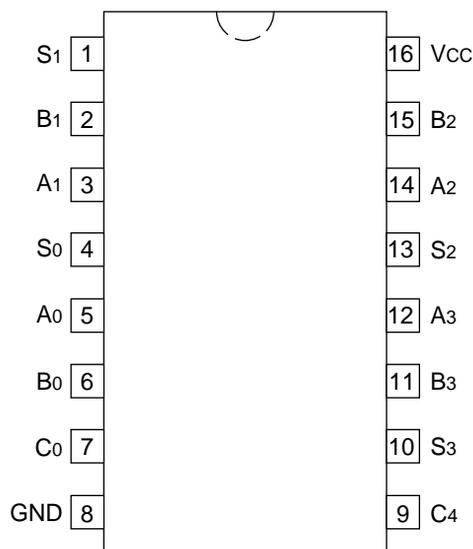
4-bit Binary Full Adder with Fast Carry

RENESAS

Description

The HD74AC283/HD74ACT283 high-speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary works ($A_0 - A_3$, $B_0 - B_3$) and a Carry input (C_0). It generates the binary Sum outputs ($S_0 - S_3$) and the Carry output (C_4) from the most significant bit. The HD74AC283/HD74ACT283 will operate with either active High or active Low operands (positive or negative logic).
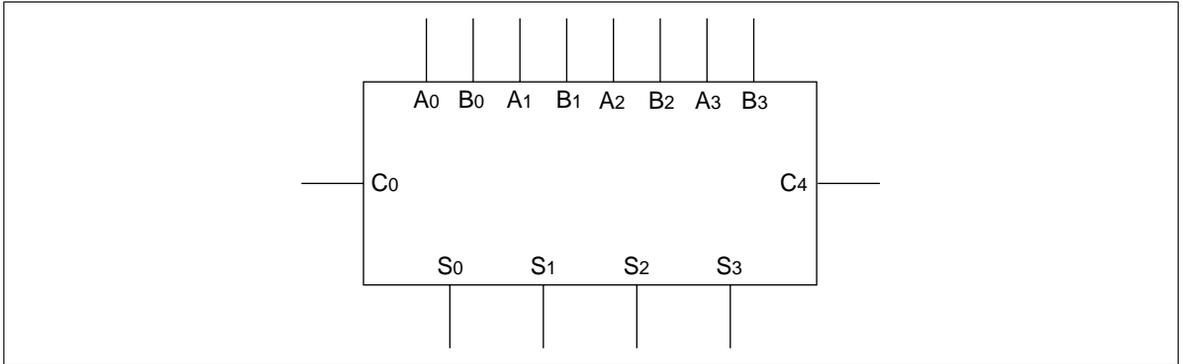
Features

- Outputs Source/Sink 24 mA
- HD74ACT283 has TTL-Cmpatible Inputs

Pin Arrangement

S_1	1	16	Vcc
B_1	2	15	B_2
A_1	3	14	A_2
S_0	4	13	S_2
A_0	5	12	A_3
B_0	6	11	B_3
C_0	7	10	S_3
GND	8	9	C_4

(Top view)

HD74AC283/HD74ACT283

Logic Symbol

Pin Names

$A_0 - A_3$ A Operand Inputs

$B_0 - B_3$ B Operand Inputs

C_0 Carry Input

$S_0 - S_3$ Sum Outputs

C_4 Carry Output

Functional Description

The HD74AC283/HD74ACT283 adds two 4-bit binary words (A plus B) plus the incoming Carry (C_0). The binary sum appears on the Sum ($S_0 - S_3$) and outgoing carry (C_4) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$$2^0 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1) + 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3) = S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$

Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus C_0, A_0, B_0 can be arbitrarily assigned to pins 5, 6 and 7 for DIPS. Due to the symmetry of the binary add function, the HD74AC283/HD74ACT283 can be used either with all inputs and outputs active High (positive logic) or with all inputs and outputs active Low (negative logic). See Figure a. Note that if C_0 is not used it must be tied Low for active High logic or tied High for active Low logic.

Due to pin limitations, the intermediate carries of the HD74AC283/HD74ACT283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. Figure b shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A_3, B_3) Low makes S_3 dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle Figure c shows a way of dividing the HD74AC283/HD74ACT283 into a 2-bit and a 1-bit adder. The third stage adder (A_2, B_2, S_2) is used merely as a means of getting a carry (C_{10}) signal into the fourth stage (via A_2 and B_2) and bringing out the carry from the second stage on S_2. Note that as long as A_2 and B_2 are the same, whether High or Low, they do not influence S_2. Similarly, when A_2 and B_2 are the same the carry into the third stage does not influence the carry out of the third

RENESAS

stage. Figure d shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S_0, S_1 and S_2 present a binary number equal to the number of inputs $I_1 - I_5$ that are true. Figure e shows one method of implementing a 5-input majority gate. When three or more of the inputs $I_1 - I_5$ are true, the output M_5 is true.

Fig. a   Active HIGH varsus Active LOW Interpretation

	C_0	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	S_0	S_1	S_2	S_3	C_4
Logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH: 0 + 10 + 9 = 3 + 16
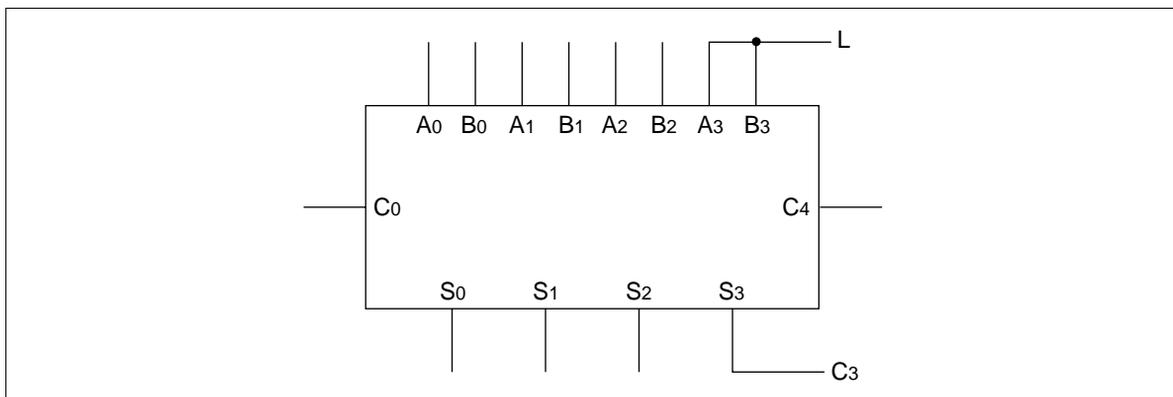Active LOW: 1 + 5 + 6 = 12 + 0

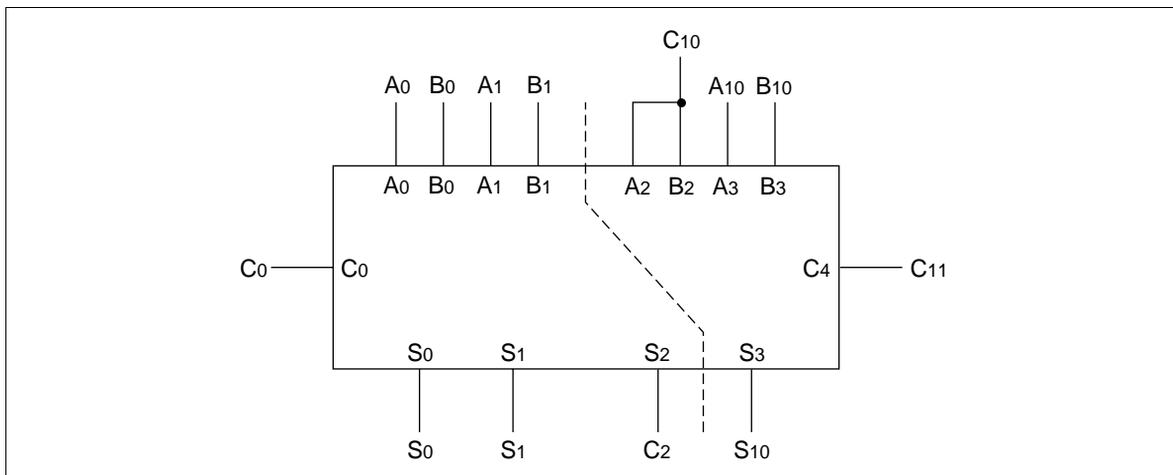

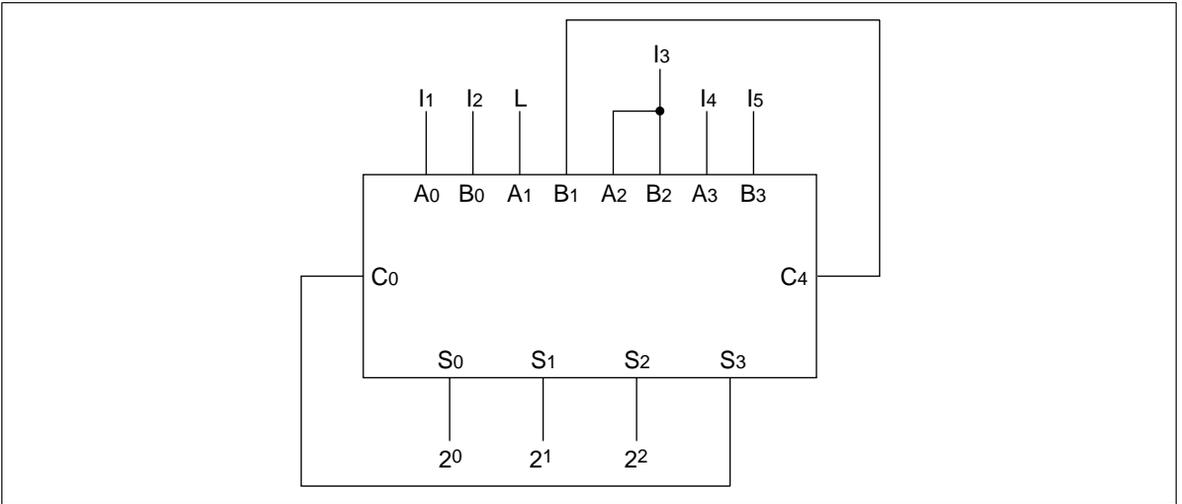**Fig. b   3-bit Adder**

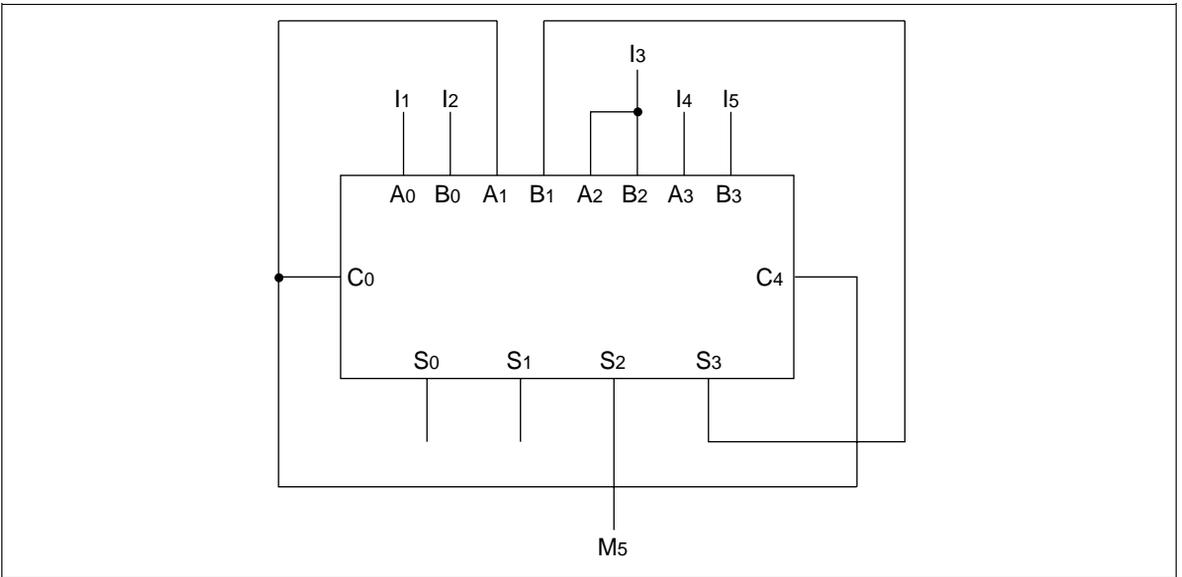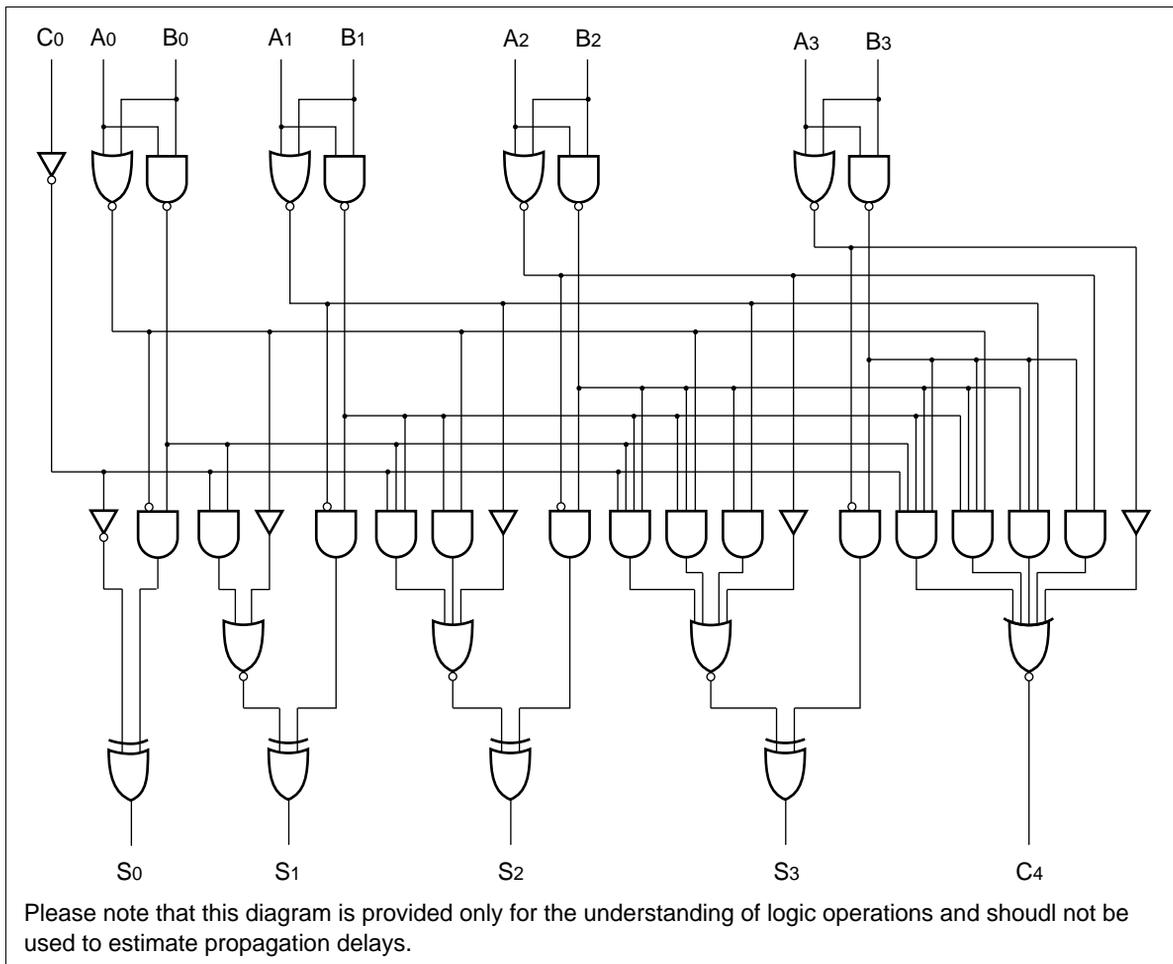**Fig. c   2-bit and 1-bit adders**

Fig. d   5-Input Encoder

Fig. e   5-Input Majority Gate

Logic Diagram

Please note that this diagram is provided only for the understanding of logic operations and shoudl not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	80	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5$ V, Ta = Worst case
Maximum quiescent supply current	I_{CC}	8.0	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5$ V, Ta = $25°$C
Maximum I_{CC}/input (HD74ACT283)	I_{CCT}	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, Ta = Worst case

AC Characteristics: HD74AC283

Item	Symbol	V_{CC} (V)[1]	Ta = +25°C C_L = 50 pF			Ta = −40°C to +85°C C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation delay C_0 to S_n	t_{PLH}	3.3	1.0	11.5	15.0	1.0	16.5	ns
		5.0	1.0	9.5	11.5	1.0	12.5	
Propagation delay C_0 to S_n	t_{PHL}	3.3	1.0	10.5	14.0	1.0	15.5	ns
		5.0	1.0	8.5	10.5	1.0	11.5	
Propagation delay A_n or B_n to S_n	t_{PLH}	3.3	1.0	14.0	17.0	1.0	18.5	ns
		5.0	1.0	11.5	13.5	1.0	14.5	
Propagation delay A_n or B_n to S_n	t_{PHL}	3.3	1.0	13.5	16.5	1.0	18.0	ns
		5.0	1.0	11.0	13.0	1.0	14.0	
Propagation delay C_0 to C_4	t_{PLH}	3.3	1.0	9.5	12.5	1.0	15.5	ns
		5.0	1.0	7.5	9.5	1.0	10.5	
Propagation delay C_0 to C_4	t_{PHL}	3.3	1.0	10.0	13.0	1.0	14.0	ns
		5.0	1.0	8.0	10.0	1.0	11.0	
Propagation delay A_n or B_n to C_4	t_{PLH}	3.3	1.0	11.5	14.5	1.0	16.0	ns
		5.0	1.0	9.5	11.5	1.0	12.5	
Propagation delay A_n or B_n to C_4	t_{PHL}	3.3	1.0	12.0	15.0	1.0	16.5	ns
		5.0	1.0	10.0	12.0	1.0	13.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

RENESAS

AC Characteristics: HD74ACT283

Item	Symbol	V_{CC} (V)*1	Ta = +25°C C_L = 50 pF			Ta = −40°C to +85°C C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation delay C_0 to S_n	t_{PLH}	5.0	1.0	11.5	13.5	1.0	14.5	ns
Propagation delay C_0 to S_n	t_{PHL}	5.0	1.0	10.0	12.0	1.0	13.0	ns
Propagation delay A_n or B_n to S_n	t_{PLH}	5.0	1.0	13.0	15.0	1.0	16.5	ns
Propagation delay A_n or B_n to S_n	t_{PHL}	5.0	1.0	12.0	14.0	1.0	15.5	ns
Propagation delay C_0 to C_4	t_{PLH}	5.0	1.0	9.0	11.0	1.0	12.0	ns
Propagation delay C_0 to C_4	t_{PHL}	5.0	1.0	10.0	12.0	1.0	13.0	ns
Propagation delay A_n or B_n to C_4	t_{PLH}	5.0	1.0	11.0	13.0	1.0	14.0	ns
Propagation delay A_n or B_n to C_4	t_{PHL}	5.0	1.0	11.5	13.5	1.0	14.5	ns

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	V_{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	60.0	pF	V_{CC} = 5.0 V

RENESAS

HD74AC283/HD74ACT283

Package Dimensions

Unit: mm

19.20
20.00 Max

16   9

6.30
7.40 Max

1   8

1.3

1.11 Max

5.06 Max
0.51 Min
2.54 Min

2.54 ± 0.25   0.48 ± 0.10

7.62

$0.25 ^{+0.13}_{-0.05}$

0° − 15°
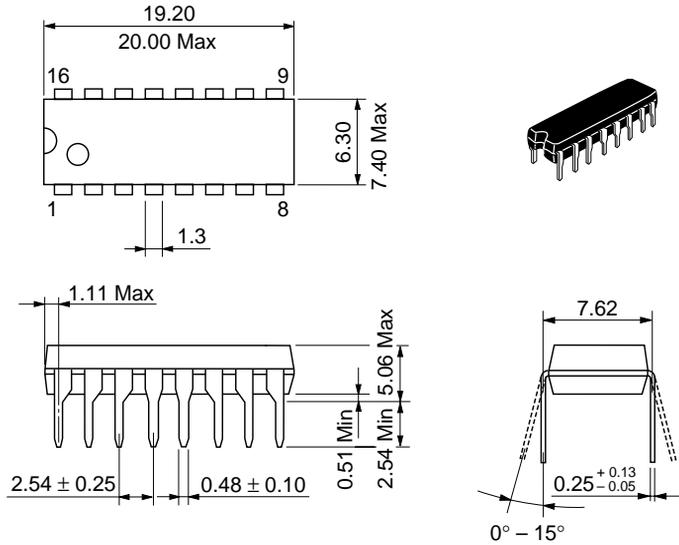
Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	1.07 g

Unit: mm

10.06
10.5 Max

16   9

5.5

1   8

0.80 Max

2.20 Max

1.27

0.10 ± 0.10

*0.42 ± 0.08
0.40 ± 0.06

△ 0.15

⊕ 0.12 Ⓜ

*0.22 ± 0.05
0.20 ± 0.04

$7.80 ^{+0.20}_{-0.30}$

1.15

0° − 8°

0.70 ± 0.20
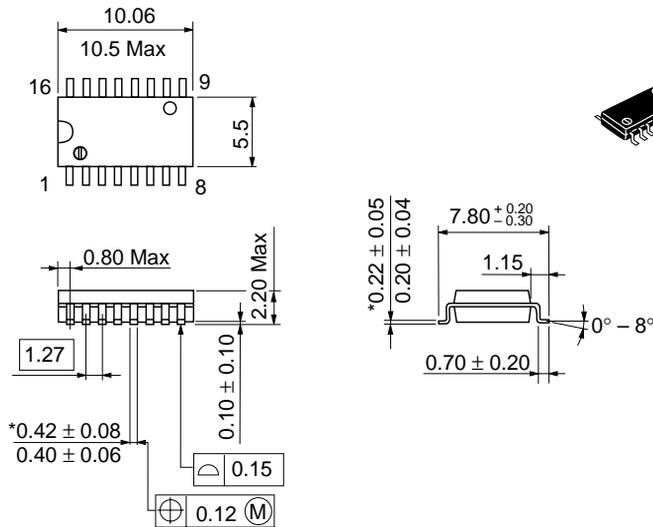
*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.24 g

RENESAS

Unit: mm

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension

Unit: mm

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Mass (reference value)	0.05 g

*Dimension including the plating thickness
Base material dimension

RENESAS

Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.

2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.

3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.

4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.

5. This product is not designed to be radiation resistant.

6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.

7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

RENESAS