National Semiconductor

September 1998

54ACT283
4-Bit Binary Full Adder with Fast Carry

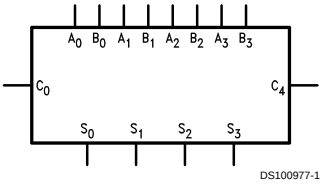
General Description

The 'ACT283 high-speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary words (A_0–A_3, B_0–B_3) and a Carry input (C_0). It generates the binary Sum outputs (S_0–S_3) and the Carry output (C_4) from the most significant bit. The 'ACT283 will operate with either active HIGH or active LOW operands (positive or negative logic).

Features

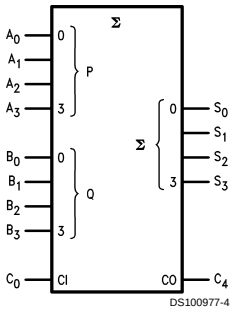
- Guaranteed 4000V minimum ESD protection
- Outputs source/sink 24 mA
- TTL-compatible inputs
- Available to Mil-Std-883

Logic Symbols



DS100977-1

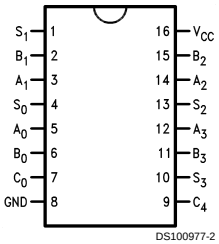
IEEE/IEC



DS100977-4

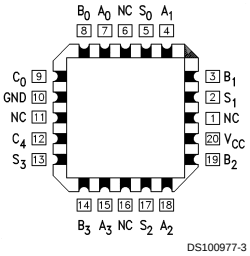
Connection Diagrams

Pin Assignment for DIP and Flatpak



DS100977-2

Pin Assignment for LCC



DS100977-3

Functional Description

The 'ACT283 adds two 4-bit binary words (A plus B) plus the incoming Carry (C_0). The binary sum appears on the Sum (S_0–S_3) and outgoing carry (C_4) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$$2^0 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1) + 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3) = S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$

Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus C_0, A_0, B_0 can be arbitrarily assigned to pins 5, 6 and 7 for DIPS, and 7, 8 and 9 for chip carrier packages. Due to the symmetry of the binary add function, the 'ACT283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). See *Figure 1*. Note that if C_0 is not used it must be tied LOW for active HIGH logic or tied HIGH for active LOW logic.

Due to pin limitations, the intermediate carries of the 'ACT283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. *Figure 2* shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A_3, B_3) LOW makes S_3 dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, *Figure 3* shows a way of dividing the 'ACT283 into a 2-bit and a 1-bit adder. The third stage adder (A_2, B_2, S_2) is used merely as a means of getting a carry (C_{10}) signal into the fourth stage (via A_2 and B_2) and bringing out the carry from the second stage on S_2.

Functional Description (Continued)

Note that as long as A_2 and B_2 are the same, whether HIGH or LOW, they do not influence S_2. Similarly, when A_2 and B_2 are the same the carry into the third stage does not influence the carry out of the third stage. *Figure 4* shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S_0, S_1 and S_2 present a binary number equal to the number of inputs I_1–I_5 that are true. *Figure 5* shows one method of implementing a 5-input majority gate. When three or more of the inputs I_1–I_5 are true, the output M_5 is true.

	C_0	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	S_0	S_1	S_2	S_3	C_4
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH: 0 + 10 + 9 = 3 + 16 Active LOW: 1 + 5 + 6 = 12 + 0

FIGURE 1. Active HIGH versus Active LOW Interpretation

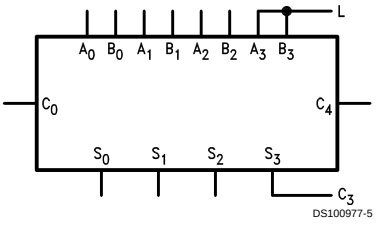


FIGURE 2. 3-Bit Adder

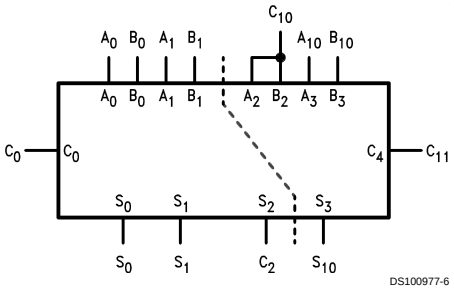


FIGURE 3. 2-Bit and 1-Bit Adders

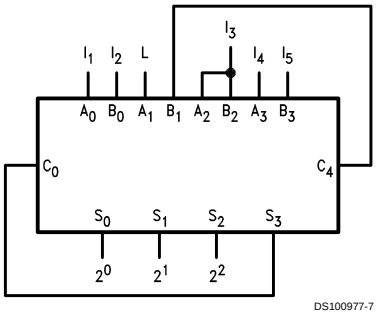


FIGURE 4. 5-Input Encoder

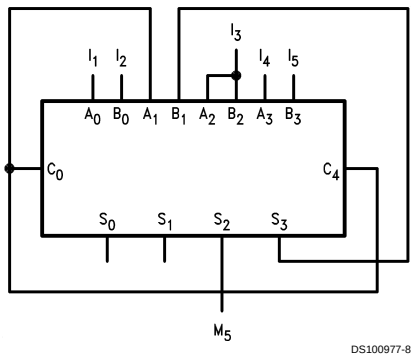
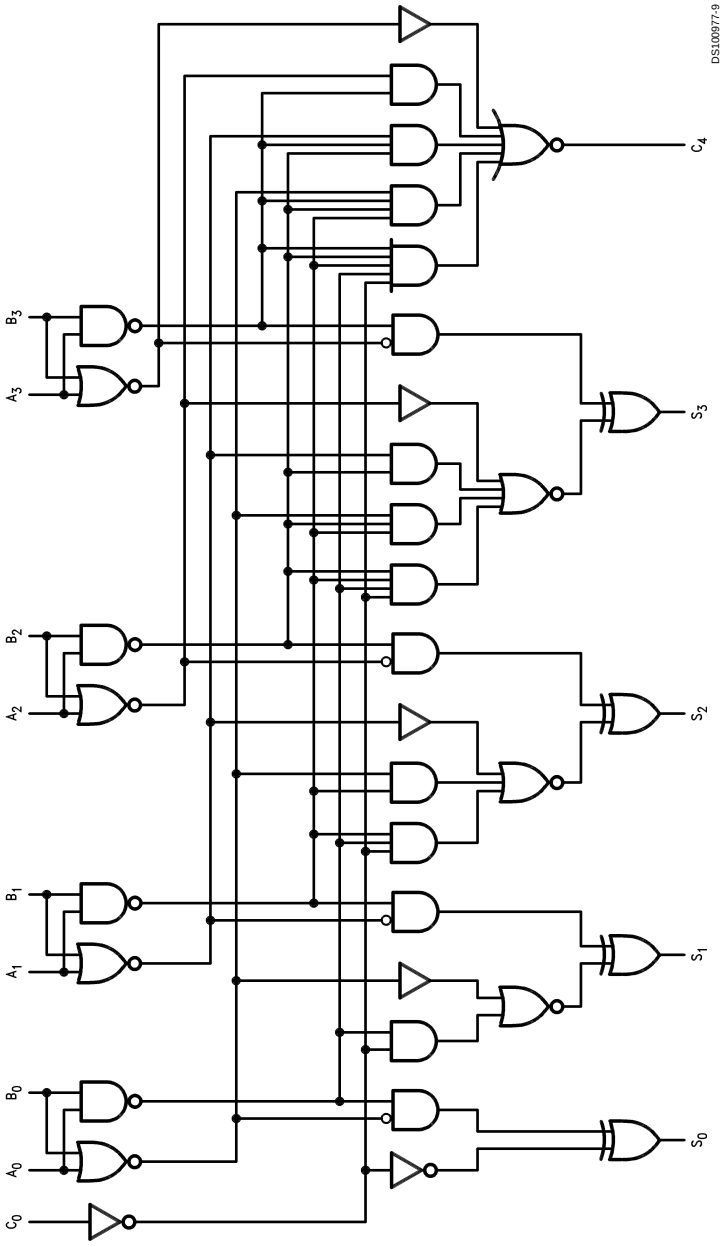


FIGURE 5. 5-Input Majority Gate

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65˚C to +150˚C
Ambient Temperature under Bias	−55˚C to +125˚C
Junction Temperature under Bias	−55˚C to +175˚C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55˚C to +125˚C
Supply Voltage	
Military	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics for 'ACT Family Devices

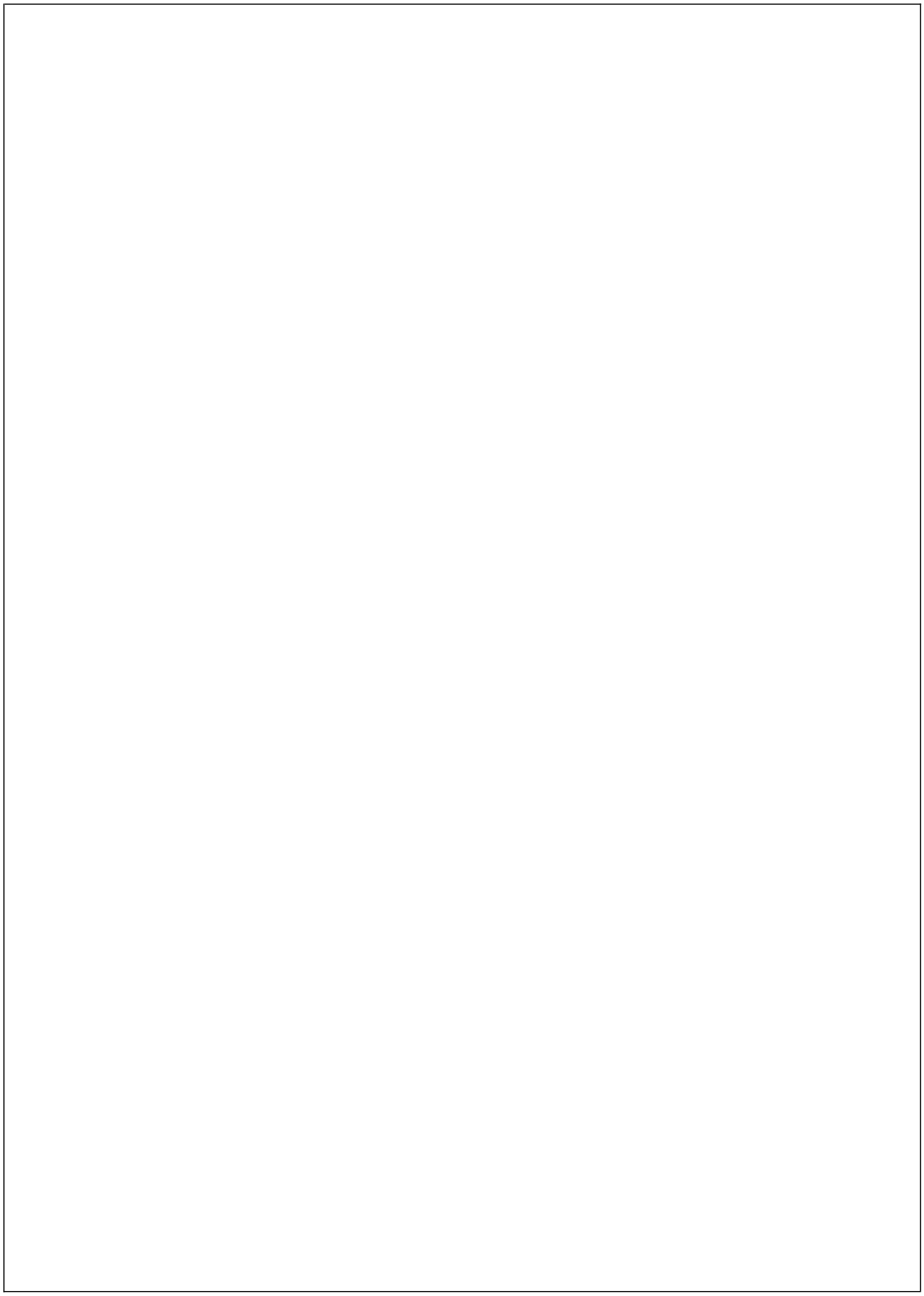
Symbol	Parameter	V_{CC} (V)	T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.4	V	I_{OUT} = −50 µA
		5.5	5.4		
		4.5	3.7	V	V_{IN} = V_{IL} or V_{IH}, I_{OH} = −24 mA
		5.5	4.7		I_{OH} = −24 mA (Note 3)
V_{OL}	Maximum Low Level Output Voltage	4.5	0.1	V	I_{OUT} = 50 µA
		5.5	0.1		
		4.5	0.5	V	V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24 mA
		5.5	0.5		I_{OL} = 24 mA (Note 3)
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	V_I = V_{CC} − 2.1V
I_{OLD}	Minimum Dynamic Output Current (Note 4)	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	160.0	µA	V_{IN} = V_{CC} or GND

Note 3: All outputs loaded; thresholds on input associated with output under test.

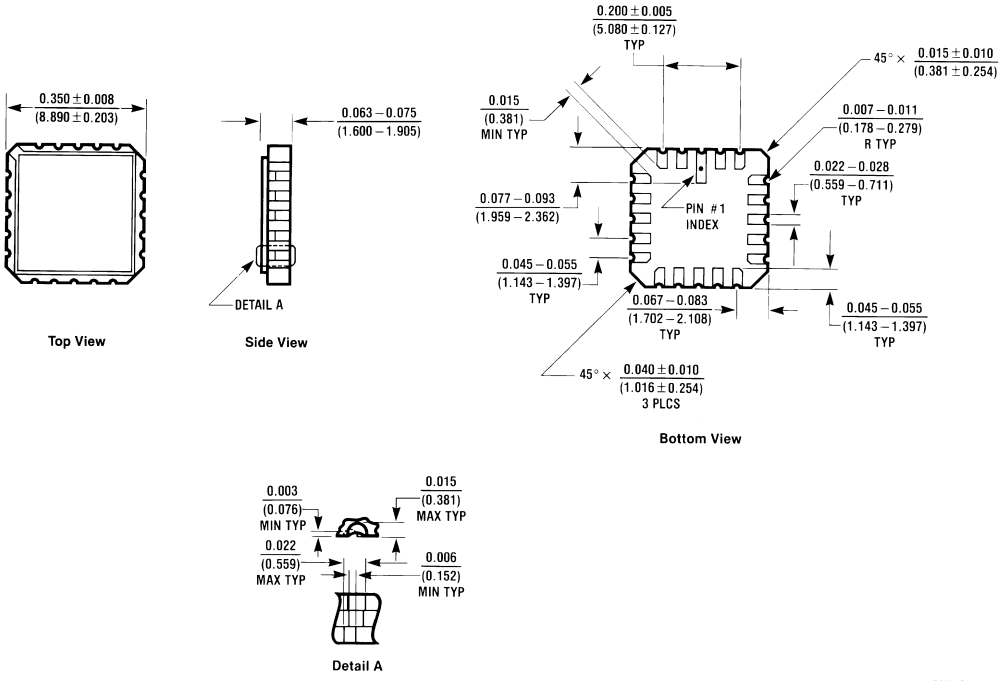
Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for 'ACT Family Devices

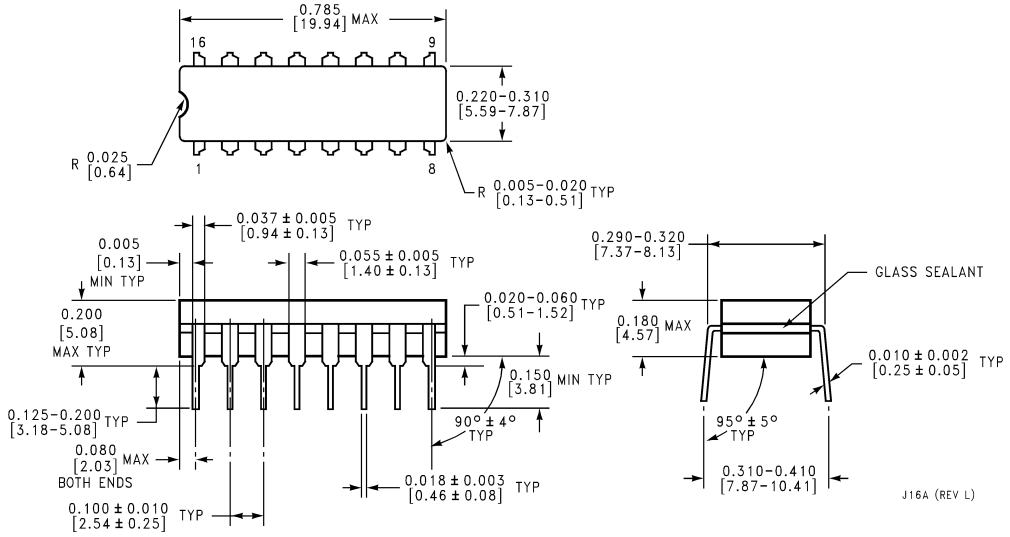
Symbol	Parameter	54ACT T_A, V_{CC} = Mil C_L = 50 pF		Units
		Min	Max	
t_{PLH}	Propagation Delay	2.5	14.0	ns
t_{PHL}	C_0 to S_n	2.5	14.0	
t_{PLH}	Propagation Delay	2.0	17.0	ns
t_{PHL}	A_n or B_n to S_n	2.0	17.0	
t_{PLH}	Propagation Delay	2.5	10.0	ns
t_{PHL}	C_0 to C_4	2.5	11.0	
t_{PLH}	Propagation Delay	2.5	10.5	ns
t_{PHL}	A_n or B_n to C_4	2.5	11.5	



Physical Dimensions inches (millimeters) unless otherwise noted

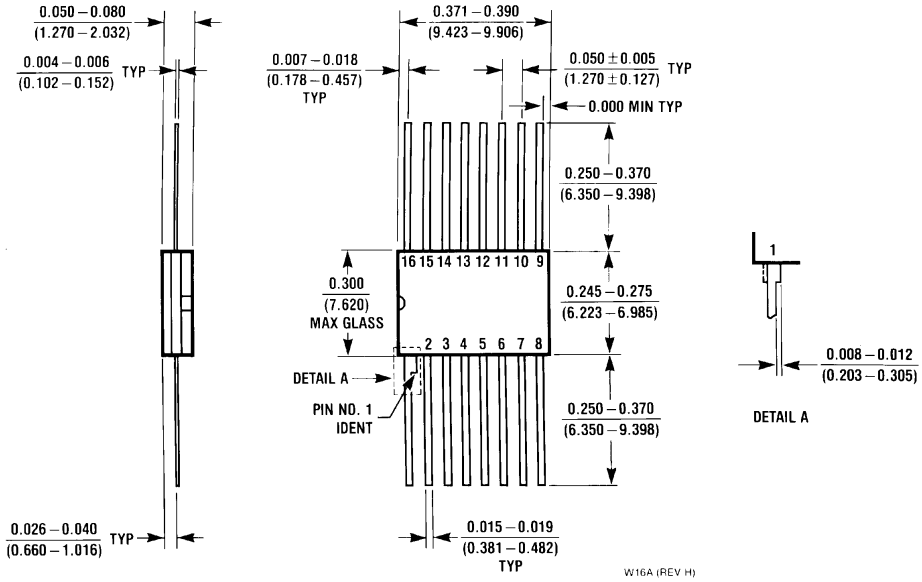


20-Lead Ceramic Leadless Chip Carrier (L)
Package Number E20A



16-Lead Ceramic Dual-In-Line Package (D)
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flatpak (F)
Package Number W16A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179