STK14CA8

128Kx8 AutoStore nvSRAM

Features

- 25[1], 35, 45 ns Read Access and Read/Write Cycle Time
- Unlimited Read/Write Endurance
- Automatic Nonvolatile STORE on Power Loss
- Nonvolatile STORE Under Hardware or Software Control
- Automatic RECALL to SRAM on Power Up
- Unlimited RECALL Cycles
- 200K STORE Cycles
- 20-Year Nonvolatile Data Retention
- Single 3.0V + 20%, -10% Operation
- Commercial and Industrial Temperatures
- Small Footprint SOIC and SSOP Packages (RoHS Compliant)

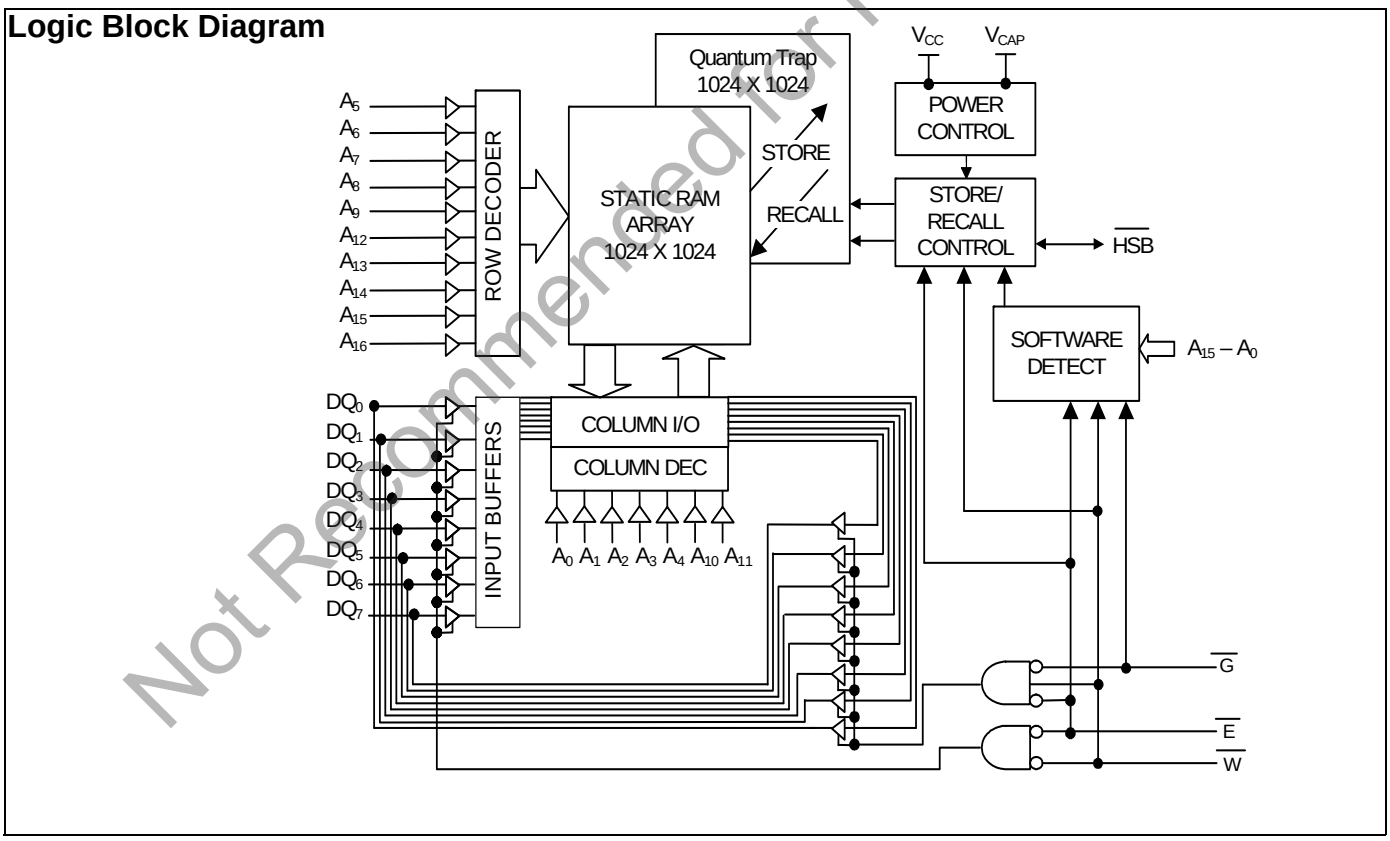
Description

The Cypress STK14CA8 is a 1 Mb fast static RAM with a nonvolatile QuantumTrap storage element included with each memory cell. This SRAM provides fast access and cycle times, ease of use, and unlimited read and write endurance of a normal SRAM.

Data transfers automatically to the nonvolatile storage cells when power loss is detected (the STORE operation). On power up, data is automatically restored to the SRAM (the RECALL operation). Both STORE and RECALL operations are also available under software control.

The Cypress nvSRAM is the first monolithic nonvolatile memory to offer unlimited writes and reads. It is the highest performing and most reliable nonvolatile memory available.

Logic Block Diagram



Note
1. 25 ns speed in Industrial temperature range is over the operating voltage range of 3.3V± 0.3V only.

Contents

Pinouts

Figure 1. 48-Pin SSOP

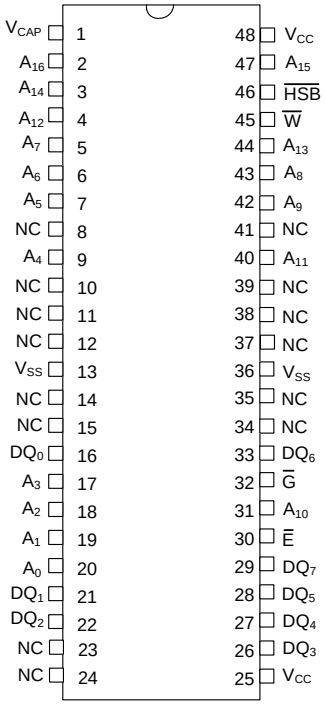


Figure 2. 32-Pin SOIC

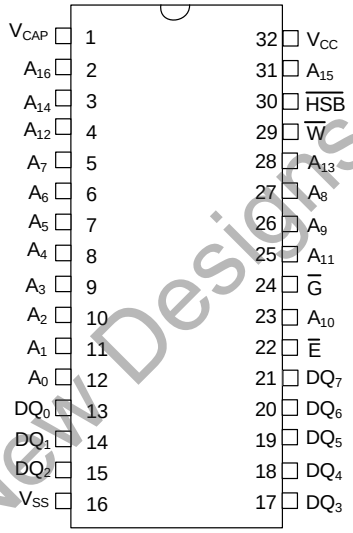
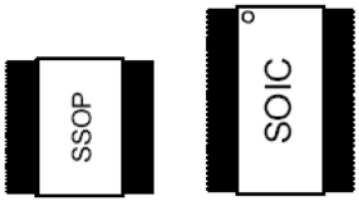


Figure 3. Relative PCB Area Usage[2]



Pin Descriptions

Pin Name	I/O	Description
A_{16}-A_0	Input	Address: The 17 address inputs select one of 131,072 bytes in the nvSRAM array.
DQ_7-DQ_0	I/O	Data: Bi-directional 8-bit data bus for accessing the nvSRAM.
$\overline{E}$	Input	Chip Enable: The active low $\overline{E}$ input selects the device.
$\overline{W}$	Input	Write Enable: The active low $\overline{W}$ allows to write the data on the DQ pins to the address location latched by the falling edge of $\overline{E}$.
$\overline{G}$	Input	Output Enable: The active low $\overline{G}$ input enables the data output buffers during read cycles. De-asserting $\overline{G}$ high causes the DQ pins to tri-state.
V_{CC}	Power Supply	Power: 3.0V, +20%, -10%.
$\overline{HSB}$	I/O	Hardware Store Busy: When low this output indicates a Store is in progress. When pulled low external to the chip, it initiates a nonvolatile STORE operation. A weak pull up resistor keeps this pin high if not connected. (Connection is optional).
V_{CAP}	Power Supply	AutoStore Capacitor: Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile storage elements.
V_{SS}	Power Supply	Ground.
NC	No Connect	Unlabeled pins have no internal connections.

Note
2. See Package Diagrams on page 16 for detailed package size specifications.

Absolute Maximum Ratings

Voltage on Input Relative to Ground.....–0.5V to 4.1V
Voltage on Input Relative to V_{SS}.....–0.5V to (V_{CC} + 0.5V)
Voltage on DQ_{0-7} or $\overline{HSB}$ .....–0.5V to (V_{CC} + 0.5V)
Temperature under Bias ..... –55°C to 125°C
Junction Temperature ..... –55°C to 140°C
Storage Temperature ..... –65°C to 150°C
Power Dissipation 1W
DC Output Current (1 output at a time, 1s duration).... 15 mA

NF (SOP-32) PACKAGE THERMAL CHARACTERISTICS

θ_{jc} 5.4 C/W; θ_{ja} 44.3 [0fpm], 37.9 [200fpm], 35.1 C/W [500fpm].

RF (SSOP-48) PACKAGE THERMAL CHARACTERISTICS

θ_{jc} 6.2 C/W; θ_{ja} 51.1 [0fpm], 44.7 [200fpm], 41.8 C/W [500fpm].

Note: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Characteristics

(V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Commercial		Industrial		Units	Notes
		Min	Max	Min	Max		
I_{CC1}	Average V_{CC} Current		65 55 50		70 60 55	mA mA mA	t_{AVAV} = 25 ns t_{AVAV} = 35 ns t_{AVAV} = 45 ns Dependent on output loading and cycle rate. Values obtained without output loads.
I_{CC2}	Average V_{CC} Current during *STORE*		3		3	mA	All Inputs Don't Care, V_{CC} = max Average current for duration of STORE cycle (t_{STORE})
I_{CC3}	Average V_{CC} Current at t_{AVAV} = 200 ns 3V, 25°C, Typical		10		10	mA	$\overline{W} \geq (V_{CC} - 0.2V)$ All Other Inputs Cycling at CMOS Levels Dependent on output loading and cycle rate. Values obtained without output loads.
I_{CC4}	Average V_{CAP} Current during AutoStore Cycle		3		3	mA	All Inputs Don't Care Average current for duration of STORE cycle (t_{STORE})
I_{SB}	V_{CC} Standby Current (Standby, Stable CMOS Levels)		3		3	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All Others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$ Standby current level after nonvolatile cycle complete
I_{ILK}	Input Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}, $\overline{E}$ or $\overline{G} \geq V_{IH}$
V_{IH}	Input Logic "1" Voltage	2.0	V_{CC}+0.3	2.0	V_{CC}+0.3	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS}–0.5	0.8	V_{SS}–0.5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} =–2 mA
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 4 mA
T_A	Operating Temperature	0	70	–40	85	°C	
V_{CC}	Operating Voltage	2.7	3.6	2.7	3.6	V	3.0V +20%, -10%
V_{CAP}	Storage Capacitance	17	120	17	120	µF	Between V_{CAP} pin and V_{SS}, 5V rated.
NV_C	Nonvolatile STORE operations	200		200		K	
$DATA_R$	Data Retention	20		20		Years	At 55 °C

Note The $\overline{HSB}$ pin has I_{OUT}=-10 uA for V_{OH} of 2.4 V, this parameter is characterized but not tested.

AC Test Conditions

Input Pulse Levels .....0V to 3V
Input Rise and Fall Times ..... ≤ 5 ns
Input and Output Timing Reference Levels 1.5V
Output Load.....See Figure 4 and Figure 5

Capacitance

(T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter[3]	Max	Units	Conditions
C_{IN}	Input Capacitance	7	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Figure 4. AC Output Loading

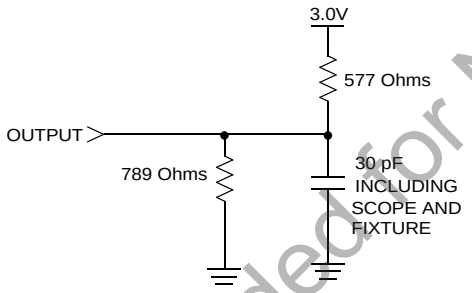
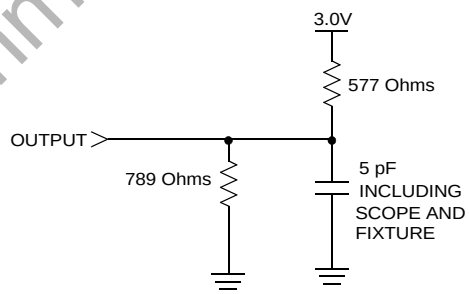


Figure 5. AC Output Loading for Tristate Specifications (t_{HZ}, t_{LZ}, t_{WLQZ}, t_{WHQZ}, t_{GLQX}, t_{GHQZ})



Note
3. These parameters are guaranteed but not tested.

SRAM READ Cycles #1 and #2

NO.	Symbols			Parameter	STK14CA8-25[1]		STK14CA8-35		STK14CA8-45		Units
	#1	#2	Alt.		Min	Max	Min	Max	Min	Max	
1		t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns
2	t_{AVAV}[4]	t_{ELEH}[4]	t_{RC}	Read Cycle Time	25		35		45		ns
3	t_{AVQV}[5]	t_{AVQV}[5]	t_{AA}	Address Access Time		25		35		45	ns
4		t_{GLQV}	t_{OE}	Output Enable to Data Valid		12		15		20	ns
5	t_{AXQX}[5]	t_{AXQX}[5]	t_{OH}	Output Hold after Address Change	3		3		3		ns
6		t_{ELQX}	t_{LZ}	Address Change or Chip Enable to Output Active	3		3		3		ns
7		t_{EHQZ}[6]	t_{HZ}	Address Change or Chip Disable to Output Inactive		10		13		15	ns
8		t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9		t_{GHQZ}[6]	t_{OHZ}	Output Disable to Output Inactive		10		13		15	ns
10		t_{ELICCH}[3]	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11		t_{EHICCL}[3]	t_{PS}	Chip Disable to Power Standby		25		35		45	ns

Figure 6. SRAM READ Cycle #1: Address Controlled[4, 5, 7]

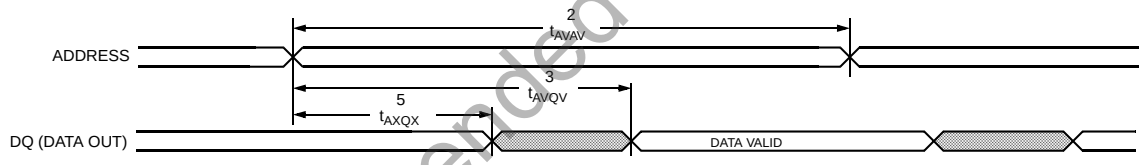
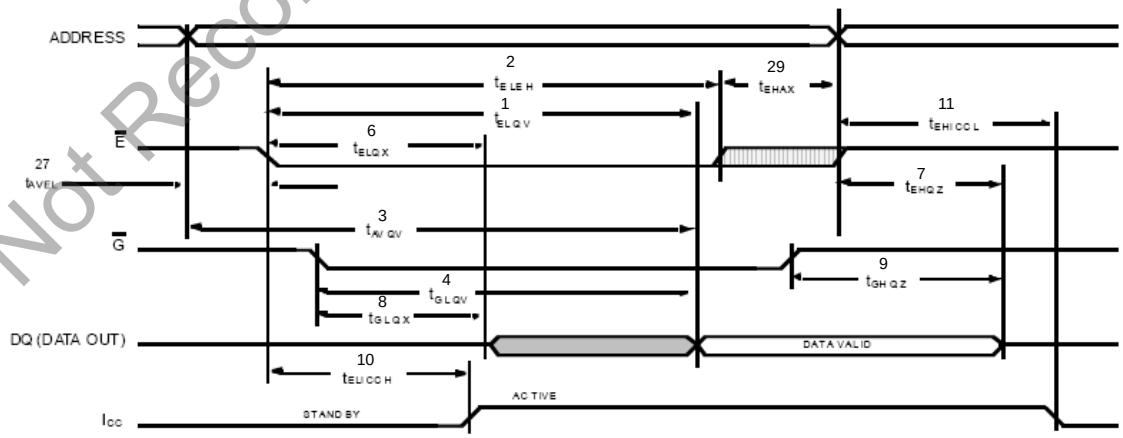


Figure 7. SRAM READ Cycle #2: $\overline{E}$ and $\overline{G}$ Controlled[4, 7]



Notes
4. $\overline{W}$ must be high during SRAM READ cycles.
5. Device is continuously selected with $\overline{E}$ and $\overline{G}$ both low
6. Measured ± 200mV from steady state output voltage.
7. $\overline{HSB}$ must remain high during READ and WRITE cycles

SRAM WRITE Cycles #1 and #2

NO.	Symbols			Parameter	STK14CA8-25[1]		STK14CA8-35		STK14CA8-45		Units
	#1	#2	Alt.		Min	Max	Min	Max	Min	Max	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Setup to End of Write	10		12		15		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Setup to End of Write	20		25		30		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Setup to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		0		0		ns
20	t_{WLQZ}[6,8]		t_{WZ}	Write Enable to Output Disable		10		13		15	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write	3		3		3		ns

Figure 8. SRAM WRITE Cycle #1: $\overline{W}$ Controlled[8,9]

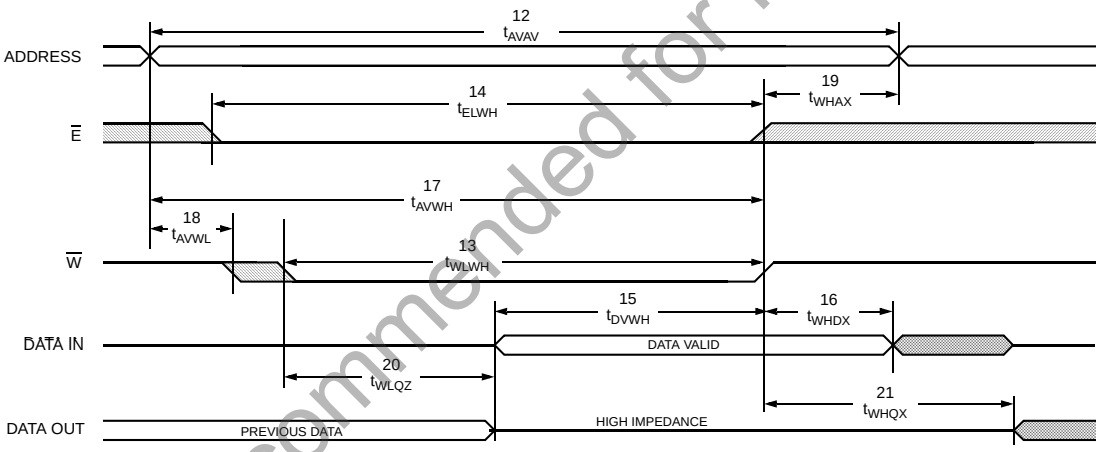
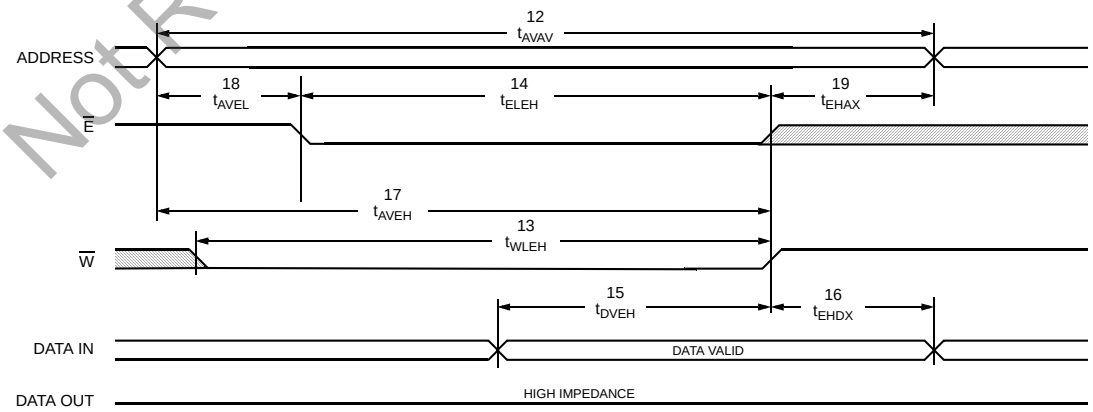


Figure 9. SRAM WRITE Cycle #2: $\overline{E}$ Controlled[8,9]

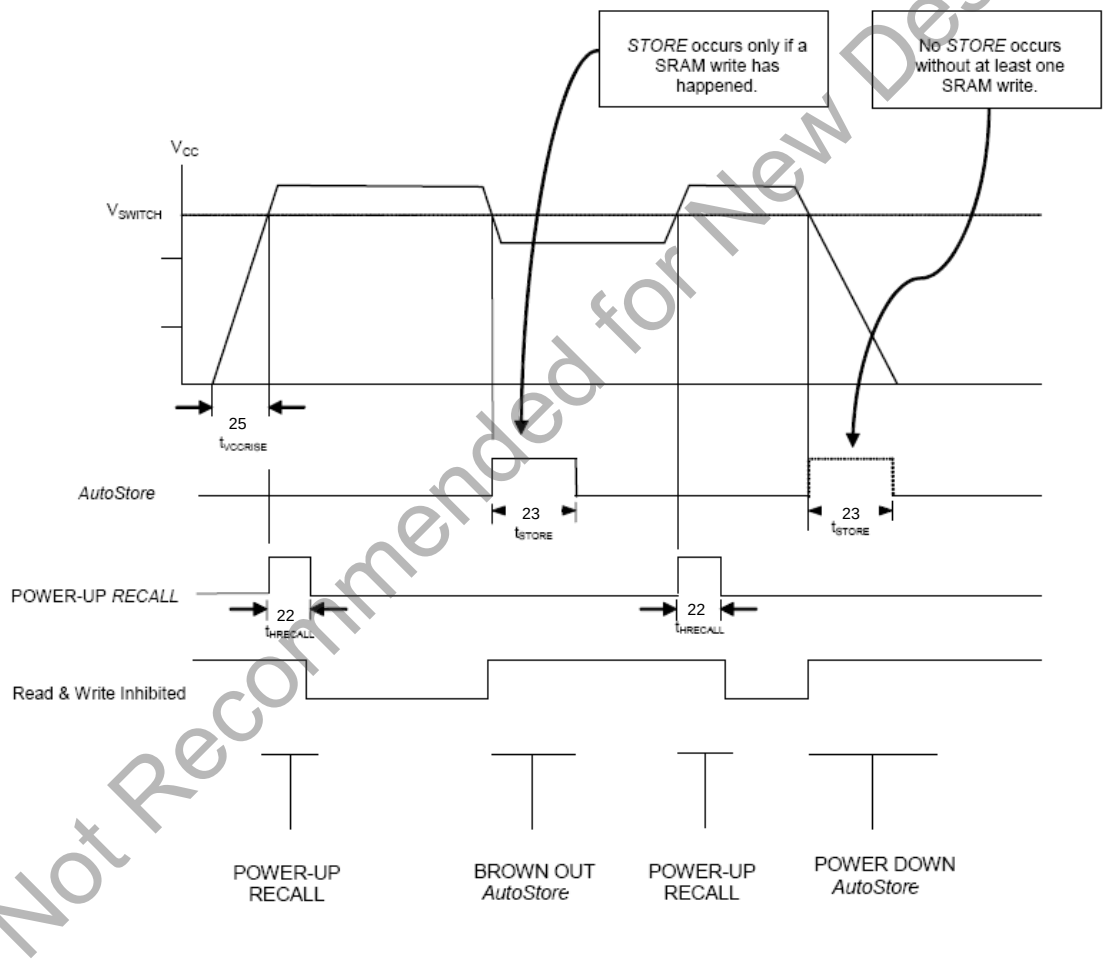


Notes
8. If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
9. $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.

AutoStore/POWER UP RECALL

NO.	Symbols		Parameter	STK14CA8		Units	Notes
	Standard	Alternate		Min	Max		
22	$t_{HRECALL}$		Power up RECALL Duration		20	ms	10
23	t_{STORE}	t_{HLHZ}	STORE Cycle Duration		12.5	ms	11, 12
24	V_{SWITCH}		Low Voltage Trigger Level		2.65	V	
25	V_{CCRISE}		V_{CC} Rise Time	150		µs	

Figure 10. AutoStore/POWER UP RECALL



Note Read and Write cycles are ignored during STORE, RECALL, and while V_{CC} is below V_{SWITCH}.

Notes
10. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}
11. If an SRAM WRITE has not taken place since the last nonvolatile cycle, no STORE takes place
12. Industrial Grade devices require maximum 15 ms.

Software Controlled STORE/RECALL Cycle

NO.	Symbols			Parameter[13,14]	STK14CA8-25[1]		STK14CA8-35		STK14CA8-45		Units	Notes
	$\overline{E}$ Cont	$\overline{G}$ Cont	Alt		Min	Max	Min	Max	Min	Max		
26	t_{AVAV}	t_{AVAV}	t_{RC}	STORE/RECALL Initiation Cycle Time	25		35		45		ns	14
27	t_{AVEL}	t_{AVGL}	t_{AS}	Address Setup Time	0		0		0		ns	
28	t_{ELEH}	t_{GLGH}	t_{CW}	Clock Pulse Width	20		25		30		ns	
29	t_{EHAX}	t_{GHAX}		Address Hold Time	1		1		1		ns	
30	t_{RECALL}	t_{RECALL}		RECALL Duration		50		50		50	µs	

Figure 11. Software STORE/RECALL CYCLE: $\overline{E}$ Controlled[14]

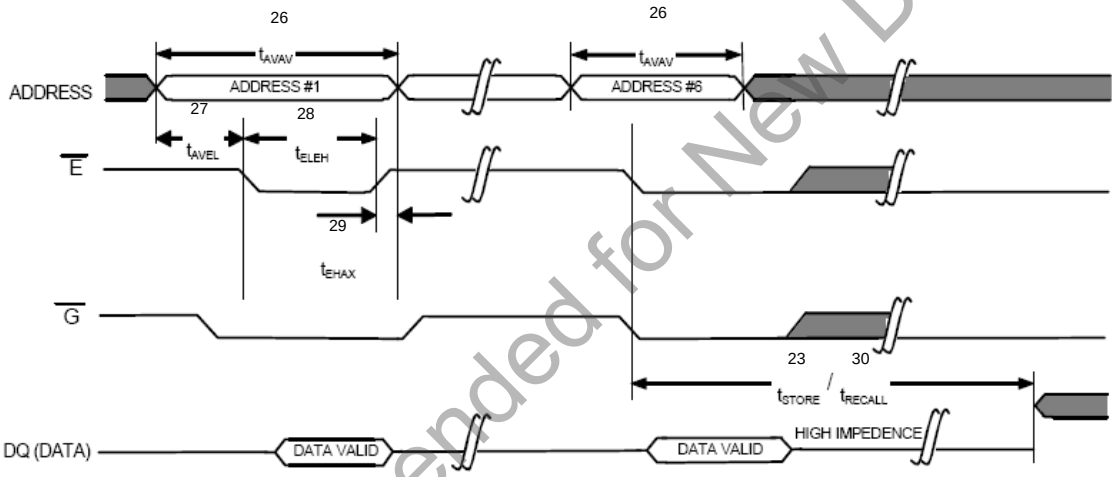
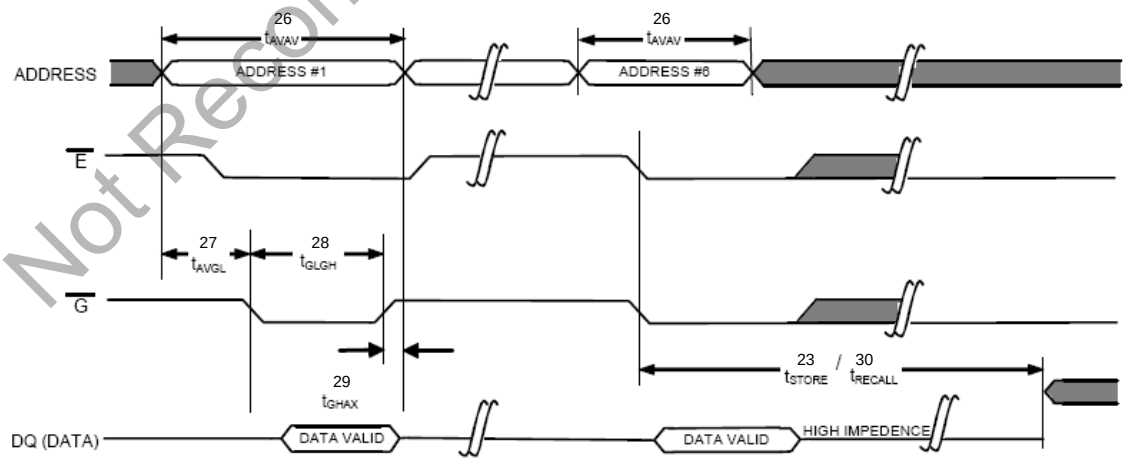


Figure 12. Software STORE/RECALL CYCLE: $\overline{G}$ Controlled[14]

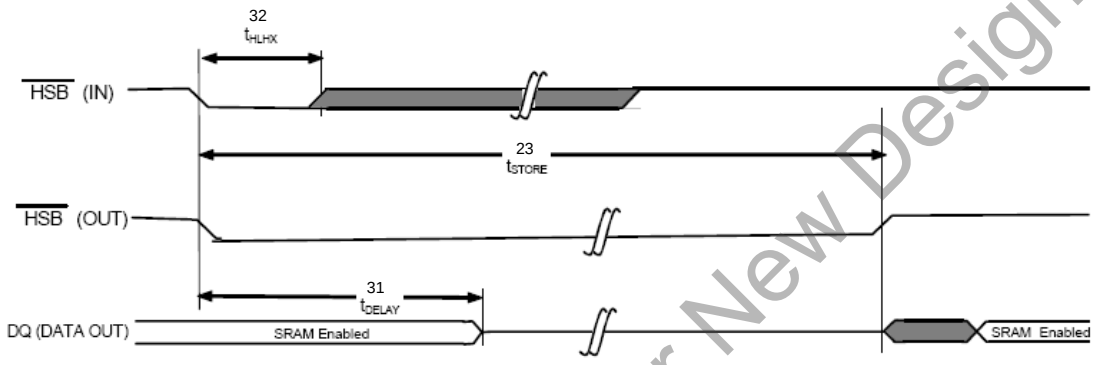


Notes
13. The software sequence is clocked on the falling edge of $\overline{E}$ controlled READs or $\overline{G}$ controlled READs
14. The six consecutive addresses must be read in the order listed in the Software STORE/RECALL Mode Selection Table. $\overline{W}$ must be high during all six consecutive cycles.

Hardware STORE Cycle

NO.	Symbols		Parameter	STK14CA8		Units	Notes
	Standard	Alternate		Min	Max		
31	t_{DELAY}	t_{HLQZ}	Hardware STORE to SRAM Disabled	1	70	µs	15
32	t_{HLHX}		Hardware STORE Pulse Width	15		ns	

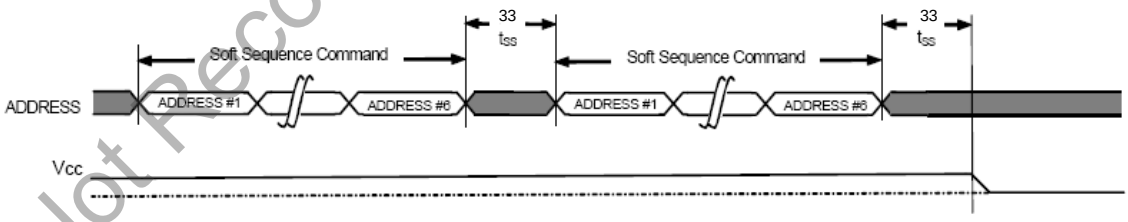
Figure 13. Hardware STORE Cycle



Soft Sequence Commands

NO.	Symbols	Parameter	STK14CA8		Units	Notes
	Standard		Min	Max		
33	t_{SS}	Soft Sequence Processing Time		70	µs	16, 17

Figure 14. Software Sequence Commands



Notes
15. On a hardware STORE initiation, SRAM operation continues to be enabled for time t_{DELAY} to allow read/write cycles to complete.
16. This is the amount of time that it takes to take action on a soft sequence command. Vcc power must remain high to effectively register command.
17. Commands such as Store and Recall lock out I/O until operation is complete which further increases this time. See specific command.

Mode Selection

$\overline{E}$	$\overline{W}$	$\overline{G}$	A_{16}-A_0	Mode	I/O	Power	Notes
H	X	X	X	Not Selected	Output High Z	Standby	
L	H	L	X	Read SRAM	Output Data	Active	
L	L	X	X	Write SRAM	Input Data	Active	
L	H	L	0x04E38 0x0B1C7 0x083E0 0x07C1F 0x0703F 0x08B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Disable	Output Data Output Data Output Data Output Data Output Data Output Data	Active	18, 19, 20
L	H	L	0x04E38 0x0B1C7 0x083E0 0x07C1F 0x0703F 0x04B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Enable	Output Data Output Data Output Data Output Data Output Data Output Data	Active	18, 19, 20
L	H	L	0x04E38 0x0B1C7 0x083E0 0x07C1F 0x0703F 0x08FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Store	Output Data Output Data Output Data Output Data Output Data Output High Z	Active I_{CC2}	18, 19, 20
L	H	L	0x04E38 0x0B1C7 0x083E0 0x07C1F 0x0703F 0x04C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Recall	Output Data Output Data Output Data Output Data Output Data Output High Z	Active	18, 19, 20

Notes
18. The six consecutive addresses must be in the order listed. $\overline{W}$ must be high during all six consecutive cycles to enable a nonvolatile cycle.
19. While there are 17 addresses on the STK14CA8, only the lower 16 are used to control software modes
20. I/O state depends on the state of $\overline{G}$. The I/O table shown assumes $\overline{G}$ low

nvSRAM Operation

nvSRAM

The STK14CA8 nvSRAM has two functional components paired in the same physical cell. These are the SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates similar to a standard fast static RAM. Data in the SRAM can be transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture allows all cells to be stored and recalled in parallel. During the STORE and RECALL operations, SRAM READ and WRITE operations are inhibited. The STK14CA8 supports unlimited read and writes similar to a typical SRAM. In addition, it provides unlimited RECALL operations from the nonvolatile cells and up to 200K STORE operations.

SRAM READ

The STK14CA8 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low while $\overline{W}$ and $\overline{HSB}$ are high. The address specified on pins A_{0-16} determine which of the 131,072 data bytes are accessed. When the READ is initiated by an address transition, the outputs are valid after a delay of t_{AVQV} (READ cycle #1). If the READ is initiated by $\overline{E}$ and $\overline{G}$, the outputs are valid at t_{ELQV} or at t_{GLQV}, whichever is later (READ cycle #2). The data outputs repeatedly responds to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and remains valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high, or $\overline{W}$ and $\overline{HSB}$ is brought low.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low and $\overline{HSB}$ is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on the common I/O pins DQ0-7 are written into memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{G}$ is left low, internal circuitry turns off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

AutoStore Operation

The STK14CA8 stores data to nvSRAM using one of three storage operations. These three operations are Hardware Store (activated by HSB), Software Store (activated by an address sequence), and AutoStore (on power down).

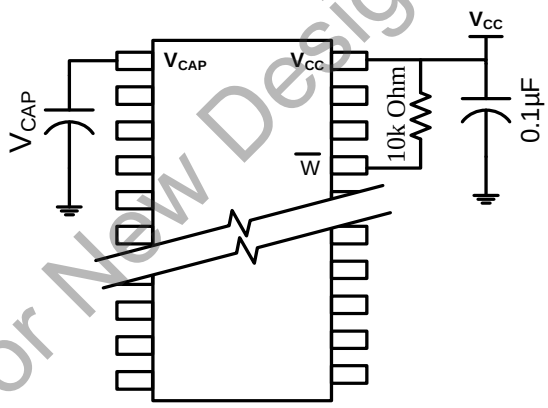
AutoStore operation is a unique feature of Cypress Quantum Trap technology is enabled by default on the STK14CA8.

During normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC}. A STORE operation is initiated with power provided by the V_{CAP} capacitor.

Figure 15 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. Refer to DC Characteristics on page 4 for the size of the capacitor. The voltage on the V_{CAP} pin is driven to 5V by a charge pump internal to the chip. A pull up should be placed on $\overline{W}$ to hold it inactive during power up.

To reduce unneeded nonvolatile stores, AutoStore and Hardware Store operations are ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place. The $\overline{HSB}$ signal can be monitored by the system to detect an AutoStore cycle is in progress.

Figure 15. AutoStore Mode



Hardware STORE ($\overline{HSB}$) Operation

The STK14CA8 provides the $\overline{HSB}$ pin for controlling and acknowledging the STORE operations. The $\overline{HSB}$ pin is used to request a hardware STORE cycle. When the $\overline{HSB}$ pin is driven low, the STK14CA8 conditionally initiates a STORE operation after t_{DELAY}. An actual STORE cycle only begins if a WRITE to the SRAM took place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin has a very resistive pull up and is internally driven low to indicate a busy condition while the STORE (initiated by any means) is in progress. This pin should be externally pulled up if it is used to drive other inputs.

SRAM READ and WRITE operations that are in progress when $\overline{HSB}$ is driven low by any means are given time to complete before the STORE operation is initiated. After $\overline{HSB}$ goes low, the STK14CA8 continues to allow SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM READ operations may take place. If a WRITE is in progress when $\overline{HSB}$ is pulled low, it is allowed a time t_{DELAY} to complete. However, any SRAM WRITE cycles requested after $\overline{HSB}$ goes low are inhibited until $\overline{HSB}$ returns high.

If $\overline{HSB}$ is not used, it should be left unconnected.

Hardware RECALL (Power Up)

During power up or after any low power condition (V_{CC}<V_{SWITCH}), an internal RECALL request is latched. When V_{CC} again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete.

Software STORE

Data can be transferred from the SRAM to the nonvolatile memory by a software address sequence. The STK14CA8 software STORE cycle is initiated by executing sequential $\overline{E}$ controlled or $\overline{G}$ controlled READ cycles from six specific address locations in exact order. During the STORE cycle, previous data is erased and then the new data is programmed into the nonvolatile elements. After a STORE cycle is initiated, further memory inputs and outputs are disabled until the cycle is completed.

To initiate the software STORE cycle, the following READ sequence must be performed:

Read Address	0x4E38	Valid READ
Read Address	0xB1C7	Valid READ
Read Address	0x83E0	Valid READ
Read Address	0x7C1F	Valid READ
Read Address	0x703F	Valid READ
Read Address	0x8FC0	Initiate STORE Cycle

When the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. It is important that READ cycles and not WRITE cycles be used in the sequence and that $\overline{G}$ is active. After the t_{STORE} cycle time is fulfilled, the SRAM is again activated for READ and WRITE operation.

Software RECALL

Data can be transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of $\overline{E}$ controlled or $\overline{G}$ controlled READ operations must be performed:

Read Address	0x4E38	Valid READ
Read Address	0xB1C7	Valid READ
Read Address	0x83E0	Valid READ
Read Address	0x7C1F	Valid READ
Read Address	0x703F	Valid READ
Read Address	0x4C63	Initiate RECALL Cycle

Internally, RECALL is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is again ready for READ or WRITE operations. The RECALL operation in no way alters the data in the nonvolatile storage elements.

Data Protection

The STK14CA8 protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low voltage condition is detected when V_{CC}<V_{SWITCH}.

If the STK14CA8 is in a WRITE mode (both $\overline{E}$ and $\overline{W}$ low) at power up, after a RECALL, or after a STORE, the WRITE is inhibited until a negative transition on $\overline{E}$ or $\overline{W}$ is detected. This protects against inadvertent writes during power up or brown out conditions.

Noise Considerations

The STK14CA8 is a high speed memory and so must have a high frequency bypass capacitor of approximately 0.1 µF connected between V_{CC} and V_{SS}, using leads and traces that are a short as possible. As with all high speed CMOS ICs, careful routing of power, ground, and signals reduce circuit noise.

Best Practices

nvSRAM products have been used effectively for over 15 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

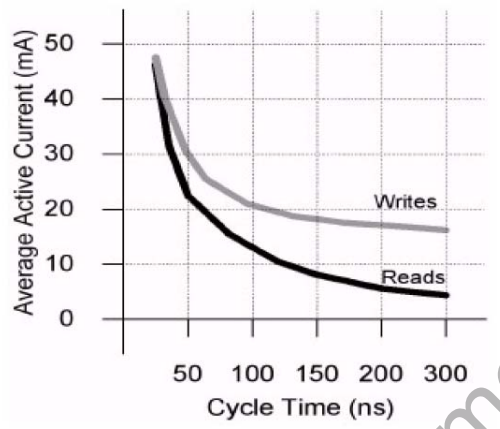
- The nonvolatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprograms these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, and so on. should always program a unique NV pattern (for example, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power up boot firmware routines should rewrite the nvSRAM into the desired state such as AutoStore enabled. While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently (program bugs, incoming inspection routines, and so on.)
- If AutoStore is firmware disabled, it does not reset to "AutoStore enabled" on every power down event captured by the nvSRAM. The application firmware should re-enable or re-disable AutoStore on each reset sequence based on the behavior desired.
- The V_{cap} value specified in this data sheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the max V_{cap} value because the nvSRAM internal algorithm calculates V_{cap} charge time based on this max Vcap value. Customers that want to use a larger V_{cap} value to make sure there is extra store charge and store time should discuss their V_{cap} size selection with Cypress to understand any impact on the V_{cap} voltage level at the end of a t_{RECALL} period.

Low Average Active Power

CMOS technology provides the STK14CA8 with the benefit of power supply current that scales with cycle time. Less current is drawn as the memory cycle time becomes longer than 50 ns. Figure 16 shows the relationship between I_{CC} and READ/WRITE cycle time. Worst case current consumption is shown for commercial temperature range, V_{CC}=3.6V, and chip enable at maximum frequency. Only standby current is drawn when the chip is disabled. The overall average current drawn by the STK14CA8 depends on the following items:

1. The duty cycle of chip enable
2. The overall cycle rate for operations
3. The ratio of READs to WRITEs
4. The operating temperature
5. The VCC Level
6. I/O Loading

Figure 16. Current vs Cycle Time



Preventing AutoStore

The AutoStore function can be disabled by initiating an *AutoStore Disable* sequence. A sequence of READ operations is performed in a manner similar to the software STORE initiation. To initiate the *AutoStore Disable* sequence, the following sequence of $\overline{E}$ controlled or $\overline{G}$ controlled READ operations must be performed:

Read Address	0x4E38	Valid READ
Read Address	0xB1C7	Valid READ
Read Address	0x83E0	Valid READ
Read Address	0x7C1F	Valid READ
Read Address	0x703F	Valid READ
Read Address	0x8B45	AutoStore Disable

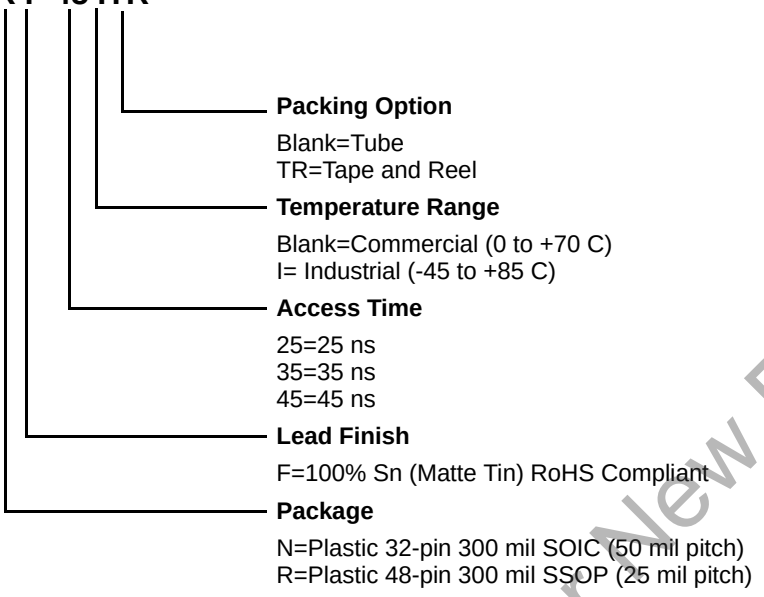
The AutoStore can be re-enabled by initiating an *AutoStore Enable* sequence. A sequence of READ operations is performed in a manner similar to the software RECALL initiation. To initiate the *AutoStore Enable* sequence, the following sequence of $\overline{E}$ controlled or $\overline{G}$ controlled READ operations must be performed:

Read Address	0x4E38	Valid READ
Read Address	0xB1C7	Valid READ
Read Address	0x83E0	Valid READ
Read Address	0x7C1F	Valid READ
Read Address	0x703F	Valid READ
Read Address	0x4B46	AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual STORE operation (Hardware or Software) must be issued to save the AutoStore state through subsequent power down cycles. The part comes from the factory with AutoStore enabled.

Ordering Information

STK14CA8-R F 45 ITR



Packing Option

Blank=Tube
TR=Tape and Reel

Temperature Range

Blank=Commercial (0 to +70 C)
I= Industrial (-45 to +85 C)

Access Time

25=25 ns
35=35 ns
45=45 ns

Lead Finish

F=100% Sn (Matte Tin) RoHS Compliant

Package

N=Plastic 32-pin 300 mil SOIC (50 mil pitch)
R=Plastic 48-pin 300 mil SSOP (25 mil pitch)

Ordering Codes

These parts are not recommended for new designs.

Part Number	Description	Access Times	Temperature
STK14CA8-NF25	3V 128Kx8 AutoStore nvSRAM SOP32-300	25 ns	Commercial
STK14CA8-NF35	3V 128Kx8 AutoStore nvSRAM SOP32-300	35 ns	Commercial
STK14CA8-NF45	3V 128Kx8 AutoStore nvSRAM SOP32-300	45 ns	Commercial
STK14CA8-NF25TR	3V 128Kx8 AutoStore nvSRAM SOP32-300	25 ns	Commercial
STK14CA8-NF35TR	3V 128Kx8 AutoStore nvSRAM SOP32-300	35 ns	Commercial
STK14CA8-NF45TR	3V 128Kx8 AutoStore nvSRAM SOP32-300	45 ns	Commercial
STK14CA8-RF25	3V 128Kx8 AutoStore nvSRAM SSOP48-300	25 ns	Commercial
STK14CA8-RF35	3V 128Kx8 AutoStore nvSRAM SSOP48-300	35 ns	Commercial
STK14CA8-RF45	3V 128Kx8 AutoStore nvSRAM SSOP48-300	45 ns	Commercial
STK14CA8-RF25TR	3V 128Kx8 AutoStore nvSRAM SSOP48-300	25 ns	Commercial
STK14CA8-RF35TR	3V 128Kx8 AutoStore nvSRAM SSOP48-300	35 ns	Commercial
STK14CA8-RF45TR	3V 128Kx8 AutoStore nvSRAM SSOP48-300	45 ns	Commercial
STK14CA8-NF25I	3.3V 128Kx8 AutoStore nvSRAM SOP32-300	25 ns	Industrial
STK14CA8-NF35I	3V 128Kx8 AutoStore nvSRAM SOP32-300	35 ns	Industrial
STK14CA8-NF45I	3V 128Kx8 AutoStore nvSRAM SOP32-300	45 ns	Industrial
STK14CA8-NF25ITR	3.3V 128Kx8 AutoStore nvSRAM SOP32-300	25 ns	Industrial
STK14CA8-NF35ITR	3V 128Kx8 AutoStore nvSRAM SOP32-300	35 ns	Industrial
STK14CA8-NF45ITR	3V 128Kx8 AutoStore nvSRAM SOP32-300	45 ns	Industrial
STK14CA8-RF25I	3.3V 128Kx8 AutoStore nvSRAM SSOP48-300	25 ns	Industrial
STK14CA8-RF35I	3V 128Kx8 AutoStore nvSRAM SSOP48-300	35 ns	Industrial
STK14CA8-RF45I	3V 128Kx8 AutoStore nvSRAM SSOP48-300	45 ns	Industrial
STK14CA8-RF25ITR	3.3V 128Kx8 AutoStore nvSRAM SSOP48-300	25 ns	Industrial
STK14CA8-RF35ITR	3V 128Kx8 AutoStore nvSRAM SSOP48-300	35 ns	Industrial
STK14CA8-RF45ITR	3V 128Kx8 AutoStore nvSRAM SSOP48-300	45 ns	Industrial

Package Diagrams

Figure 17. 32-Pin 300 mil SOIC (51-85127)

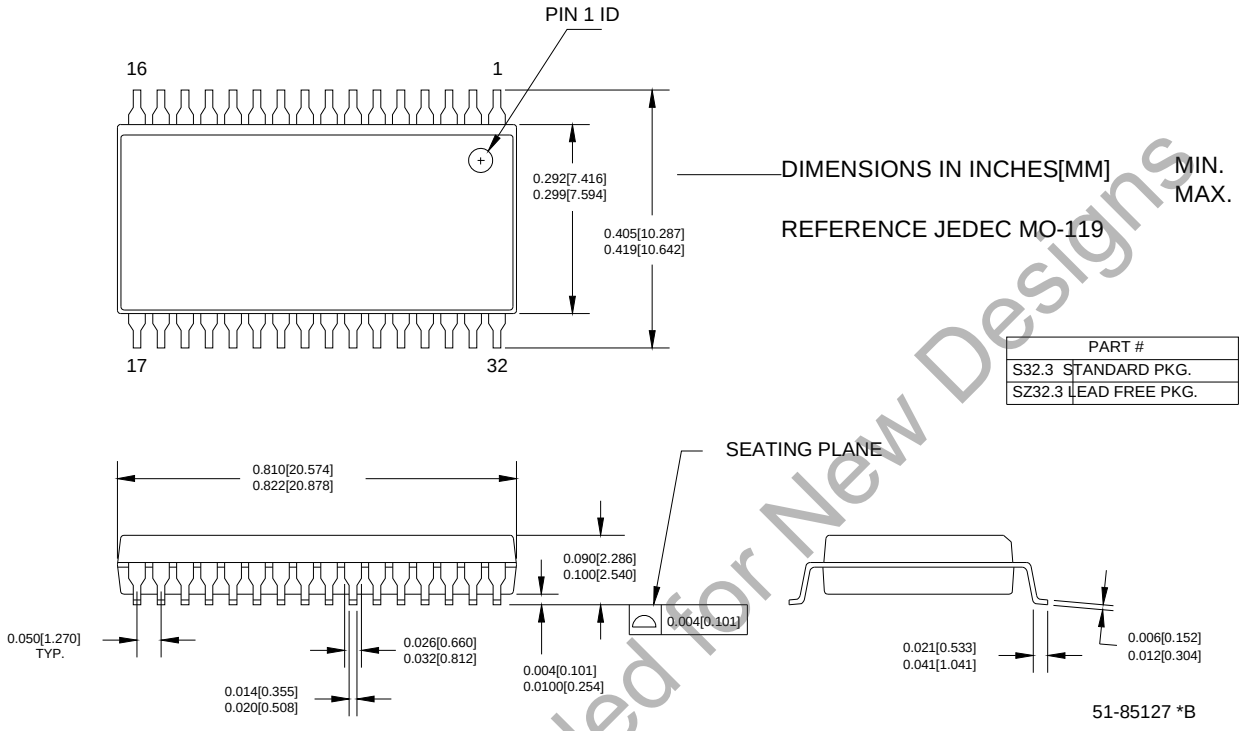
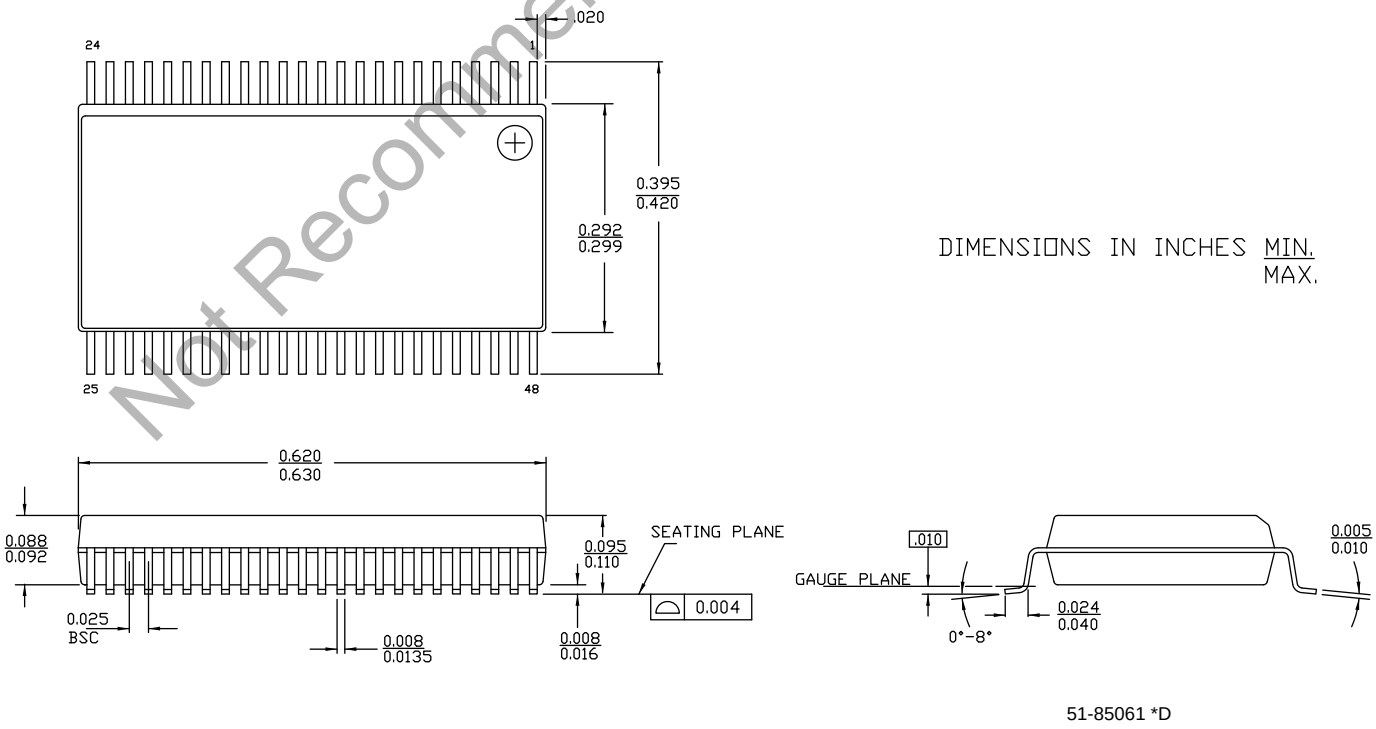


Figure 18. 48-Pin 300 mil SSOP (51-85061)



Document History Page

Document Title: STK14CA8 128Kx8 AutoStore nvSRAM Document Number: 001-51592				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2665610	GVCH/PYRS	02/04/09	New data sheet
*A	2821358	GVCH	12/04/09	Added Note in Ordering Information mentioning that these parts are not recommended for new designs. Added “Not recommended for New Designs” watermark in the PDF. Added Contents on page 2.
*B	2895330	GVCH	03/18/10	Added foot note 1 for 25ns access speed, Updated Package Diagram 48-Pin 300 mil SSOP. Updated Ordering Codes Description
*C	2902517	GVCH	03/31/2010	Added watermark "Not Recommended for New Designs" in pdf version. Move to external web.

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