STK12C68-M

CMOS nvSRAM
8K x 8 *AutoStore™*
Nonvolatile Static RAM
MIL-STD-883 / SMD # 5962-94599

FEATURES

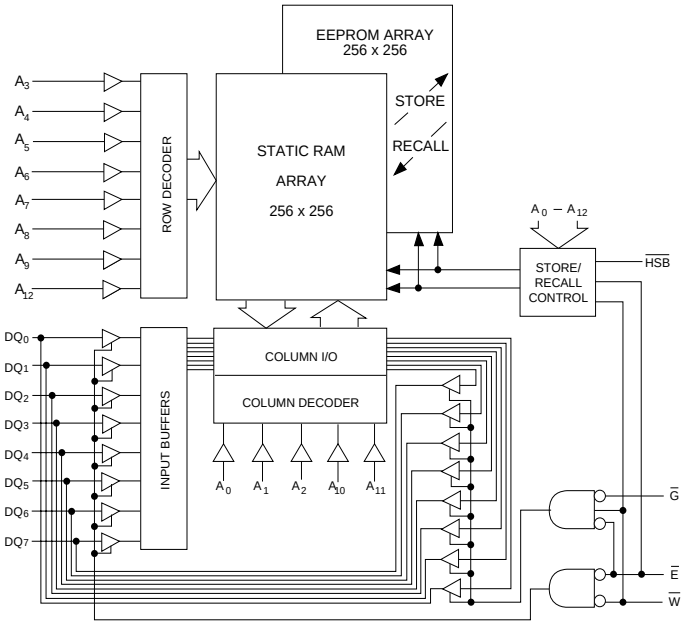
- **40, 45 and 55ns Access Times**
- **15 mA I_{CC} at 200ns Access Speed**
- **Automatic *STORE* to EEPROM on Power Down**
- **Hardware or Software initiated *STORE* to EEPROM**
- **Automatic *STORE* Timing**
- **100,000 *STORE* cycles to EEPROM**
- **10 year data retention in EEPROM**
- **Automatic *RECALL* on Power Up**
- **Software initiated *RECALL* from EEPROM**
- **Unlimited *RECALL* cycles from EEPROM**
- **Single 5V±10% Operation**
- **Available in multiple standard packages**

DESCRIPTION

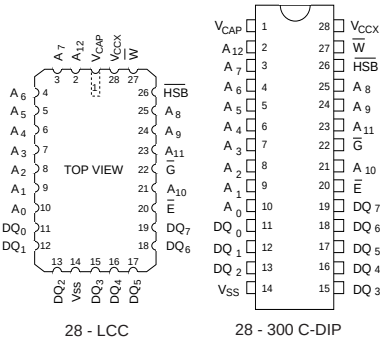
The Simtek STK12C68-M is a fast static RAM (40, 45 and 55ns), with a nonvolatile EEPROM element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the *STORE* operation) take place automatically upon power down using charge stored in an external 100 µF capacitor. Transfers from the EEPROM to the SRAM (the *RECALL* operation) take place automatically on power up. Software sequences may also be used to initiate both *STORE* and *RECALL* operations. A *STORE* can also be initiated via a single pin.

The STK12C68-M is available in the following packages: a 28-pin 300 mil ceramic DIP and 28-pad LCC.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN NAMES

A_0 - A_{12}	Address Inputs
$\overline{W}$	Write Enable
DQ_0 - DQ_7	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{CCX}	Power (+5V)
V_{SS}	Ground
V_{CAP}	Capacitor
$\overline{HSB}$	Hardware Store/Busy

ABSOLUTE MAXIMUM RATINGS[a]

Voltage on typical input relative to V_{SS}. . . . . –0.6V to 7.0V
Voltage on DQ_{0-7} and $\overline{G}$. . . . . .–0.5V to (V_{CC}+0.5V)
Temperature under bias . . . . . –55°C to 125°C
Storage temperature. . . . . –65°C to 150°C
Power dissipation. 1W
DC output current 15mA
(One output at a time, one second duration)

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ± 10%)[d]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC_1}[b]	Average V_{CC} Current		85	mA	t_{AVAV} = 40ns
			80	mA	t_{AVAV} = 45ns
			75	mA	t_{AVAV} = 55ns
I_{CC_2}	Average V_{CC} Current During *STORE*		8	mA	All inputs ≤ 0.2V or ≥ (V_{CC} – 0.2V)
I_{CC_3}[b]	Average V_{CC} Current		15	mA	$\overline{E}$ ≤ 0.2V, $\overline{W}$ ≥ (V_{CC} – 0.2V)
	at t_{AVAV} = 200ns				others ≤ 0.2V or ≥ (V_{CC} – 0.2V)
I_{CC_4}	Average VCC current during AutoStore™ cycle		4	mA	All inputs ≤ 0.2V or ≥ (V_{CC} - 0.2V)
I_{SB_1}[c]	Average V_{CC} Current		35	mA	t_{AVAV} = 40ns
	(Standby, Cycling TTL Input Levels)		32	mA	t_{AVAV} = 45ns
			28	mA	t_{AVAV} = 55ns
					$\overline{E}$ ≥ V_{IH}; all others cycling
I_{CC_2}[b]	Average V_{CC} Current		4	mA	$\overline{E}$ ≥ (V_{CC} – 0.2V)
	(Standby, Stable CMOS Input Levels)				
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	V_{CC} = max
					V_{IN} = V_{SS} to V_{CC}
I_{OLK}	Off State Output Leakage Current		±5	µA	V_{CC} = max
					V_{OUT} = V_{SS} to V_{CC}
V_{IH}	Input Logic "1" Voltage	2.2	V_{CC}+.5	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS}–.5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OUT} = –4mA except $\overline{HSB}$
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OUT} = 8mA except $\overline{HSB}$
T_A	Operating Temperature	–55	125	°C	

Note b: I_{CC_1} and I_{CC_3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: Bringing $\overline{E}$ ≥ V_{IH} will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.
Note d: V_{CC} reference levels throughout this datasheet refer to V_{CCX} if that is where the power supply connection is made, or V_{CAP} if V_{CCX} is connected to ground.

AC TEST CONDITIONS

Input Pulse Levels. . . . . V_{SS} to 3V
Input Rise and Fall Times. . . . . ≤ 5ns
Input and Output Timing Reference Levels. 1.5V
Output Load. . . . . See Figure 1

CAPACITANCE (T_A=25°C, f=1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	8	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

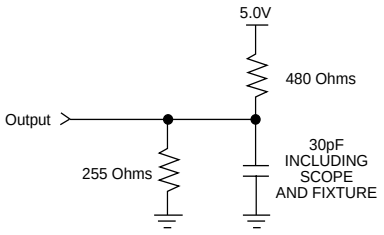


Figure 1: AC Output Loading

SRAM MEMORY OPERATION

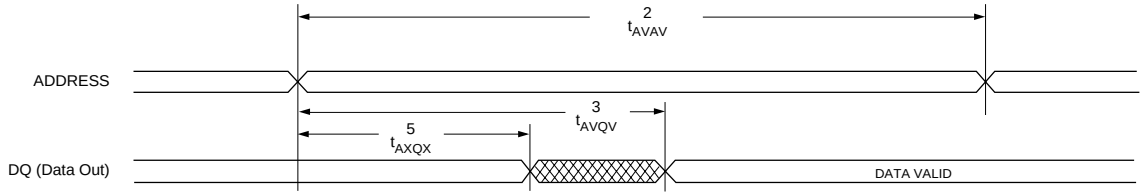
READ CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)[d]

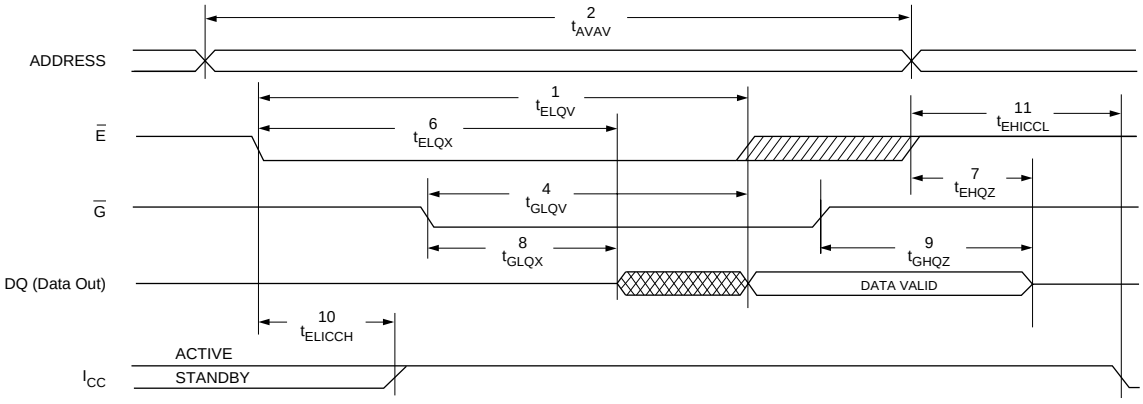
NO.	SYMBOLS		PARAMETER	STK12C68-40M		STK12C68-45M		STK12C68-55M		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		40		45		55	ns
2	t_{AVAV}	t_{RC}	Read Cycle Time	40		45		55		ns
3	t_{AVQV}[g]	t_{AA}	Address Access Time		40		45		55	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		20		25		35	ns
5	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		ns
6	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns
7	t_{EHQZ}[h]	t_{HZ}	Chip Disable to Output Inactive		17		20		25	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHQZ}[h]	t_{OHZ}	Output Disable to Output Inactive		17		20		25	ns
10	t_{ELICCH}[e]	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	t_{EHICCL}[c,e]	t_{PS}	Chip Disable to Power Standby		35		45		55	ns

Note c: Bringing $\overline{E} \geq V_{IH}$ will not produce standby currents until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.
Note e: Parameter guaranteed but not tested.
Note f: For READ CYCLE #1 and #2, $\overline{W}$ is high for entire cycle.
Note g: Device is continuously selected with $\overline{E}$ low and $\overline{G}$ low.
Note h: Measured ± 200mV from steady state output voltage.

READ CYCLE #1 [f,g]



READ CYCLE #2 [f]



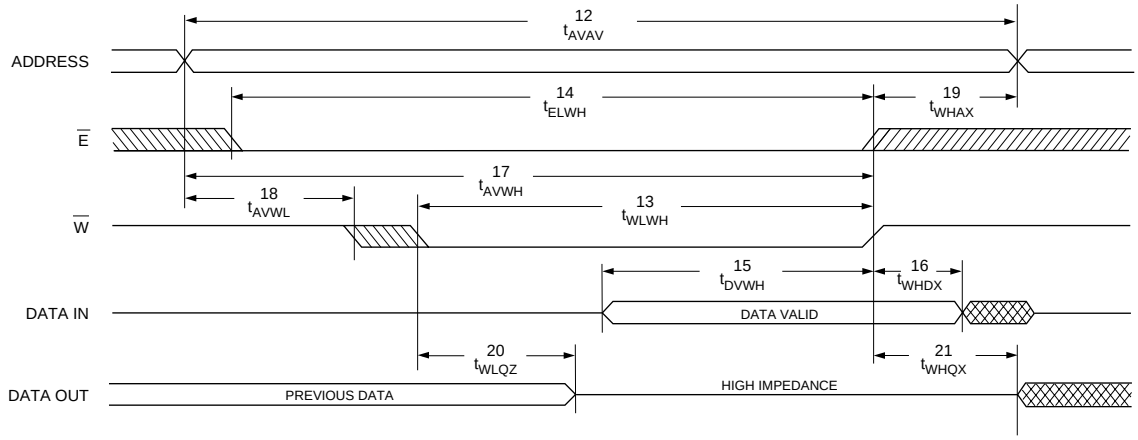
WRITE CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)[d]

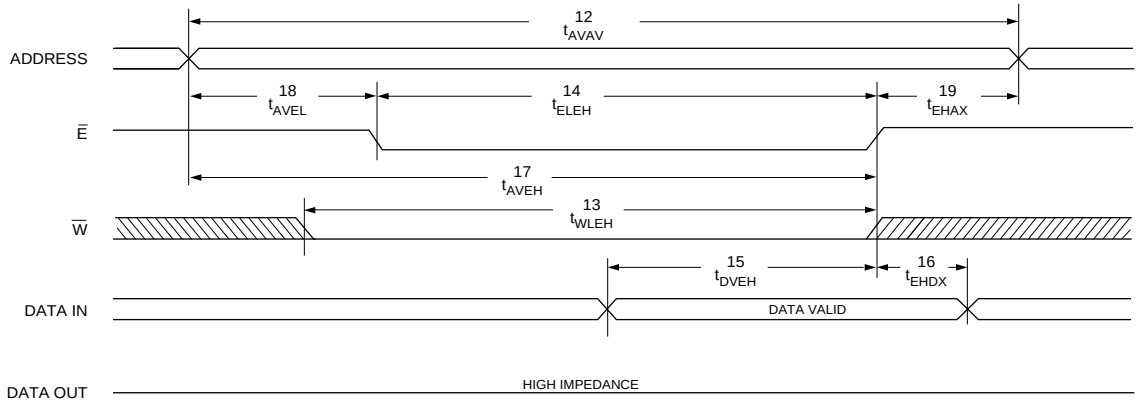
NO.	SYMBOLS			PARAMETER	STK12C68-40M		STK12C68-45M		STK12C68-55M		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	35		45		55		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	30		35		45		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	30		35		45		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	18		20		25		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	30		35		45		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns
20	t_{WLQZ}[h,j]		t_{WZ}	Write Enable to Output Disable		17		20		25	ns
21	t_{WHQX}		t_{OW}	Output Active After End of Write	5		5		5		ns

Note h: Measured ±200mV from steady state output voltage.
Note i: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note j: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.

WRITE CYCLE #1: $\overline{W}$ CONTROLLED [i]



WRITE CYCLE #2: $\overline{E}$ CONTROLLED [i]



NONVOLATILE MEMORY OPERATION

MODE SELECTION

$\overline{E}$	$\overline{W}$	$\overline{HSB}$	A_{12} - A_0(hex)	MODE	I/O	POWER	NOTES
H	X	H	X	Not Selected	Output High Z	Standby	
L	H	H	X	Read SRAM	Output Data	Active	l
L	L	H	X	Write SRAM	Input Data	Active	
L	H	H	0000	Read SRAM	Output Data	Active	k,l
			1555	Read SRAM	Output Data		k,l
			0AAA	Read SRAM	Output Data		k,l
			1FFF	Read SRAM	Output Data		k,l
			10F0	Read SRAM	Output Data		k,l
			0F0F	Nonvolatile *STORE*	Output High Z		k
L	H	H	0000	Read SRAM	Output Data	Active	k,l
			1555	Read SRAM	Output Data		k,l
			0AAA	Read SRAM	Output Data		k,l
			1FFF	Read SRAM	Output Data		k,l
			10F0	Read SRAM	Output Data		k,l
			0F0E	Nonvolatile *RECALL*	Output High Z		k
X	X	L	X	*STORE*/Inhibit	Output High Z	I_{CC2}/Standby	m

Note k: The six consecutive addresses must be in order listed - (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a *STORE* cycle or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a *RECALL* cycle. $\overline{W}$ must be high during all six consecutive cycles. See *STORE* cycle and *RECALL* cycle tables and diagrams for further details.

Note l: I/O state assumes that $\overline{G} \le V_{IL}$. Activation of nonvolatile cycles does not depend on the state of $\overline{G}$.

Note m: $\overline{HSB}$ initiated *STORE* operation actually occurs only if a WRITE has been done since last *STORE* operation. After the *STORE* (if any) completes, the part will go into standby mode inhibiting all operation until $\overline{HSB}$ rises.

HARDWARE *STORE* / *RECALL*

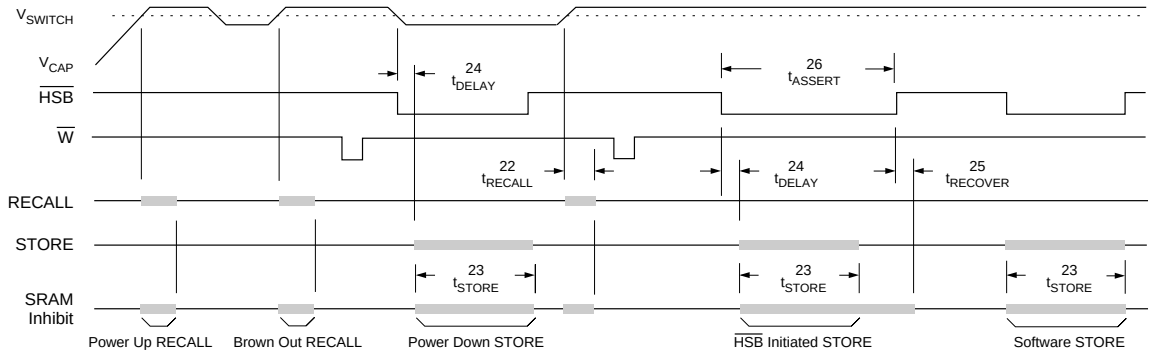
NO.	SYMBOLS		PARAMETER	MIN	MAX	UNITS	NOTES
22	t_{RECALL}		*RECALL* Cycle Duration		20	µs	Note o
23	t_{STORE}	t_{HLHH}	*STORE* Cycle Duration		10	ms	$V_{CC} \ge 4.5V$
24	t_{DELAY}	t_{HLQZ}	$\overline{HSB}$ Low to Inhibit On	1		µs	
25	$t_{RECOVER}$	t_{HHQX}	$\overline{HSB}$ High to Inhibit Off		300	ns	Note e
26	t_{ASSERT}	t_{HLHX}	External *STORE* Pulse Width	250		ns	Note e
	V_{SWITCH}		Low Voltage Trigger Level	4.0	4.5	V	
	$I_{\overline{HSB}\_OL}$		$\overline{HSB}$ Output Low Current	3		mA	$\overline{HSB} = V_{OL}$, Note e, n
	$I_{\overline{HSB}\_OH}$		$\overline{HSB}$ Output High Current	5	60	µA	$\overline{HSB} = V_{IL}$, Note e, n

Note e: These parameters guaranteed but not tested.

Note n: $\overline{HSB}$ is an I/O that has a weak internal pullup; it is basically an open drain output. It is meant to allow up to 32 STK12C68-Ms to be ganged together for simultaneous storing. Do not use $\overline{HSB}$ to pullup any external circuitry other than other STK12C68-M $\overline{HSB}$ pins.

Note o: A RECALL cycle is initiated automatically at power up when V_{CC} exceeds V_{SWITCH}. t_{RECALL} is measured from the point at which V_{CC} exceeds 4.5V.

HARDWARE *STORE* / *RECALL*



SOFTWARE STORE/RECALL CYCLE

(V_{CC} = 5.0V ± 10%)[d]

NO.	SYMBOLS		PARAMETER	STK12C68-40M		STK12C68-45M		STK12C68-55M		UNITS
	Std.	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
28	t_{AVAV}	t_{RC}	*STORE/RECALL* Initiation Cycle Time	35		45		55		ns
29	t_{ELQZ}[p]		Chip Enable to Output Inactive		85		85		85	ns
30	t_{AVELN}	t_{AE}	Address Set-up to Chip Enable	0		0		0		ns
31	t_{ELEHN}[q,r]	t_{EP}	Chip Enable Pulse Width	25		35		45		ns
32	t_{EHAXN}	t_{EA}	Chip Disable to Address Change	0		0		0		ns

Note p: Once the software *STORE* or *RECALL* cycle is initiated, it completes automatically, ignoring all inputs.

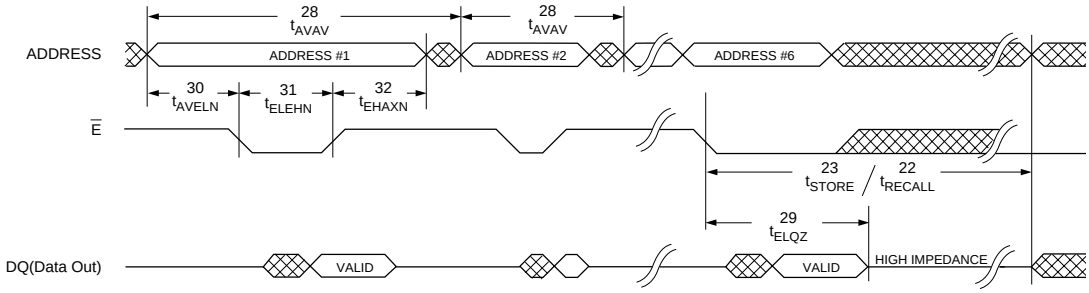
Note q: Noise on the $\overline{E}$ pin may trigger multiple read cycles from the same address and abort the address sequence.

Note r: If the Chip Enable Pulse Width is less than t_{ELQV} (see READ CYCLE #2) but greater than or equal to t_{ELEHN}, then the data may not be valid at the end of the low pulse, however the *STORE* or *RECALL* will still be initiated.

Note s: $\overline{W}$ must be HIGH when $\overline{E}$ is LOW during the address sequence in order to initiate a nonvolatile cycle. $\overline{G}$ may be either HIGH or LOW throughout. Addresses #1 through #6 are found in the MODE SELECTION table. Address #6 determines whether the STK12C68-M performs a *STORE* or *RECALL*.

Note t: $\overline{E}$ must be used to clock in the address sequence for the Software *STORE* and *RECALL* cycles.

SOFTWARE STORE/RECALL CYCLE [q,r,t]



DEVICE OPERATION

The STK12C68-M has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to EEPROM (the *STORE* operation) or from EEPROM to SRAM (the *RECALL* operation). In this mode SRAM functions are disabled.

STORE cycles may be initiated under user control via a software sequence or $\overline{HSB}$ assertion and are also automatically initiated when the power supply voltage level of the chip falls below V_{SWITCH}. *RECALL* operations are automatically initiated upon power-up and whenever the power supply voltage level rises above V_{SWITCH}. *RECALL* cycles may also be initiated by a software sequence.

SRAM READ

The STK12C68-M performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are LOW and $\overline{HSB}$ and $\overline{W}$ are HIGH. The address specified on pins A_{0-12} determines which of the 8192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV}. If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV}, whichever is later. The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought HIGH or $\overline{W}$ or $\overline{HSB}$ is brought LOW.

SRAM WRITE

A write cycle is performed whenever $\overline{E}$ and $\overline{W}$ are LOW and $\overline{HSB}$ is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ go HIGH at the end of the cycle. The data on pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept HIGH during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{G}$ is left LOW, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes LOW.

SOFTWARE *STORE*

The STK12C68-M software *STORE* cycle is initiated by executing sequential READ cycles from six specific address locations. By relying on READ cycles only, the STK12C68-M implements nonvolatile operation while remaining compatible with standard 8Kx8 SRAMs. During the *STORE* cycle, an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into the nonvolatile elements. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of addresses is used for *STORE* initiation, it is critical that no other read or write accesses intervene in the sequence or the sequence will be aborted.

To initiate the *STORE* cycle the following READ sequence must be performed:

1.	Read address	0000 (hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0F (hex)	Initiate *STORE* Cycle

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{G}$ be LOW for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE RECALL

A *RECALL* cycle of the EEPROM data into the SRAM is initiated with a sequence of READ operations in a manner similar to the *STORE* initiation. To initiate the *RECALL* cycle the following sequence of READ operations must be performed:

1.	Read address	0000(hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0E (hex)	Initiate *RECALL* Cycle

Internally, *RECALL* is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The *RECALL* operation in no way alters the data in the

EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

AUTOMATIC RECALL

During power up, or after any low power condition (V_{CAP} < V_{SWITCH}), when V_{CAP} exceeds the sense voltage of V_{SWITCH}, a *RECALL* cycle will automatically be initiated. After the initiation of this automatic *RECALL*, if V_{CAP} falls below V_{SWITCH}, then another *RECALL* operation will be performed whenever V_{CAP} again rises above V_{SWITCH}.

If the STK12C68-M is in a WRITE state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected between $\overline{W}$ and system V_{CC}.

HARDWARE PROTECT

The STK12C68-M offers hardware protection against inadvertent *STORE* operation during low voltage conditions. When V_{CAP} < V_{SWITCH}, all externally initiated *STORE* operations will be inhibited.

$\overline{HSB}$ OPERATION

The Hardware Store Busy pin ($\overline{HSB}$) is an open drain circuit acting as both input and output to perform two different functions. When driven low by the internal chip circuitry it indicates that a *STORE* operation (initiated via any means) is in progress within the chip. When driven low by external circuitry for longer than t_{ASSERT}, the chip will conditionally initiate a *STORE* operation after t_{DELAY}.

READ and WRITE operations that are in progress when $\overline{HSB}$ is driven low (either by internal or external circuitry) will be allowed to complete before the *STORE* operation is performed, in the following manner. After $\overline{HSB}$ goes low, the part will continue normal SRAM operations for t_{DELAY}. During t_{DELAY}, a transition on any address or control signal will terminate SRAM operation and cause the *STORE* to commence. Note that if an SRAM write is attempted after $\overline{HSB}$ has been forced low, the write will not occur and the *STORE* operation will begin immediately.

Hardware-Store-Busy ($\overline{HSB}$) is a high speed, low drive capability bi-directional control line. In order to allow a bank of STK12C68-Ms to perform synchronized *STORE* functions, the $\overline{HSB}$ pin from a number of chips may be connected together. Each chip contains a small internal current source to pull $\overline{HSB}$ HIGH when it is not being driven low. To decrease the sensitivity of this signal to noise generated on the PC board, it may optionally be pulled to V_{CCX} via an external resistor with a value such that the combined load of the resistor and all parallel chip connections does not exceed $I_{\overline{HSB}\_OL}$ at V_{OL}. Do not connect this or any other pull-up to the V_{CAP} node.

If $\overline{HSB}$ is to be connected to external circuits other than other STK12C68-Ms, an external pull-up resistor should be used.

During any *STORE* operation, regardless of how it was initiated, the STK12C68-M will continue to drive the $\overline{HSB}$ pin low, releasing it only when the *STORE* is complete. Upon completion of a *STORE* operation, the part will be disabled until $\overline{HSB}$ actually goes HIGH.

AUTOMATIC *STORE* OPERATION

During normal operation, the STK12C68-M will draw current from V_{CCX} to charge up a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single *STORE* operation. After power up, when the voltage on the V_{CAP} pin drops below V_{SWITCH}, the part will automatically disconnect the V_{CAP} pin from V_{CCX} and initiate a *STORE* operation.

Figure 1 shows the proper connection of capacitors for automatic store operation. The charge storage capacitor should have a capacity of at least 100µF (± 20%) at 6V. Each STK12C68-M must have its own 100µF capacitor. Each STK12C68-M *must* have a high quality, high frequency bypass capacitor of 0.1µF connected between V_{CAP} and V_{SS}, using leads and traces that are as short as possible.

If the *AutoStore*™ function is not required, then V_{CAP} should be tied directly to the power supply and V_{CCX} should be tied to ground. In this mode, *STORE* operations may be triggered through software control or the $\overline{HSB}$ pin. In either event, V_{CAP} (Pin 1) *must* always have a proper bypass capacitor connected to it.

In order to prevent unneeded *STORE* operations, automatic *STOREs* as well as those initiated by externally driving $\overline{HSB}$ LOW will be ignored unless at least one

WRITE operation has taken place since the most recent *STORE* cycle. Note that if HSB is driven low via external circuitry and no WRITEs have taken place, the part will still be disabled until HSB is allowed to return HIGH. Software initiated *STORE* cycles are performed regardless of whether or not a WRITE operation has taken place.

PREVENTING AUTOMATIC STORES

The *AutoStore*™ function can be disabled on the fly by holding HSB HIGH with a driver capable of sourcing 15mA at a VOH of at least 2.2V as it will have to overpower the internal pull-down device that drives HSB low for 50ns at the onset of an *AutoStore*™. When the STK12C68-M is connected for *AutoStore*™ operation (system V_{CC} connected to V_{CCX} and a 100uF capacitor on V_{CAP}) and V_{CC} crosses V_{SWITCH} on the way down, the STK12C68 will attempt to pull HSB LOW; if HSB doesn't actually get below V_{IL}, the part will stop trying to pull HSB LOW and abort the *AutoStore*™ attempt.

LOW AVERAGE ACTIVE POWER

The STK12C68-M has been designed to draw significantly less power when $\overline{E}$ is LOW (chip enabled) but the access cycle time is longer than 55ns. *Figure 2* below shows the relationship between I_{CC} and access times for READ cycles. All remaining inputs are assumed to cycle, and current consumption is given for all inputs at CMOS or TTL levels. *Figure 3* shows the same relationship for WRITE cycles. When $\overline{E}$ is HIGH, the chip consumes only standby currents, and these plots do not apply.

The cycle time used in *Figure 2* corresponds to the length of time from the later of the last address transition or $\overline{E}$ going LOW to the earlier of $\overline{E}$ going HIGH or the next address transition. $\overline{W}$ is assumed to be HIGH, while the state of $\overline{G}$ does not matter. Additional current is consumed when the address lines change state while $\overline{E}$ is asserted. The cycle time used in *Figure 3* corresponds to the length of time from the later of $\overline{W}$ or $\overline{E}$ going LOW to the earlier of $\overline{W}$ or $\overline{E}$ going HIGH.

The overall average current drawn by the part depends on the following items: 1) CMOS or TTL input levels; 2) the time during which the chip is disabled ($\overline{E}$ HIGH); 3) the cycle time for accesses ($\overline{E}$ LOW); 4) the ratio of reads to writes; 5) the operating temperature; 6) the V_{CC} level; and 7) output load.

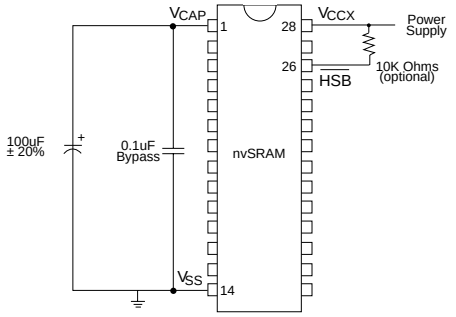


Figure 1
Schematic Diagram

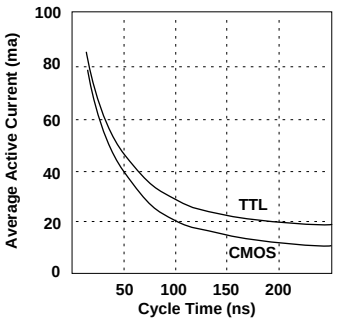


Figure 2
I_{CC} (Max) Reads

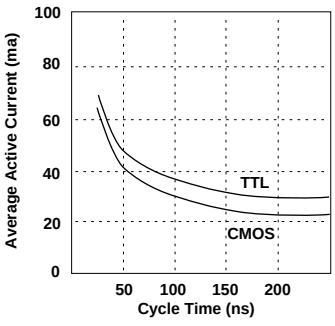


Figure 3
I_{CC} (Max) Writes

Note: Typical at 25° C

ORDERING INFORMATION

STK12C68 - 5 C 40 M

Temperature Range
M = Military (-55 to 125 degrees C)

Access Time
40 = 40ns
45 = 45ns
55 = 55ns

Package
C = Ceramic 28 pin 300-mil DIP with gold lead finish
K = Ceramic 28 pin 300-mil DIP with solder DIP finish
L = Ceramic 28 pin LCC

Retention / Endurance
10 years / 100,000 cycles

5962-94599 01 MX X

Lead Finish
A = Solder DIP lead finish
C = Gold lead DIP finish
X = lead finish "A" or "C" is acceptable

Package
MX = Ceramic 28 pin 300-mil DIP
MY = Ceramic 28 pin LCC

Access Time
01 = 55ns
02 = 45ns