

FEATURES

- 25, 35, 45, 55 ns Read Access & Write Cycle Time
- Unlimited Read/Write Endurance
- Automatic Non-volatile STORE on Power Loss
- Non-Volatile STORE Under Hardware or Software Control
- Automatic RECALL to SRAM on Power Up
- Unlimited RECALL Cycles
- 1 Million STORE Cycles
- 100-Year Non-volatile Data Retention
- Single 5V ± 10% Power Supply
- Commercial, Industrial, Military Temperatures
- 28-pin 330-mil SOIC, 300-mil PDIP, and 600-mil PDIP Packages (RoHS-Compliant)
- 28-Pin CDIP and LCC Military Packages

DESCRIPTION

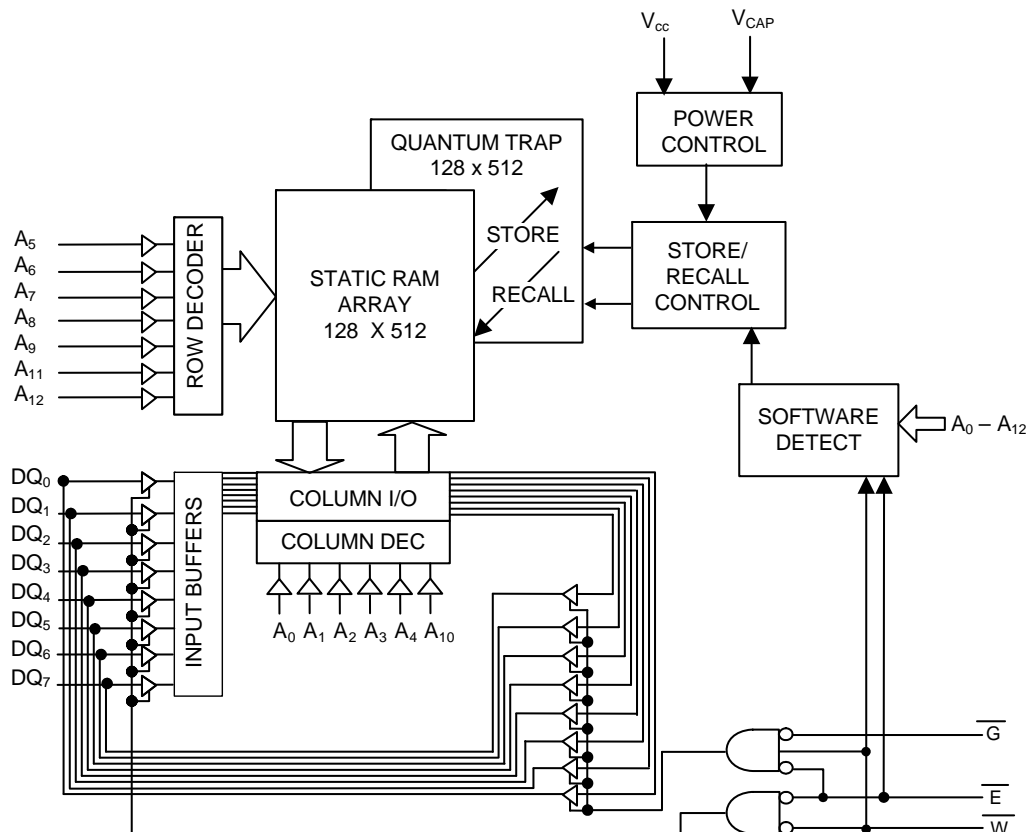
The Simtek STK12C68 is a 64Kb fast static RAM with a non-volatile Quantum Trap storage element included with each memory cell.

The SRAM provides the fast access & cycle times, ease of use and unlimited read & write endurance of a normal SRAM.

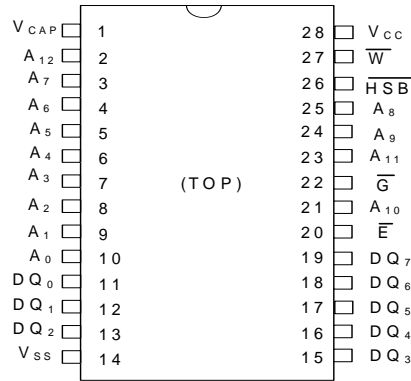
Data transfers automatically to the non-volatile storage cells when power loss is detected (the *STORE* operation). On power up, data is automatically restored to the SRAM (the *RECALL* operation). Both *STORE* and *RECALL* operations are also available under software control.

The Simtek nvSRAM is the first monolithic non-volatile memory to offer unlimited writes and reads. It is the highest performance, most reliable non-volatile memory available.

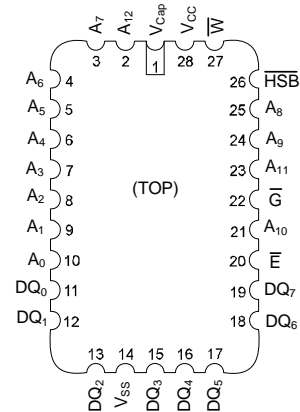
Block Diagram



Packages



**28-pin SOIC
28-pin DIP**



28-pin LCC

Pin Descriptions

Pin Name	I/O	Description
A ₁₂ -A ₀	Input	Address: The 13 address inputs select one of 8,192 bytes in the nvSRAM array
DQ ₇ -DQ ₀	I/O	Data: Bi-directional 8-bit data bus for accessing the nvSRAM
\bar{E}	Input	Chip Enable: The active low \bar{E} input selects the device
\bar{W}	Input	Write Enable: The active low \bar{W} enables data on the DQ pins to be written to the address location latched by the falling edge of \bar{E}
\bar{G}	Input	Output Enable: The active low \bar{G} input enables the data output buffers during read cycles. De-asserting \bar{G} high caused the DQ pins to tri-state.
V _{CC}	Power Supply	Power: 5.0V, $\pm 10\%$
\overline{HSB}	I/O	Hardware Store Busy: When low this output indicates a Store is in progress. When pulled low external to the chip, it will initiate a nonvolatile STORE operation. A weak pull up resistor keeps this pin high if not connected. (Connection Optional).
V _{CAP}	Power Supply	AutoStore Capacitor: Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile storage elements.
V _{SS}	Power Supply	Ground

ABSOLUTE MAXIMUM RATINGS^a

Voltage on Input Relative to Ground -0.5V to 7.0V
 Voltage on Input Relative to V_{SS} -0.6V to (V_{CC} + 0.5V)
 Voltage on DQ₀₋₇ or HSB -0.5V to (V_{CC} + 0.5V)
 Temperature under Bias -55°C to 125°C
 Storage Temperature -65°C to 150°C
 Power Dissipation 1W
 DC Output Current (1 output at a time, 1s duration) 15mA
 Package Thermal Characteristics - See Website at <http://www.simtek.com>

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ± 10%)^e

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL MILITARY		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I _{CC1} ^b	Average V _{CC} Current		85		85	mA	t _{AVAV} = 25ns (commercial and industrial only) t _{AVAV} = 35ns t _{AVAV} = 45ns (commercial and industrial only) t _{AVAV} = 55ns
			75		75	mA	
			65		65	mA	
			--		55	mA	
I _{CC2} ^c	Average V _{CC} Current during STORE		3		3	mA	All Inputs Don't Care, V _{CC} = max
I _{CC3} ^b	Average V _{CC} Current at t _{AVAV} = 200ns 5V, 25°C, Typical		10		10	mA	$\bar{W} \geq (V_{CC} - 0.2V)$ All Others Cycling, CMOS Levels
I _{CC4} ^c	Average V _{CAP} Current during AutoStore Cycle		2		2	mA	All Inputs Don't Care
I _{SB1} ^d	Average V _{CC} Current (Standby, Cycling TTL Input Levels)		27		27	mA	t _{AVAV} = 25ns, $\bar{E} \geq V_{IH}$ (commercial and industrial only) t _{AVAV} = 35ns, $\bar{E} \geq V_{IH}$ t _{AVAV} = 45ns, $\bar{E} \geq V_{IH}$ (commercial and industrial only) t _{AVAV} = 55ns, $\bar{E} \geq V_{IH}$
			24		24	mA	
			20		20	mA	
			--		19	mA	
I _{SB2} ^d	V _{CC} Standby Current (Standby, Stable CMOS Input Levels)		1.5		2.5	mA	$\bar{E} \geq (V_{CC} - 0.2V)$ All Others V _{IN} ≤ 0.2V or ≥ (V _{CC} - 0.2V)
I _{ILK}	Input Leakage Current		±1		±1	µA	V _{CC} = max V _{IN} = V _{SS} to V _{CC}
I _{OLK}	Off-State Output Leakage Current		±5		±5	µA	V _{CC} = max V _{IN} = V _{SS} to V _{CC} , \bar{E} or $\bar{G} \geq V_{IH}$
V _{IH}	Input Logic "1" Voltage	2.2	V _{CC} + .5	2.2	V _{CC} + .5	V	All Inputs
V _{IL}	Input Logic "0" Voltage	V _{SS} - .5	0.8	V _{SS} - .5	0.8	V	All Inputs
V _{OH}	Output Logic "1" Voltage	2.4		2.4		V	I _{OUT} = -4mA except $\bar{H}\bar{S}\bar{B}$
V _{OL}	Output Logic "0" Voltage		0.4		0.4	V	I _{OUT} = 8mA except $\bar{H}\bar{S}\bar{B}$
V _{BL}	Logic "0" Voltage on $\bar{H}\bar{S}\bar{B}$ Output		0.4		0.4	V	I _{OUT} = 3mA
T _A	Operating Temperature	0	70	-40/-55	85/125	°C	

Note b: I_{CC1} and I_{CC3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note c: I_{CC2} and I_{CC4} are the average currents required for the duration of the respective STORE cycles (t_{STORE}).

Note d: $\bar{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.

Note e: V_{CC} reference levels throughout this datasheet refer to V_{CC} if that is where the power supply connection is made, or V_{CAP} if V_{CC} is connected to ground.

AC TEST CONDITIONS

Input Pulse Levels 0V to 3V
 Input Rise and Fall Times ≤ 5ns
 Input and Output Timing Reference Levels 1.5V
 Output Load See Figure 1

CAPACITANCE^f (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C _{IN}	Input Capacitance	8	pF	ΔV = 0 to 3V
C _{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note f: These parameters are guaranteed but not tested.

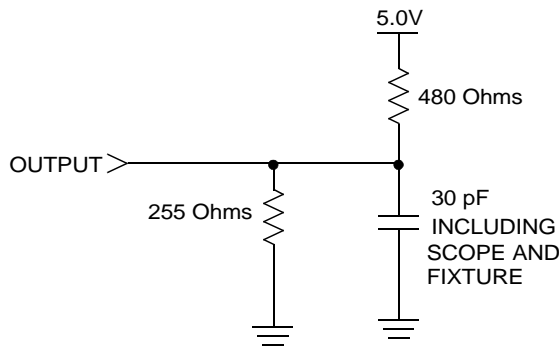


Figure 1. AC Output Loading

SRAM READ CYCLES #1 & #2

($V_{CC} = 5.0V \pm 10\%$)^e

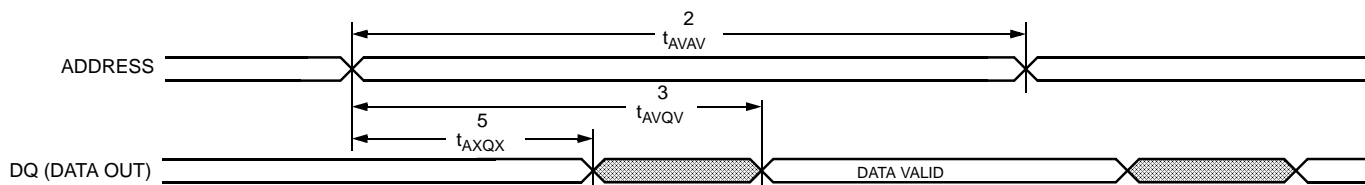
NO.	SYMBOLS		PARAMETER	STK12C68, STK12C68-5-25		STK12C68, STK12C68-5-35		STK12C68, STK12C68-5-45		STK12C68, STK12C68-5-55		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45		55	ns
2	t_{AVAV}^g, t_{ELEH}^g	t_{RC}	Read Cycle Time	25		35		45		55		ns
3	t_{AVQV}^h	t_{AA}	Address Access Time		25		35		45		55	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		10		15		20		35	ns
5	t_{AXQX}^h	t_{OH}	Output Hold after Address Change	5		5		5		5		ns
6	t_{ELQX}	t_{LZ}	Address Change or Chip Enable to Output Active	5		5		5		5		ns
7	t_{EHQZ}^i	t_{HZ}	Address Change or Chip Disable to Output Inactive		10		10		12		12	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		0		ns
9	t_{GHQZ}^i	t_{OHZ}	Output Disable to Output Inactive		10		10		12		12	ns
10	t_{ELICCH}^f	t_{PA}	Chip Enable to Power Active	0		0		0		0		ns
11	t_{EHICCL}^f	t_{PS}	Chip Disable to Power Standby		25		35		45		55	ns

Note g: \overline{W} and HSB must be high during SRAM READ cycles.

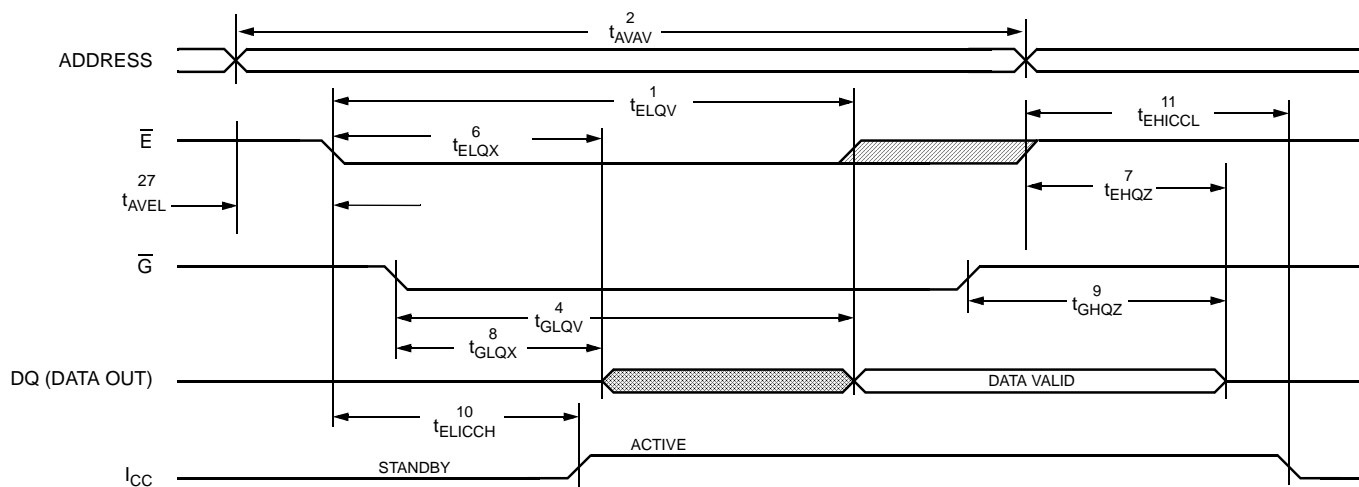
Note h: Device is continuously selected with \overline{E} and \overline{G} both low.

Note i: Measured $\pm 200mV$ from steady state output voltage.

SRAM READ CYCLE #1: Address Controlled^{g, h}



SRAM READ CYCLE #2: \overline{E} and \overline{G} Controlled^g



SRAM WRITE CYCLES #1 & #2

($V_{CC} = 5.0V \pm 10\%$)^e

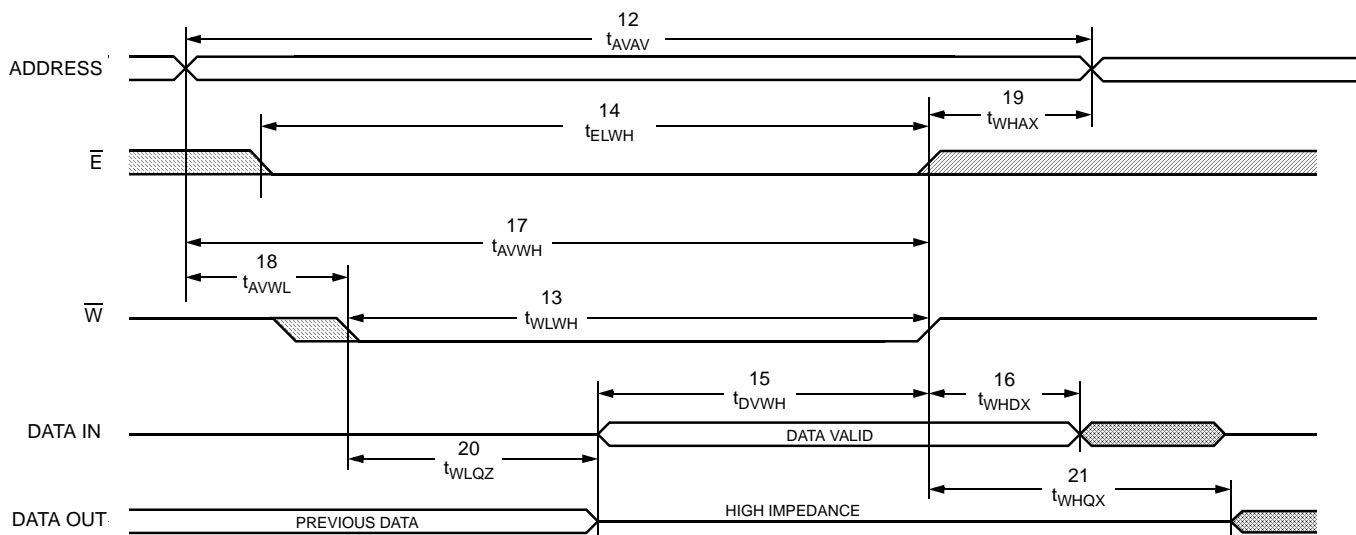
NO.	SYMBOLS			PARAMETER	STK12C68, STK12C68-5-25		STK12C68, STK12C68-5-35		STK12C68, STK12C68-5-45		STK12C68, STK12C68-5-55		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		55		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		45		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		45		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		12		15		25		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		30		45		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		0		0		0		ns
20	$t_{WLQZ}^{i,j}$		t_{WZ}	Write Enable to Output Disable		10		13		14		15	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write	5		5		5		5		ns

Note j: If \bar{W} is low when \bar{E} goes low, the outputs remain in the high-impedance state.

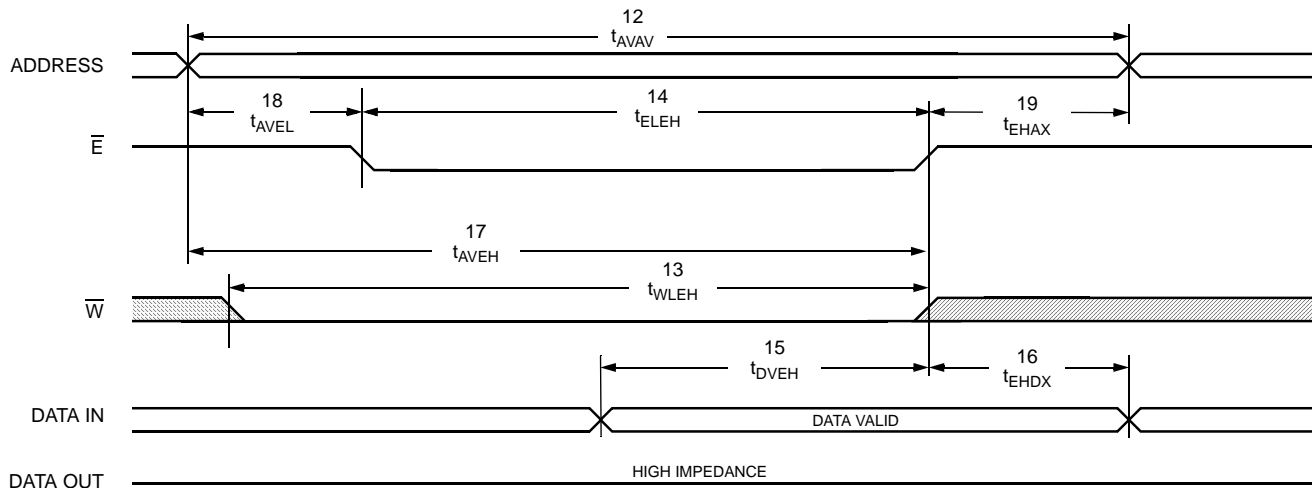
Note k: \bar{E} or \bar{W} must be $\geq V_{IH}$ during address transitions.

Note l: HSB must be high during SRAM WRITE cycles.

SRAM WRITE CYCLE #1: \bar{W} Controlled^{k, l}



SRAM WRITE CYCLE #2: \bar{E} Controlled^{k, l}



HARDWARE MODE SELECTION

\overline{E}	\overline{W}	\overline{HSB}	A ₁₂ - A ₀ (hex)	MODE	I/O	POWER	NOTES
H	X	H	X	Not Selected	Output High Z	Standby	
L	H	H	X	Read SRAM	Output Data	Active	o
L	L	H	X	Write SRAM	Input Data	Active	
X	X	L	X	Nonvolatile <i>STORE</i>	Output High Z	I _{CC2}	m
L	H	H	0000	Read SRAM	Output Data	Active	n, o
			1555	Read SRAM	Output Data		
			0AAA	Read SRAM	Output Data		
			1FFF	Read SRAM	Output Data		
			10F0	Read SRAM	Output Data		
			0F0F	Nonvolatile <i>STORE</i>	Output High Z		
L	H	H	0000	Read SRAM	Output Data	Active	n, o
			1555	Read SRAM	Output Data		
			0AAA	Read SRAM	Output Data		
			1FFF	Read SRAM	Output Data		
			10F0	Read SRAM	Output Data		
			0F0E	Nonvolatile <i>RECALL</i>	Output High Z		

Note m: \overline{HSB} *STORE* operation occurs only if an SRAM WRITE has been done since the last nonvolatile cycle. After the *STORE* (if any) completes, the part will go into standby mode, inhibiting all operations until \overline{HSB} rises.

Note n: The six consecutive addresses must be in the order listed. \overline{W} must be high during all six consecutive \overline{E} controlled cycles to enable a nonvolatile cycle.

Note o: I/O state assumes $\overline{G} \leq V_{IL}$. Activation of nonvolatile cycles does not depend on state of \overline{G} .

HARDWARE STORE CYCLE

(V_{CC} = 5.0V ± 10%)^e

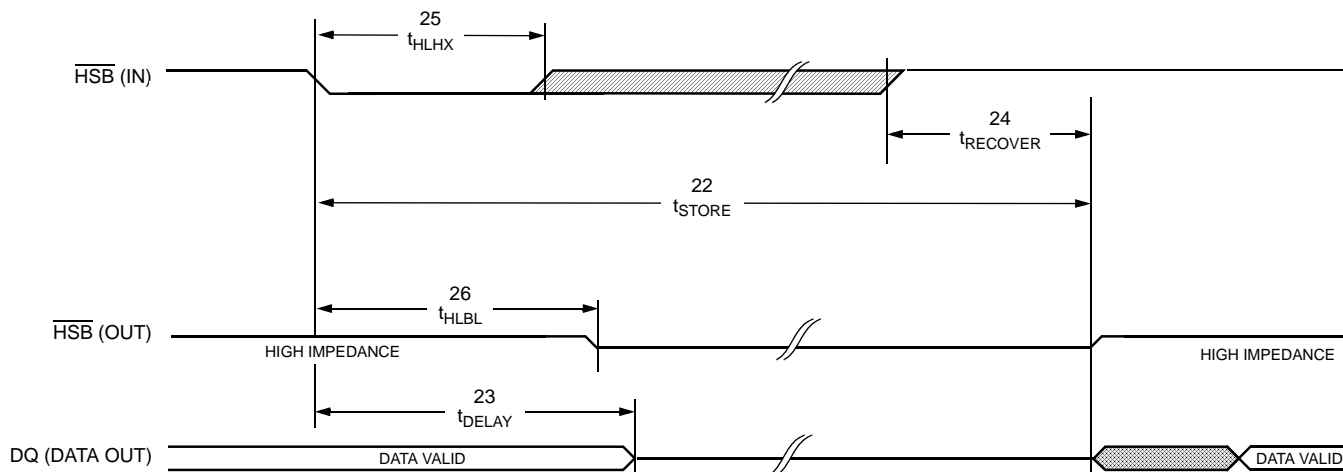
NO.	SYMBOLS		PARAMETER	STK12C68, STK12C68-5		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
22	t _{STORE}	t _{HLHZ}	<i>STORE</i> Cycle Duration		10	ms	i, p
23	t _{DELAY}	t _{HLQZ}	Time Allowed to Complete SRAM Cycle	1		μs	i, q
24	t _{RECOVER}	t _{HHQX}	Hardware <i>STORE</i> High to Inhibit Off		700	ns	p, r
25	t _{HLHX}		Hardware <i>STORE</i> Pulse Width	15		ns	
26	t _{HLBL}		Hardware <i>STORE</i> Low to Store Busy		300	ns	

Note p: \overline{E} and \overline{G} low for output behavior.

Note q: \overline{E} and \overline{G} low and \overline{W} high for output behavior.

Note r: t_{RECOVER} is only applicable after t_{STORE} is complete.

HARDWARE STORE CYCLE



AutoStore™/POWER-UP RECALL

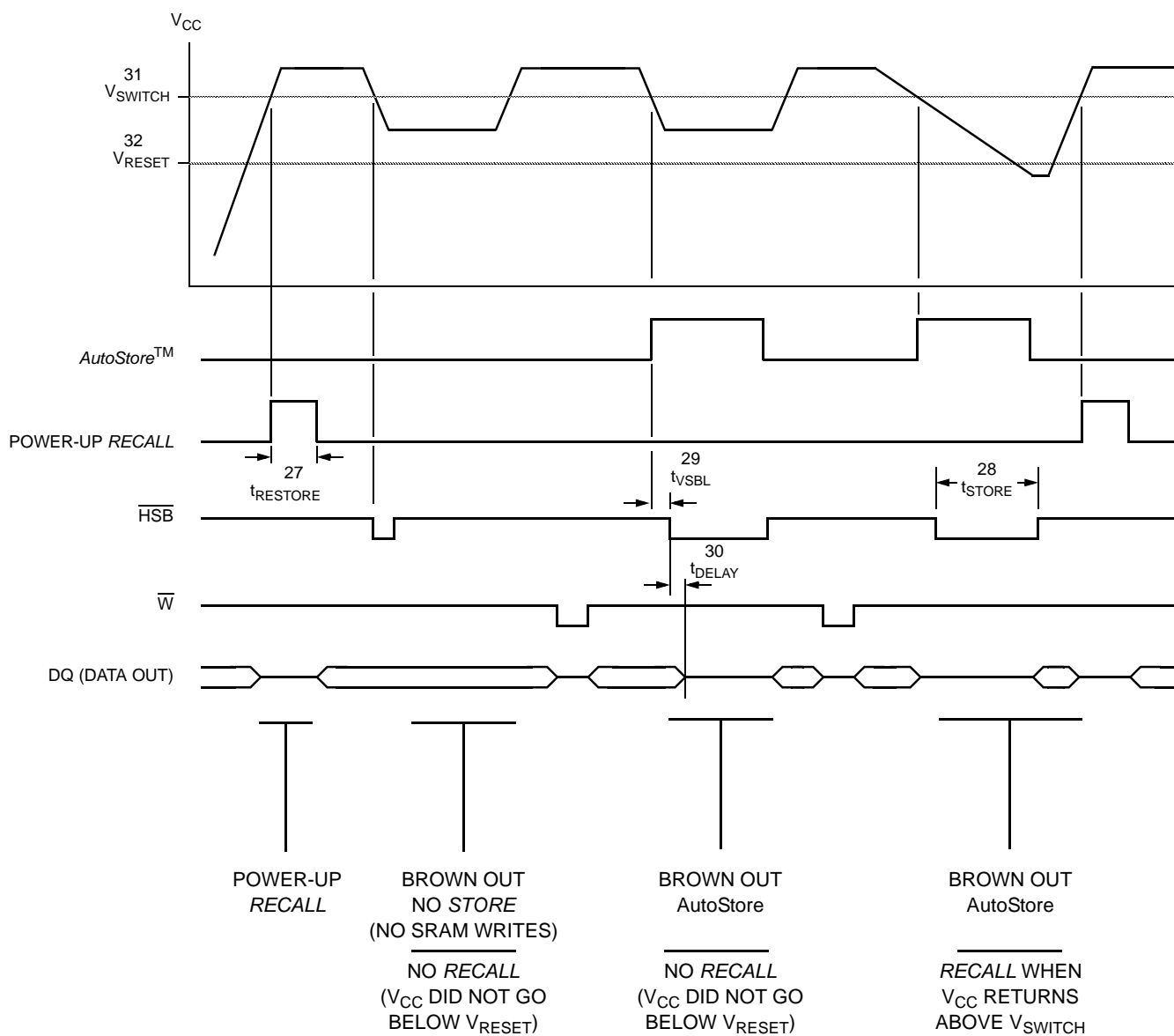
($V_{CC} = 5.0V \pm 10\%$)^e

NO.	SYMBOLS		PARAMETER	STK12C68, STK12C68-5		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
27	$t_{RESTORE}$		Power-up <i>RECALL</i> Duration		550	μ s	s
28	t_{STORE}	t_{HLHZ}	<i>STORE</i> Cycle Duration		10	ms	p, q, t
29	t_{VSBL}		Low Voltage Trigger (V_{SWITCH}) to \overline{HSB} Low		300	ns	l
30	t_{DELAY}	t_{BLQZ}	Time Allowed to Complete SRAM Cycle	1		μ s	p
31	V_{SWITCH}		Low Voltage Trigger Level	4.0	4.5	V	
32	V_{RESET}		Low Voltage Reset Level		3.9	V	

Note s: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH} .

Note t: \overline{HSB} is asserted low for 1μ s when V_{CAP} drops through V_{SWITCH} . If an SRAM WRITE has not taken place since the last nonvolatile cycle, \overline{HSB} will be released and no *STORE* will take place.

AutoStore™/POWER-UP RECALL



STK12C68, STK12C68-5 (SMD5962-94599)

SOFTWARE-CONTROLLED STORE/RECALL CYCLE^v

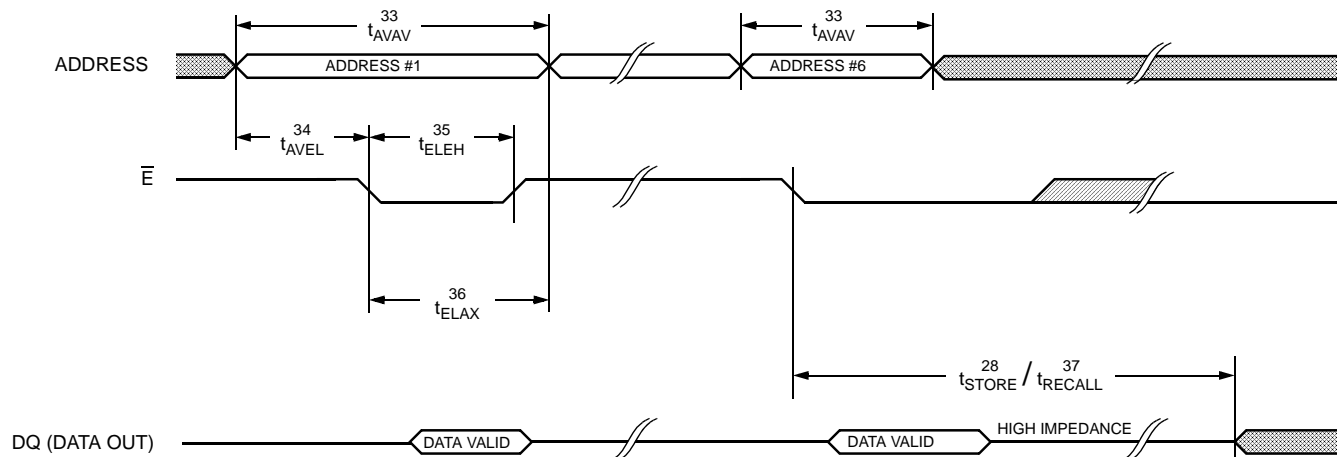
($V_{CC} = 5.0V \pm 10\%$)^e

NO.	SYMBOLS		PARAMETER	STK12C68, STK12C68-5-25		STK12C68, STK12C68-5-35		STK12C68, STK12C68-5-45		STK12C68, STK12C68-5-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
33	t_{AVAV}	t_{RC}	STORE/RECALL Initiation Cycle Time	25		35		45		55		ns	p
34	t_{AVEL}	t_{AS}	Address Set-up Time	0		0		0		0		ns	u
35	t_{ELEH}	t_{CW}	Clock Pulse Width	20		25		30		30		ns	u
36	t_{ELAX}		Address Hold Time	20		20		20		20		ns	u
37	t_{RECALL}		RECALL Duration		20		20		20		20	μ s	

Note u: The software sequence is clocked on the falling edge of \bar{E} without involving \bar{G} (double clocking will abort the sequence). See application note: MA0002 <http://www.simtek.com/attachments/AppNote02.pdf>.

Note v: The six consecutive addresses must be in the order listed in the Software STORE/RECALL Mode Selection Table: (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a STORE cycle or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a RECALL cycle. \bar{W} must be high during all six consecutive cycles.

SOFTWARE STORE/RECALL CYCLE: \bar{E} Controlled^v



DEVICE OPERATION

The STK12C68, STK12C68-5 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to Nonvolatile Elements (the *STORE* operation) or from Nonvolatile Elements to SRAM (the *RECALL* operation). In this mode SRAM functions are disabled.

NOISE CONSIDERATIONS

The STK12C68, STK12C68-5 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately $0.1\mu\text{F}$ connected between V_{CAP} and V_{SS} , using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM READ

The STK12C68, STK12C68-5 performs a *READ* cycle whenever $\overline{\text{E}}$ and $\overline{\text{G}}$ are low and $\overline{\text{W}}$ and $\overline{\text{HSB}}$ are high. The address specified on pins A_{0-12} determines which of the 8,192 data bytes will be accessed. When the *READ* is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (*READ* cycle #1). If the *READ* is initiated by $\overline{\text{E}}$ or $\overline{\text{G}}$, the outputs will be valid at t_{ELQV} or at t_{GLQV} , whichever is later (*READ* cycle #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{\text{E}}$ or $\overline{\text{G}}$ is brought high, or $\overline{\text{W}}$ or $\overline{\text{HSB}}$ is brought low.

SRAM WRITE

A *WRITE* cycle is performed whenever $\overline{\text{E}}$ and $\overline{\text{W}}$ are low and $\overline{\text{HSB}}$ is high. The address inputs must be stable prior to entering the *WRITE* cycle and must remain stable until either $\overline{\text{E}}$ or $\overline{\text{W}}$ goes high at the end of the cycle. The data on the common I/O pins DQ_{0-7} will be written into the memory if it is valid t_{DWH} before the end of a $\overline{\text{W}}$ controlled *WRITE* or t_{DVEH} before the end of an $\overline{\text{E}}$ controlled *WRITE*.

It is recommended that $\overline{\text{G}}$ be kept high during the entire *WRITE* cycle to avoid data bus contention on common I/O lines. If $\overline{\text{G}}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{\text{W}}$ goes low.

POWER-UP RECALL

During power up, or after any low-power condition ($V_{\text{CAP}} < V_{\text{RESET}}$), an internal *RECALL* request will be latched. When V_{CAP} once again exceeds the sense voltage of V_{SWITCH} , a *RECALL* cycle will automatically be initiated and will take t_{RESTORE} to complete.

If the STK12C68, STK12C68-5 is in a *WRITE* state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected either between $\overline{\text{W}}$ and system V_{CC} or between $\overline{\text{E}}$ and system V_{CC} .

SOFTWARE NONVOLATILE STORE

The STK12C68, STK12C68-5 software *STORE* cycle is initiated by executing sequential $\overline{\text{E}}$ controlled *READ* cycles from six specific address locations. During the *STORE* cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of *READ*s from specific addresses is used for *STORE* initiation, it is important that no other *READ* or *WRITE* accesses intervene in the sequence, or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To initiate the software *STORE* cycle, the following *READ* sequence must be performed:

- | | | |
|-----------------|------------|-----------------------------|
| 1. Read address | 0000 (hex) | Valid <i>READ</i> |
| 2. Read address | 1555 (hex) | Valid <i>READ</i> |
| 3. Read address | 0AAA (hex) | Valid <i>READ</i> |
| 4. Read address | 1FFF (hex) | Valid <i>READ</i> |
| 5. Read address | 10F0 (hex) | Valid <i>READ</i> |
| 6. Read address | 0F0F (hex) | Initiate <i>STORE</i> cycle |

The software sequence must be clocked with $\overline{\text{E}}$ controlled *READ*s.

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that *READ* cycles and not *WRITE* cycles be used in the sequence, although it is not necessary that $\overline{\text{G}}$ be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for *READ* and *WRITE* operation.

SOFTWARE NONVOLATILE RECALL

A software *RECALL* cycle is initiated with a sequence of READ operations in a manner similar to the software *STORE* initiation. To initiate the *RECALL* cycle, the following sequence of \bar{E} controlled READ operations must be performed:

1.	Read address	0000 (hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0E (hex)	Initiate <i>RECALL</i> cycle

Internally, *RECALL* is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The *RECALL* operation in no way alters the data in the Nonvolatile Elements. The nonvolatile data can be recalled an unlimited number of times.

AutoStore MODE

The STK12C68, STK12C68-5 can be powered in one of three modes.

During normal AutoStore operation, the STK12C68, STK12C68-5 will draw current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single *STORE* operation. After power up, when the voltage on the V_{CAP} pin drops below V_{SWITCH} , the part will automatically disconnect the V_{CAP} pin from V_{CC} and initiate a *STORE* operation.

Figure 2 shows the proper connection of capacitors for automatic store operation. A charge storage capacitor having a capacity of between $68\mu\text{F}$ and $220\mu\text{F}$ ($\pm 20\%$) rated at 6V should be provided.

In system power mode, both V_{CC} and V_{CAP} are connected to the + 5V power supply without the $68\mu\text{F}$ capacitor. In this mode the AutoStore function of the STK12C68, STK12C68-5 will operate on the stored system charge as power goes down. The user must, however, guarantee that V_{CC} does not drop below 3.6V during the 10ms *STORE* cycle.

AutoStore INHIBIT MODE

If an automatic *STORE* on power loss is not required, then V_{CC} can be tied to ground and + 5V applied to

V_{CAP} (Figure 3). This is the AutoStore Inhibit mode, in which the AutoStore function is disabled. If the STK12C68, STK12C68-5 is operated in this configuration, references to V_{CC} should be changed to V_{CAP} throughout this data sheet. In this mode, *STORE* operations may be triggered through software control or the HSB pin. To enable or disable AutoStore using an IO port pin, see "PREVENTING STORES" on page 11.

In order to prevent unneeded *STORE* operations, automatic *STORES* as well as those initiated by externally driving HSB low will be ignored unless at least one WRITE operation has taken place since the most recent *STORE* or *RECALL* cycle. Software initiated *STORE* cycles are performed regardless of whether a WRITE operation has taken place. An optional pull-up resistor is shown connected to HSB. This can be used to signal the system that the AutoStore cycle is in progress.

If the power supply drops faster than $20 \mu\text{s/volt}$ before V_{CC} reaches V_{SWITCH} , then a 2.2 ohm resistor should be inserted between V_{CC} and the system supply to avoid momentary excess of current between V_{CC} and V_{cap} .

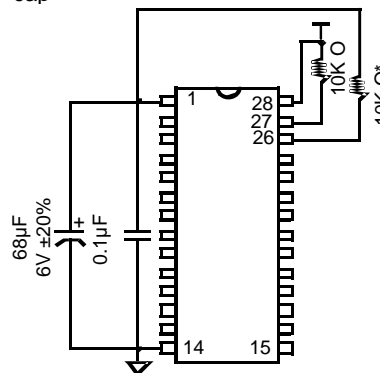


Figure 2: AutoStore Mode
*If HSB is not used, it should be left unconnected.

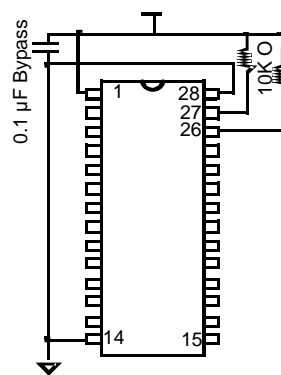


Figure 3: AutoStore Inhibit Mode

HSB OPERATION

The STK12C68, STK12C68-5 provides the $\overline{\text{HSB}}$ pin for controlling and acknowledging the *STORE* operations. The $\overline{\text{HSB}}$ pin is used to request a hardware *STORE* cycle. When the $\overline{\text{HSB}}$ pin is driven low, the STK12C68, STK12C68-5 will conditionally initiate a *STORE* operation after t_{DELAY} ; an actual *STORE* cycle will only begin if a *WRITE* to the SRAM took place since the last *STORE* or *RECALL* cycle. The $\overline{\text{HSB}}$ pin has a very resistive pullup and is internally driven low to indicate a busy condition while the *STORE* (initiated by any means) is in progress.

SRAM *READ* and *WRITE* operations that are in progress when $\overline{\text{HSB}}$ is driven low by any means are given time to complete before the *STORE* operation is initiated. After $\overline{\text{HSB}}$ goes low, the STK12C68, STK12C68-5 will continue SRAM operations for $t_{\text{DE-LAY}}$. During t_{DELAY} , multiple SRAM *READ* operations may take place. If a *WRITE* is in progress when $\overline{\text{HSB}}$ is pulled low it will be allowed a time, t_{DELAY} to complete. However, any SRAM *WRITE* cycles requested after $\overline{\text{HSB}}$ goes low will be inhibited until $\overline{\text{HSB}}$ returns high.

The $\overline{\text{HSB}}$ pin can be used to synchronize multiple STK12C68, STK12C68-5s while using a single larger capacitor. To operate in this mode the $\overline{\text{HSB}}$ pin should be connected together to the $\overline{\text{HSB}}$ pins from the other STK12C68, STK12C68-5s. An external pull-up resistor to +5V is required since $\overline{\text{HSB}}$ acts as an open drain pull down. The V_{CAP} pins from the other STK12C68, STK12C68-5 parts can be tied together and share a single capacitor. The capacitor size must be scaled by the number of devices connected to it. When any one of the STK12C68, STK12C68-5s detects a power loss and asserts $\overline{\text{HSB}}$, the common $\overline{\text{HSB}}$ pin will cause all parts to request a *STORE* cycle (a *STORE* will take place in those STK12C68, STK12C68-5s that have been written since the last nonvolatile cycle).

During any *STORE* operation, regardless of how it was initiated, the STK12C68, STK12C68-5 will continue to drive the $\overline{\text{HSB}}$ pin low, releasing it only when the *STORE* is complete. Upon completion of the *STORE* operation the STK12C68, STK12C68-5 will remain disabled until the $\overline{\text{HSB}}$ pin returns high.

If $\overline{\text{HSB}}$ is not used, it should be left unconnected.

PREVENTING STORES

The *STORE* function can be disabled on the fly by holding $\overline{\text{HSB}}$ high with a driver capable of sourcing 30mA at a V_{OH} of at least 2.2V, as it will have to overpower the internal pull-down device that drives $\overline{\text{HSB}}$ low for 20 μ s at the onset of a *STORE*. When the STK12C68, STK12C68-5 is connected for AutoStore operation (system V_{CC} connected to V_{CC} and a 68 μ F capacitor on V_{CAP}) and V_{CC} crosses V_{SWITCH} on the way down, the STK12C68, STK12C68-5 will attempt to pull $\overline{\text{HSB}}$ low; if $\overline{\text{HSB}}$ doesn't actually get below V_{IL} , the part will stop trying to pull $\overline{\text{HSB}}$ low and abort the *STORE* attempt.

HARDWARE PROTECT

The STK12C68, STK12C68-5 offers hardware protection against inadvertent *STORE* operation and SRAM *WRITES* during low-voltage conditions. When $V_{\text{CAP}} < V_{\text{SWITCH}}$, all externally initiated *STORE* operations and SRAM *WRITES* are inhibited.

AutoStore can be completely disabled by tying V_{CC} to ground and applying +5V to V_{CAP} . This is the AutoStore Inhibit mode; in this mode, *STORES* are only initiated by explicit request using either the software sequence or the $\overline{\text{HSB}}$ pin.

LOW AVERAGE ACTIVE POWER

The STK12C68, STK12C68-5 draws significantly less current when it is cycled at times longer than 50ns. Figure 4 shows the relationship between I_{CC} and *READ* cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, $V_{\text{CC}} = 5.5\text{V}$, 100% duty cycle on chip enable). Figure 5 shows the same relationship for *WRITE* cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK12C68, STK12C68-5 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of *READS* to *WRITES*; 5) the operating temperature; 6) the V_{CC} level; and 7) I/O loading.

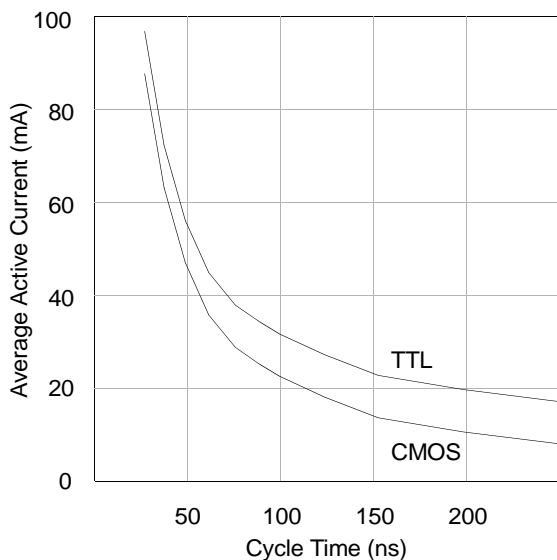


Figure 4: I_{CC} (max) Reads

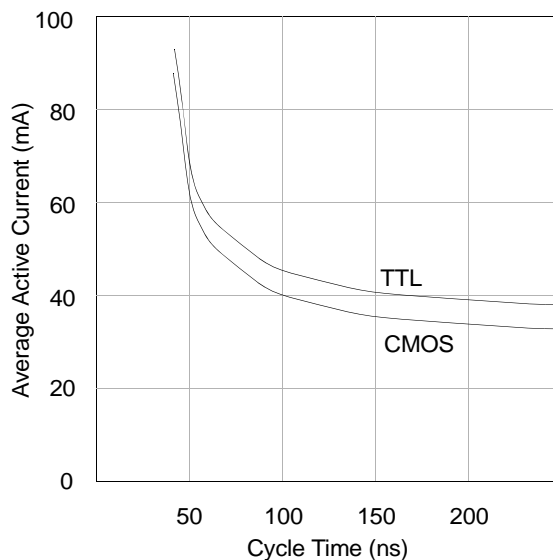


Figure 5: I_{CC} (max) Writes

BEST PRACTICES

nvSRAM products have been used effectively for over 15 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

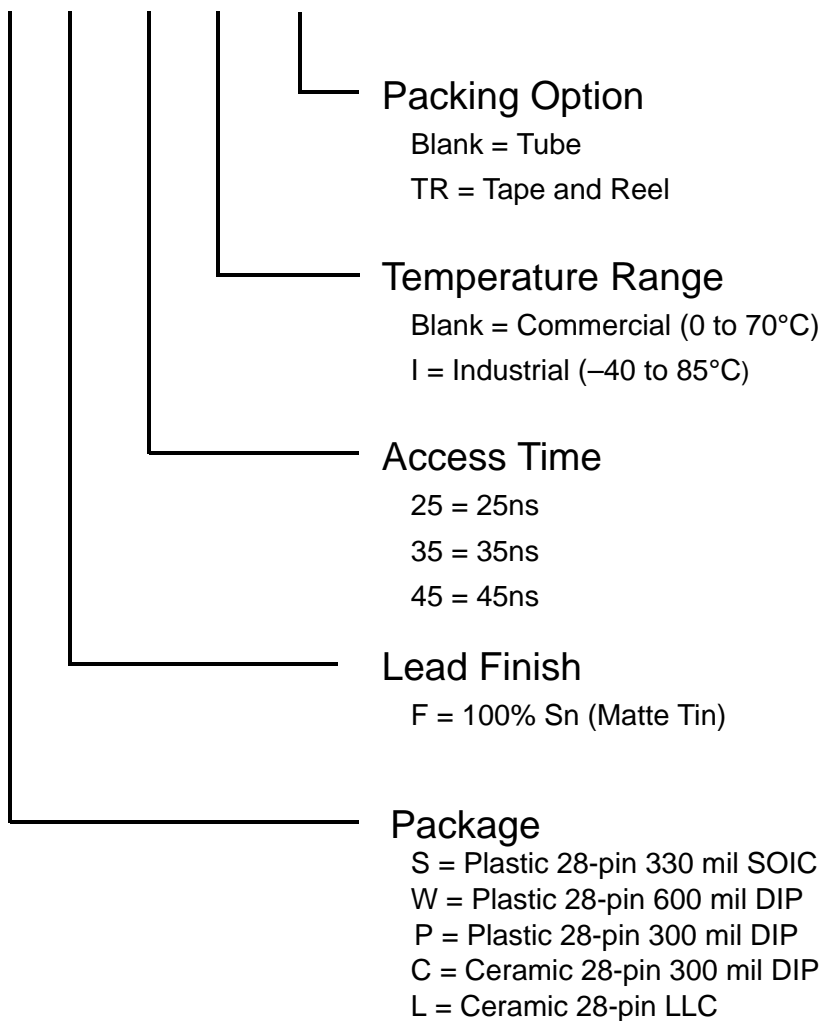
- The non-volatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites will sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, etc. should always program a unique NV pattern (e.g., complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power up boot firmware routines should rewrite the nvSRAM into the desired state. While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the

desired state as a safeguard against events that might flip the bit inadvertently (program bugs, incoming inspection routines, etc.).

- The V_{cap} value specified in this datasheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the max V_{cap} value because the higher inrush currents may reduce the reliability of the internal pass transistor. Customers that want to use a larger V_{cap} value to make sure there is extra store charge should discuss their V_{cap} size selection with Simtek.

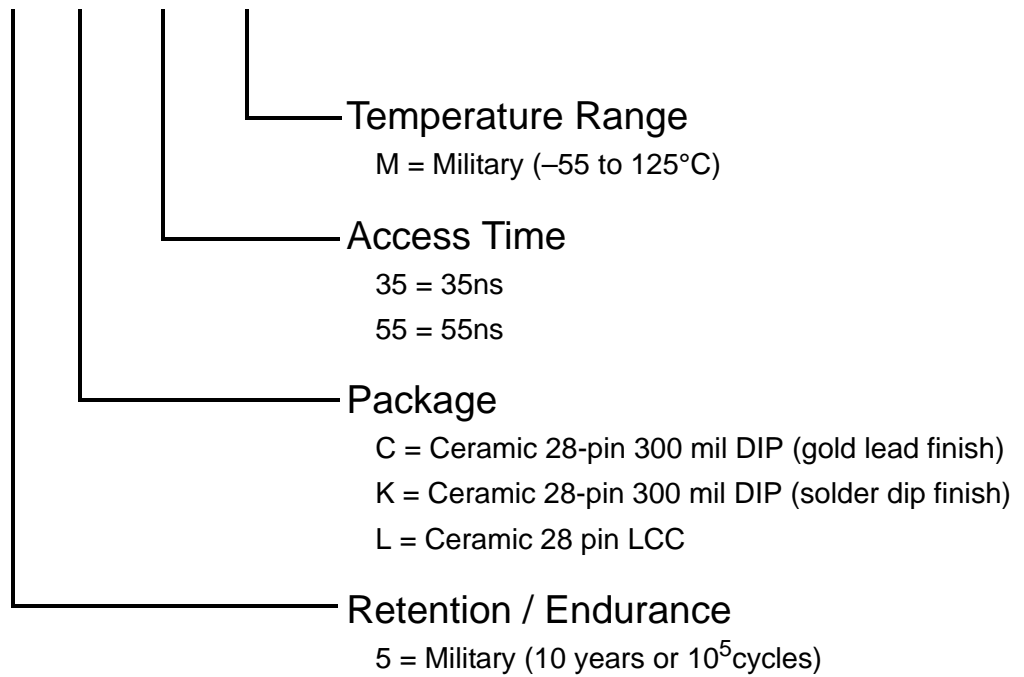
COMMERCIAL AND INDUSTRIAL ORDERING INFORMATION

STK12C68 - S F 45 I TR

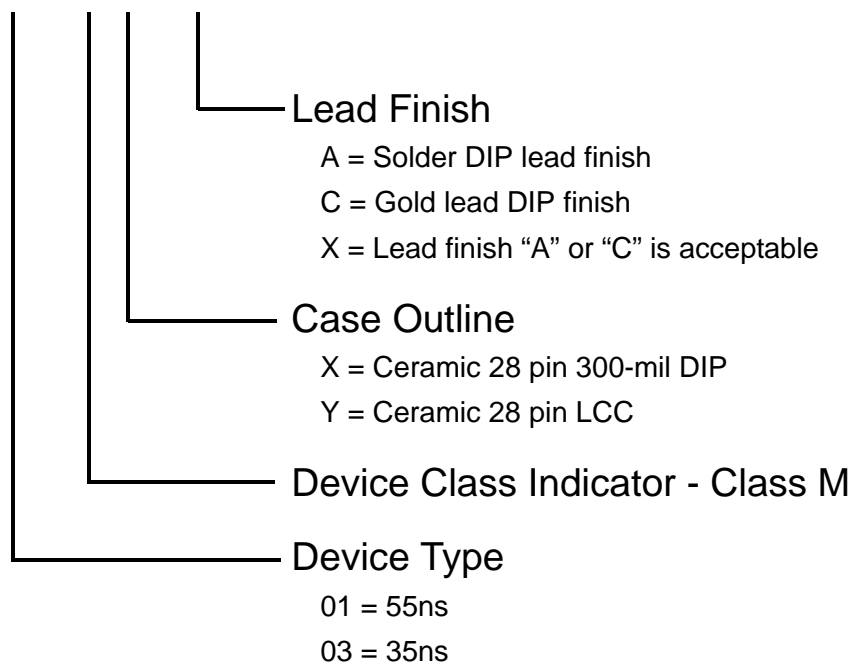


MILITARY ORDERING INFORMATION

STK12C68 - 5 C 35 M



5962 - 94599 01 MX X

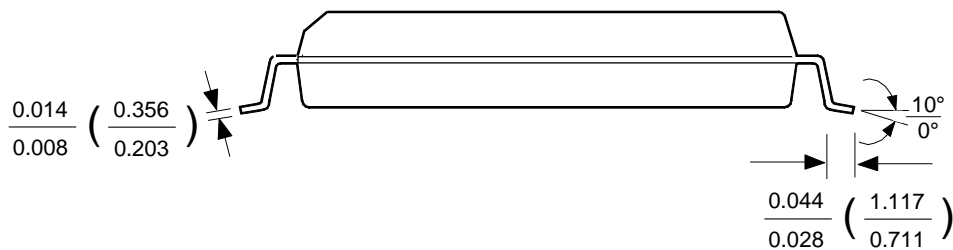
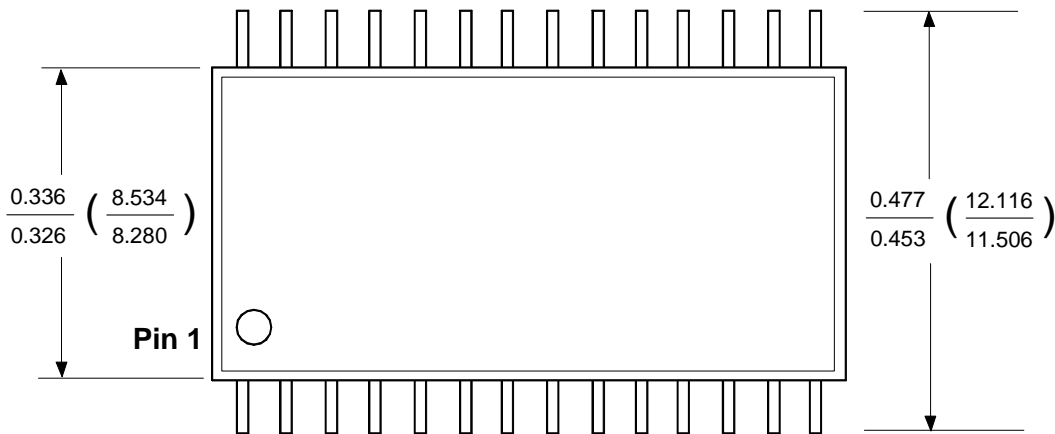
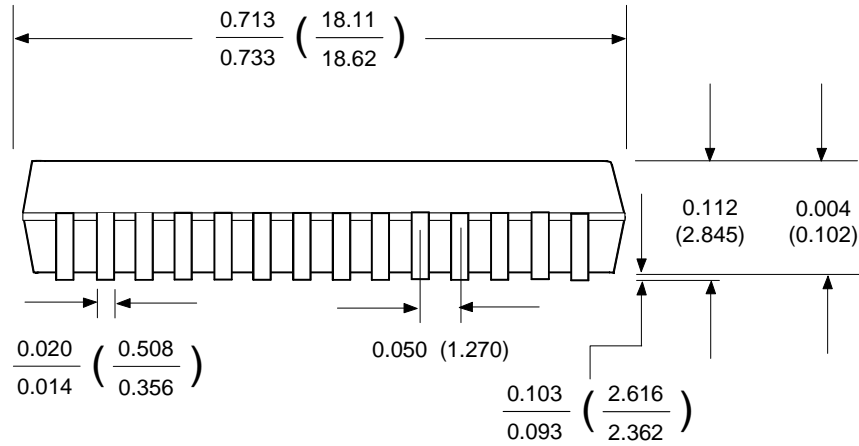


ORDERING INFORMATION

Part Number	Description	Access Times	Temperature
STK12C68-C35	5V 8Kx8 AutoStore nvSRAM CDIP28-300	35 ns access time	Commercial
STK12C68-C45	5V 8Kx8 AutoStore nvSRAM CDIP28-300	45 ns access time	Commercial
STK12C68-L35	5V 8Kx8 AutoStore nvSRAM LCC28	35 ns access time	Commercial
STK12C68-L45	5V 8Kx8 AutoStore nvSRAM LCC28	45 ns access time	Commercial
STK12C68-PF25	5V 8Kx8 AutoStore nvSRAM PDIP28-600	25 ns access time	Commercial
STK12C68-PF45	5V 8Kx8 AutoStore nvSRAM PDIP28-600	45 ns access time	Commercial
STK12C68-SF25	5V 8Kx8 AutoStore nvSRAM SOP28-330	25 ns access time	Commercial
STK12C68-SF25TR	5V 8Kx8 AutoStore nvSRAM SOP28-330	25 ns access time	Commercial
STK12C68-SF45	5V 8Kx8 AutoStore nvSRAM SOP28-330	45 ns access time	Commercial
STK12C68-SF45TR	5V 8Kx8 AutoStore nvSRAM SOP28-330	45 ns access time	Commercial
STK12C68-WF25	5V 8Kx8 AutoStore nvSRAM PDIP28-600	25 ns access time	Commercial
STK12C68-WF45	5V 8Kx8 AutoStore nvSRAM PDIP28-600	45 ns access time	Commercial
STK12C68-C35I	5V 8Kx8 AutoStore nvSRAM CDIP28-300	35 ns access time	Industrial
STK12C68-C45I	5V 8Kx8 AutoStore nvSRAM CDIP28-300	45 ns access time	Industrial
STK12C68-L35I	5V 8Kx8 AutoStore nvSRAM LCC28	35 ns access time	Industrial
STK12C68-L45I	5V 8Kx8 AutoStore nvSRAM LCC28	45 ns access time	Industrial
STK12C68-PF25I	5V 8Kx8 AutoStore nvSRAM PDIP28-600	25 ns access time	Industrial
STK12C68-PF45I	5V 8Kx8 AutoStore nvSRAM PDIP28-600	45 ns access time	Industrial
STK12C68-SF25I	5V 8Kx8 AutoStore nvSRAM SOP28-330	25 ns access time	Industrial
STK12C68-SF25ITR	5V 8Kx8 AutoStore nvSRAM SOP28-330	25 ns access time	Industrial
STK12C68-SF45I	5V 8Kx8 AutoStore nvSRAM SOP28-330	45 ns access time	Industrial
STK12C68-SF45ITR	5V 8Kx8 AutoStore nvSRAM SOP28-330	45 ns access time	Industrial
STK12C68-WF25I	5V 8Kx8 AutoStore nvSRAM PDIP28-600	25 ns access time	Industrial
STK12C68-WF45I	5V 8Kx8 AutoStore nvSRAM PDIP28-600	45 ns access time	Industrial
SMD5962-9459901MXA	5V 8Kx8 AutoStore nvSRAM CDIP28-300	55 ns access time	Military
SMD5962-9459901MXC	5V 8Kx8 AutoStore nvSRAM CDIP28-300	55 ns access time	Military
SMD5962-9459901MXX	5V 8Kx8 AutoStore nvSRAM CDIP28-300	55 ns access time	Military
SMD5962-9459901MYA	5V 8Kx8 AutoStore nvSRAM LCC28	55 ns access time	Military
SMD5962-9459901MYX	5V 8Kx8 AutoStore nvSRAM LCC28	55 ns access time	Military
SMD5962-9459903MXA	5V 8Kx8 AutoStore nvSRAM CDIP28-300	35 ns access time	Military
SMD5962-9459903MXC	5V 8Kx8 AutoStore nvSRAM CDIP28-300	35 ns access time	Military
SMD5962-9459903MXX	5V 8Kx8 AutoStore nvSRAM CDIP28-300	35 ns access time	Military
SMD5962-9459903MYA	5V 8Kx8 AutoStore nvSRAM LCC28	35 ns access time	Military
SMD5962-9459903MYX	5V 8Kx8 AutoStore nvSRAM LCC28	35 ns access time	Military
STK12C68-5C35M	5V 8Kx8 AutoStore nvSRAM CDIP28-300	35 ns access time	Military
STK12C68-5C55M	5V 8Kx8 AutoStore nvSRAM CDIP28-300	35 ns access time	Military
STK12C68-5K35M	5V 8Kx8 AutoStore nvSRAM CDIP28-300	35 ns access time	Military
STK12C68-5K55M	5V 8Kx8 AutoStore nvSRAM CDIP28-300	35 ns access time	Military
STK12C68-5L35M	5V 8Kx8 AutoStore nvSRAM LCC28	35 ns access time	Military
STK12C68-5L55M	5V 8Kx8 AutoStore nvSRAM LCC28	35 ns access time	Military

Package Diagrams

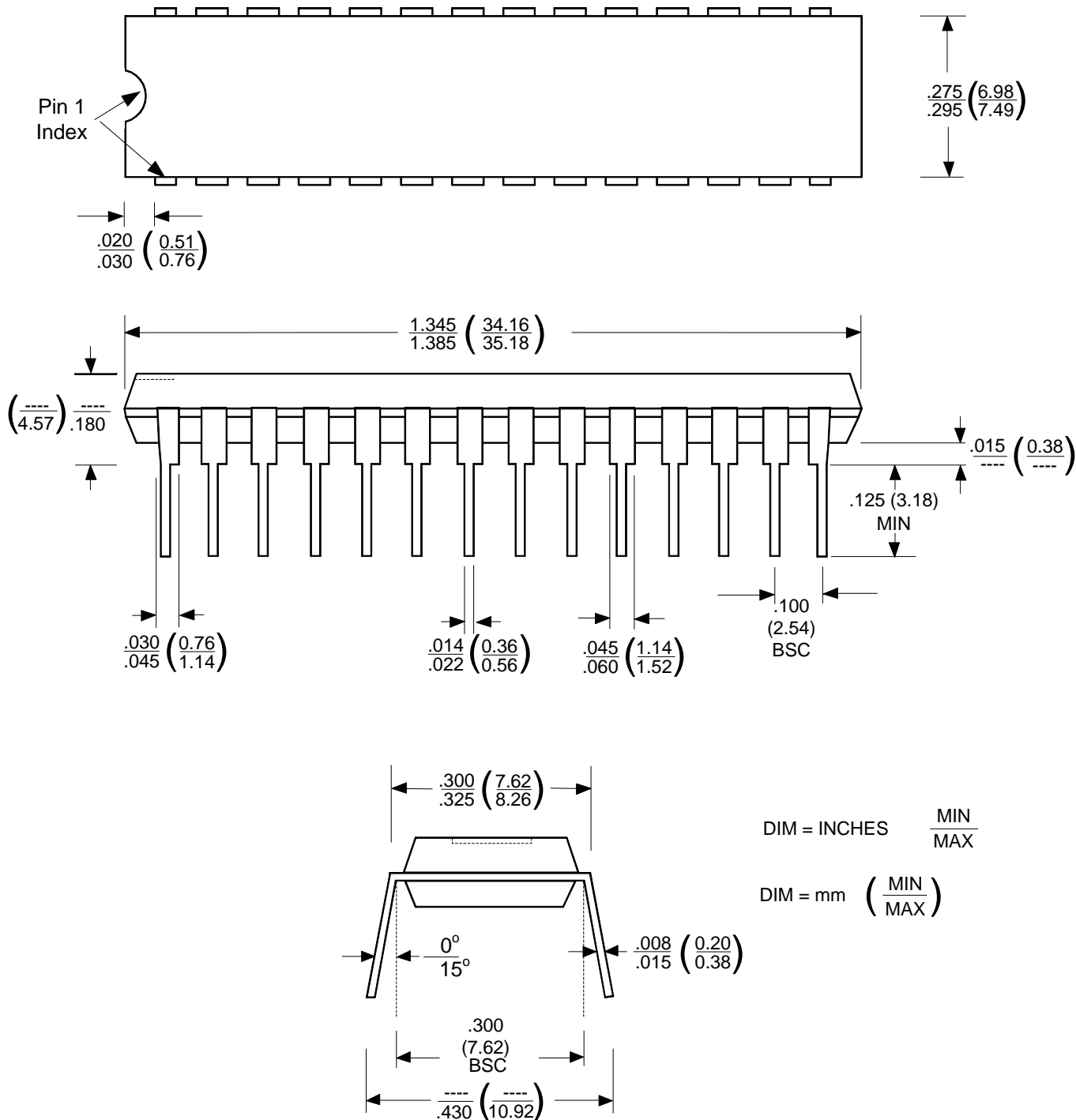
28-Lead, 330 mil SOIC Gull Wing



DIM = INCHES $\frac{\text{MIN}}{\text{MAX}}$

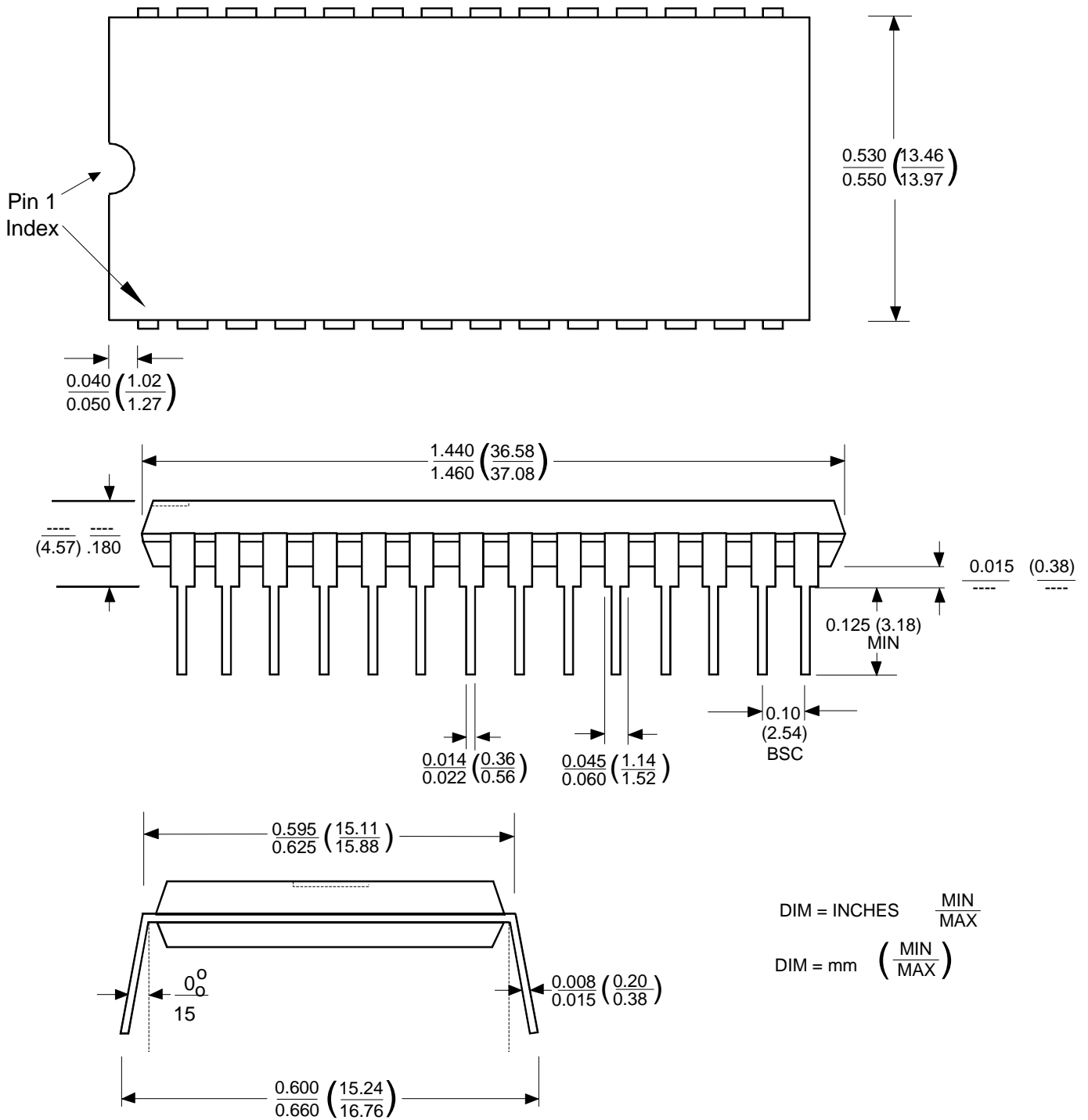
DIM = mm ($\frac{\text{MIN}}{\text{MAX}}$)

28-Lead 300 mil PDIP

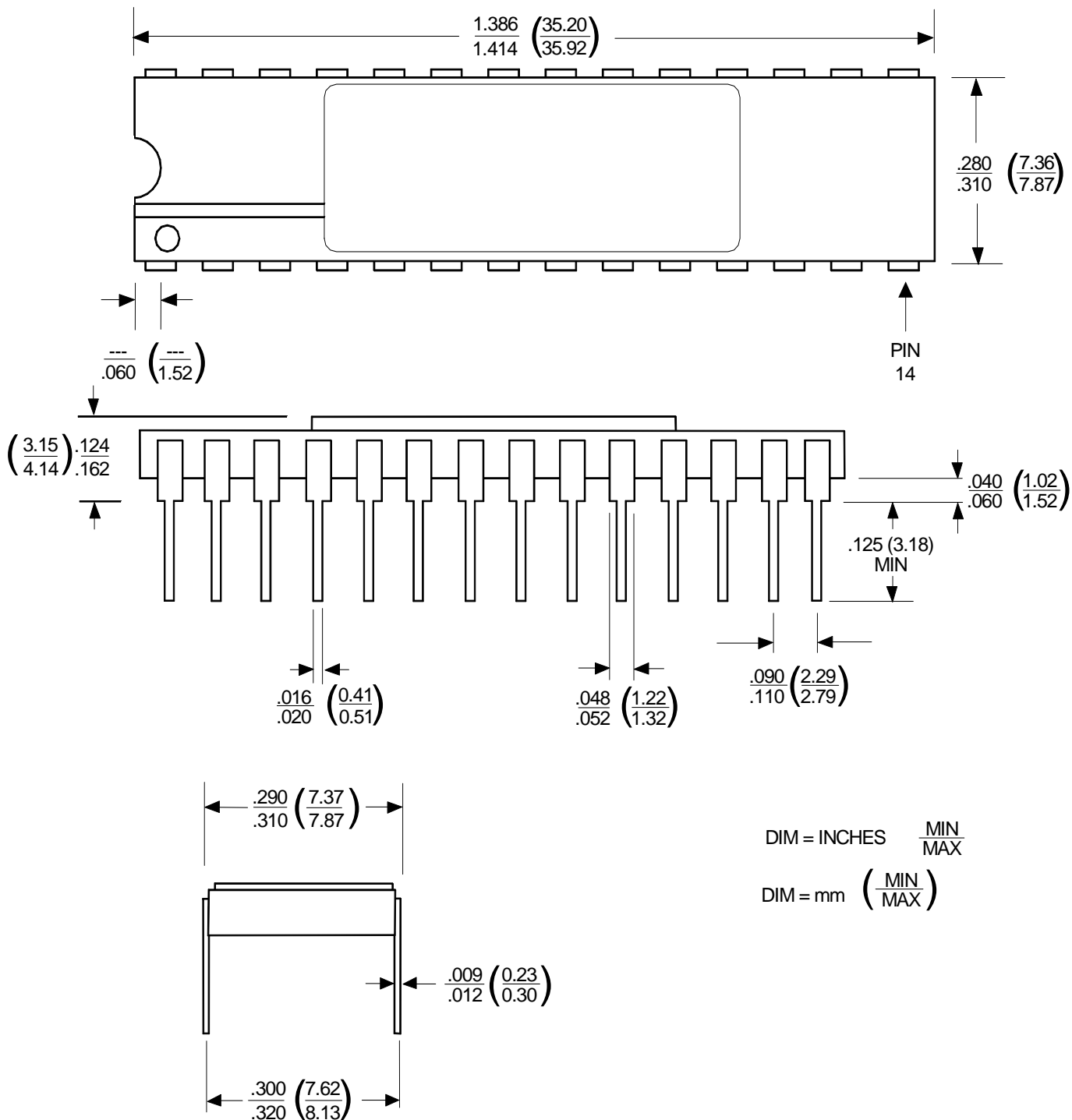


STK12C68, STK12C68-5 (SMD5962-94599)

28-Lead, 600 mil PDIP

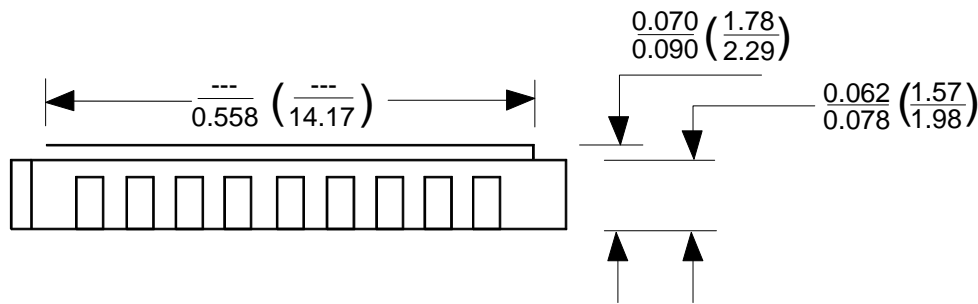
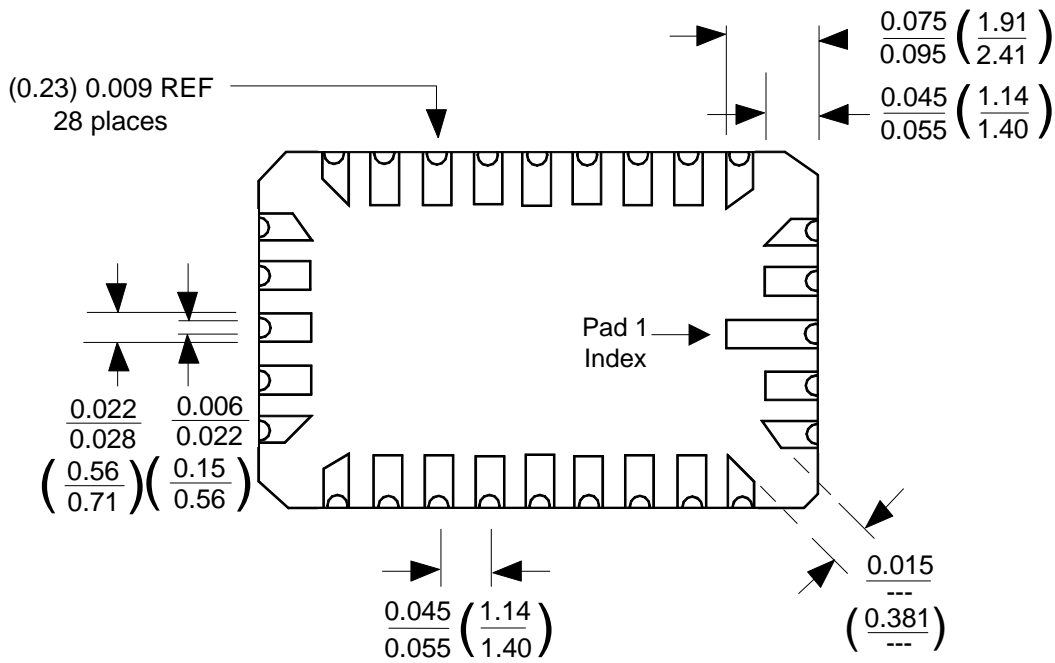
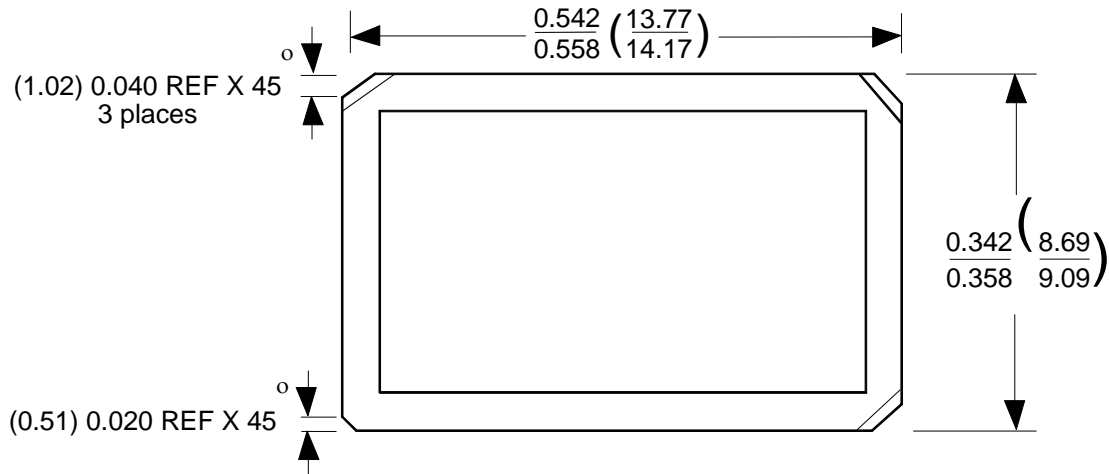


28-Lead, 300 mil Side Braze DIL



STK12C68, STK12C68-5 (SMD5962-94599)

28-Pad, 350 mil Ceramic LCC



DIM = INCHES $\frac{\text{MIN}}{\text{MAX}}$
 DIM = mm ($\frac{\text{MIN}}{\text{MAX}}$)

Document Revision History

Revision	Date	Summary
0.0	December 2002	Combined commercial, industrial and military data sheets. Removed 20 nsec device.
0.1	January 2003	Added 35ns SMD to order information
0.2	July 2003	Added "28 - SOIC" label to page 1 pinout drawing
0.3	September 2003	Added lead-free lead finish
0.4	October 2003	Restored "W" 600 mil DIP package to ordering information
0.5	March 2006	Removed Commercial 35 ns and leaded lead finish, Removed Military 45ns device
0.6	August 2006	Reformat SMD Ordering Information to SDDC Part Number Format
0.7	February 2007	Add Fast Power-Down Slew Rate Information Restore Comm/Ind C & L Package Options Add Tape Reel Ordering Options Add Product Ordering Code Listing Add Package Outline Drawings Reformat Entire Document
0.8	July 2007	extend definition of t_{HZ} (#7) update fig. SRAM READ CYCLE #2, SRAM WRITE CYCLE #1, update notes in tables HARDWARE STORE CYCLE, AutoStore / POWER_UP RECALL, update Note s and Note u split off SOFTWARE STORE / RECALL MODE SELEKTION table to clarify product usage
2.0	June 2008	Added STK-12C68-5 part number to header. Page 3: in the DC characteristics table, identified access times valid for commercial and industrial applications only; referred users to Website for package thermal characteristics. Page 4: in SRAM Read Cycles #1 & #2 table, revised description for t_{ELQX} and t_{ELQX} , and changed Symbol #2 to t_{ELEH} for Read Cycle Time; updated SRAM Read Cycle #2 timing diagram and changed title to add \bar{G} controlled. Page 11: under HSB Operation, revised first paragraph to read "The \bar{HSB} pin has a very resistive pullup..." Page 14: added access time column to table.

SIMTEK STK12C68, STK12C68-5 Datasheet, June 2008

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