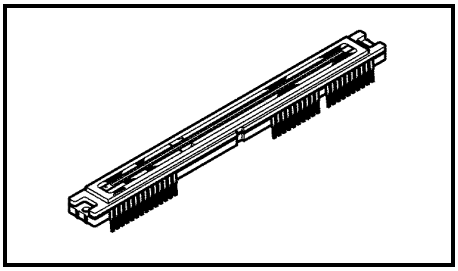
TOSHIBA CCD Linear Image Sensor CCD (Charge Coupled Device)

TCD2706DG

The TCD2706DG is a high sensitive and low dark current 7500 pixels × 3 line CCD color image sensor. The sensor is designed for color scanner.

The device contains a row of 7500 pixels × 3 line photodiodes which provide a 24 lines/mm across a A3 size paper.

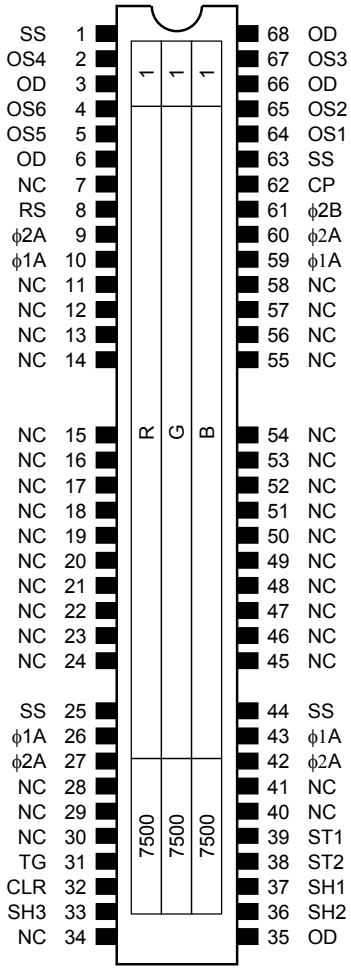


Weight: 16.0 g (typ.)

Features

- Number of image sensing pixels : 22500 pixels (7500 pixels × 3 line)
- Image sensing pixels size : 9.325 μm by 5.5 μm on 9.325 μm center
- Photo sensing region : High sensitive pn photodiode
- Clock : 2-phase (5 V)
- Distance between photodiode array
  : Pixel R to pixel G: 18.65 μm (2 lines)
  Pixel G to pixel B: 18.65 μm (2 lines)
- Internal circuit : Clamp circuit
- Package : 68-pin CERDIP
- Color filter : Red, Green, Blue

Pin Connections (top view)

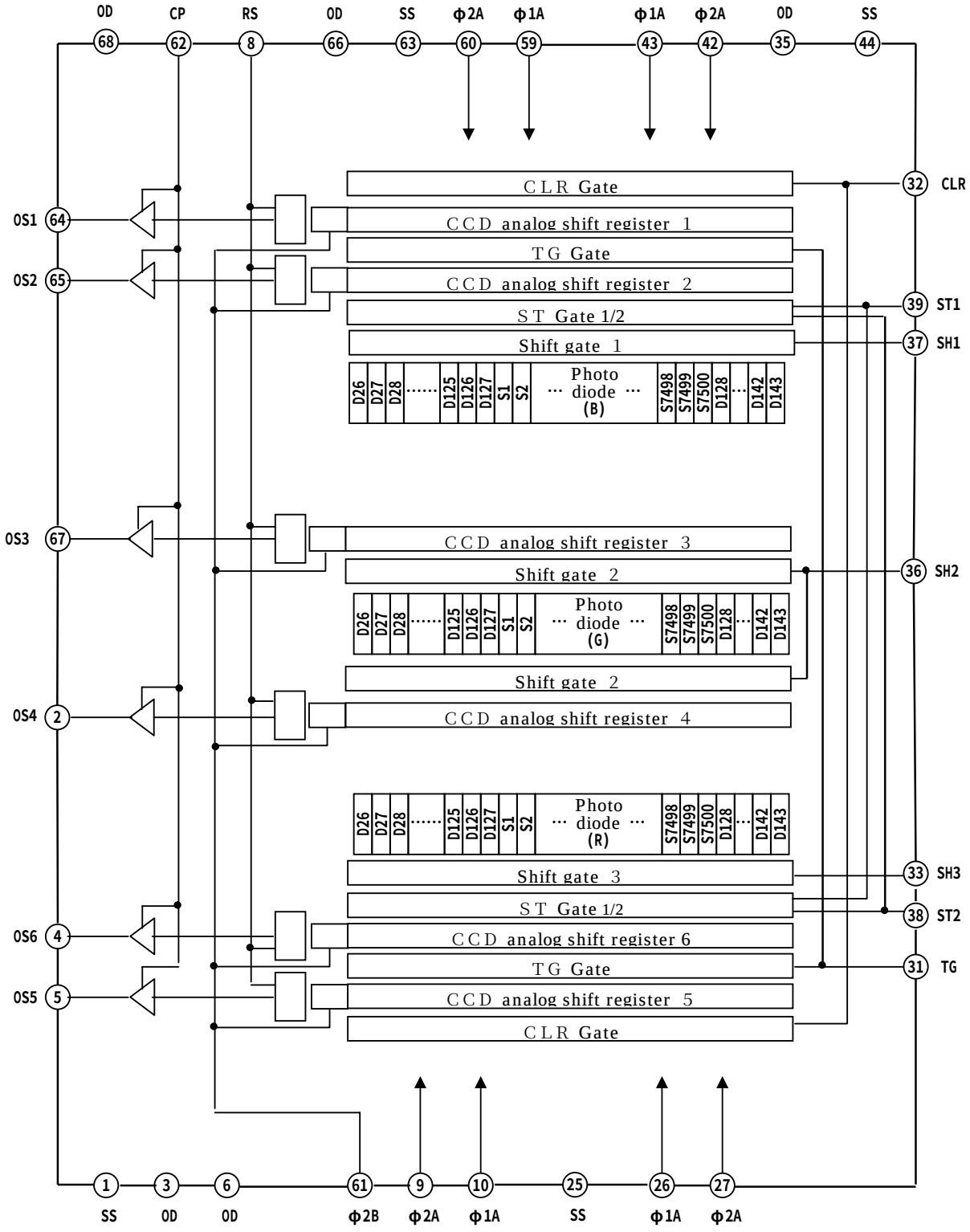


Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Clock pulse voltage	$V_{\phi A}$	−0.3~8	V
Last stage clock pulse voltage	$V_{\phi B}$		
Shift pulse voltage	V_{SH}		
Reset pulse voltage	V_{RS}		
Clamp pulse voltage	V_{CP}		
ST pulse voltage	V_{ST}		
TG pulse voltage	V_{TG}		
CLR pulse voltage	V_{CLR}		
Power supply voltage	V_{OD}	−0.3~15	V
Operating temperature	t_{opr}	0~60	°C
Storage temperature	t_{stg}	−25~85	°C

Note 1: All voltages are with respect to SS pins (ground)

Circuit Diagram



Pin Names

Pin No.	Symbol	Name	Pin No.	Symbol	Name
1	SS	Ground	35	OD	Power supply
2	OS4	Output signal 4 (GREEN)	36	SH2	Shift gate 2
3	OD	Power supply	37	SH1	Shift gate 1
4	OS6	Output signal 6 (RED)	38	ST2	ST Gate 2
5	OS5	Output signal 5 (RED)	39	ST1	ST Gate 1
6	OD	Power supply	40	NC	No connect
7	NC	No connect	41	NC	No connect
8	RS	Reset gate	42	ϕ2A	Transfer clock (phase 2)
9	ϕ2A	Transfer clock (phase 2)	43	ϕ1A	Transfer clock (phase 1)
10	ϕ1A	Transfer clock (phase 1)	44	SS	Ground
11	NC	No connect	45	NC	No connect
12	NC	No connect	46	NC	No connect
13	NC	No connect	47	NC	No connect
14	NC	No connect	48	NC	No connect
15	NC	No connect	49	NC	No connect
16	NC	No connect	50	NC	No connect
17	NC	No connect	51	NC	No connect
18	NC	No connect	52	NC	No connect
19	NC	No connect	53	NC	No connect
20	NC	No connect	54	NC	No connect
21	NC	No connect	55	NC	No connect
22	NC	No connect	56	NC	No connect
23	NC	No connect	57	NC	No connect
24	NC	No connect	58	NC	No connect
25	SS	Ground	59	ϕ1A	Transfer clock (phase 1)
26	ϕ1A	Transfer clock (phase 1)	60	ϕ2A	Transfer clock (phase 2)
27	ϕ2A	Transfer clock (phase 2)	61	ϕ2B	Last stage clock (phase 2)
28	NC	No connect	62	CP	Clamp gate
29	NC	No connect	63	SS	Ground
30	NC	No connect	64	OS1	Output signal 1 (BLUE)
31	TG	TG Gate	65	OS2	Output signal 2 (BLUE)
32	CLR	CLR Gate	66	OD	Power supply
33	SH3	Shift gate 3	67	OS3	Output signal 3 (GREEN)
34	NC	No connect	68	OD	Power supply

Optical/Electrical Characteristics

(Ta = 25°C, V_{OD} = 10 V, V_ϕ = V_{SH} = V_{RS} = V_{CP}= V_{ST}= V_{TG}= V_{CLR} = 5 V (pulse), f_ϕ = 1 MHz, load resistance = 100 kΩ, t_{INT} (integration time) = 10 ms, light source = A light source + CM500S filter (t = 1.0 mm))

Characteristics		Symbol	Min	Typ.	Max	Unit	Note
Sensitivity	Red	R (R)	6.1	8.8	11.5	V/lx・s	(Note 2)
	Green	R (G)	8.9	12.8	16.6		
	Blue	R (B)	3.1	4.5	5.9		
Photo response non uniformity		PRNU (1)	—	10	20	%	(Note 3)
		PRNU (3)	—	3	12	mV	(Note 4)
Saturation output voltage		V_{SAT}	1.8	2.5	—	V	(Note 5)
Saturation exposure		SE	0.10	—	—	lx・s	(Note 6)
Dark signal voltage		V_{DRK}	—	3	6	mV	(Note 7)
Dark signal non uniformity		DSNU	—	8	12	mV	(Note 8)
Dc power dissipation		P_D	—	700	1000	mW	—
Total transfer efficiency		TTE	92	98	—	%	—
Output impedance		Z_O	—	0.2	0.5	kΩ	—
Dc signal output voltage		V_{OS}	3.5	4.5	5.5	V	(Note 9)
Random noise		$N_{D\sigma}$	—	1.5	—	mV	(Note 10)

Note 2:Sensitivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

Note 3:PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

$$\text{PRNU (1)} = \frac{\Delta\chi}{\bar{\chi}} \times 100\ (\%)$$

$\bar{\chi}$: Average of total signal outputs
$\Delta\chi$: The maximum deviation from $\bar{\chi}$.

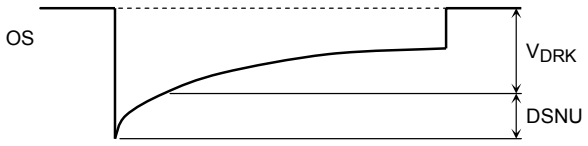
Note 4:PRNU (3) is defined as maximum voltage with next pixel, where measured 5% of SE (typ.).

Note 5:V_{SAT} is defined as minimum saturation output voltage of all effective pixels.

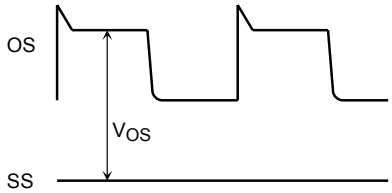
Note 6:Definition of SE: $\text{SE} = \frac{V_{SAT}}{RG}$

Note 7:V_{DRK} is defined as average dark signal voltage of all effective pixels.

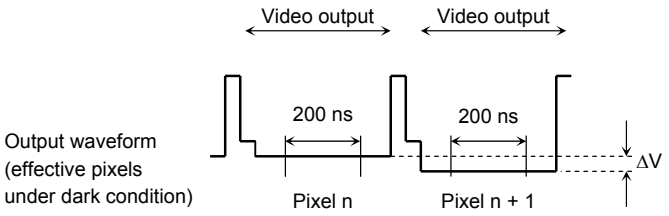
Note 8:DSNU is defined by the difference between average value (V_{DRK}) and the maximum value of the dark voltage.



Note 9:DC signal output voltage is defined as follows:



Note 10:Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark condition) calculated by the following procedure.



1) Two adjacent pixels (pixel n and n + 1) in one reading are fixed as measurement points.
2) Each of the output levels at video output periods averaged over 200 nanosecond period to get Vn and Vn + 1.
3) Vn + 1 is subtracted from Vn to get ΔV.
   ΔV = Vn − Vn + 1
4) The standard deviation of ΔV is calculated after procedure 2) and 3) are repeated 30 times (30 readings).

$$\Delta V = \frac{1}{30}\sum_{i=1}^{30}|\Delta Vi| \qquad \sigma = \sqrt{\frac{1}{30}\sum_{i=1}^{30}\left(|\Delta Vi| - \overline{\Delta V}\right)^2}$$

5) Procedure 2), 3) and 4) are repeated 10 times to get 10 sigma values.

$$\bar{\sigma} = \frac{1}{10}\sum_{j=1}^{10}\sigma j$$

6) $\bar{\sigma}$ value calculated using the above procedure is observed $\sqrt{2}$ times larger than that measured relative to the ground level. So we specify the random noise as follows.

$$\text{Random noise} = \frac{1}{\sqrt{2}}\bar{\sigma}$$

Operating Condition (Ta = 25°C)

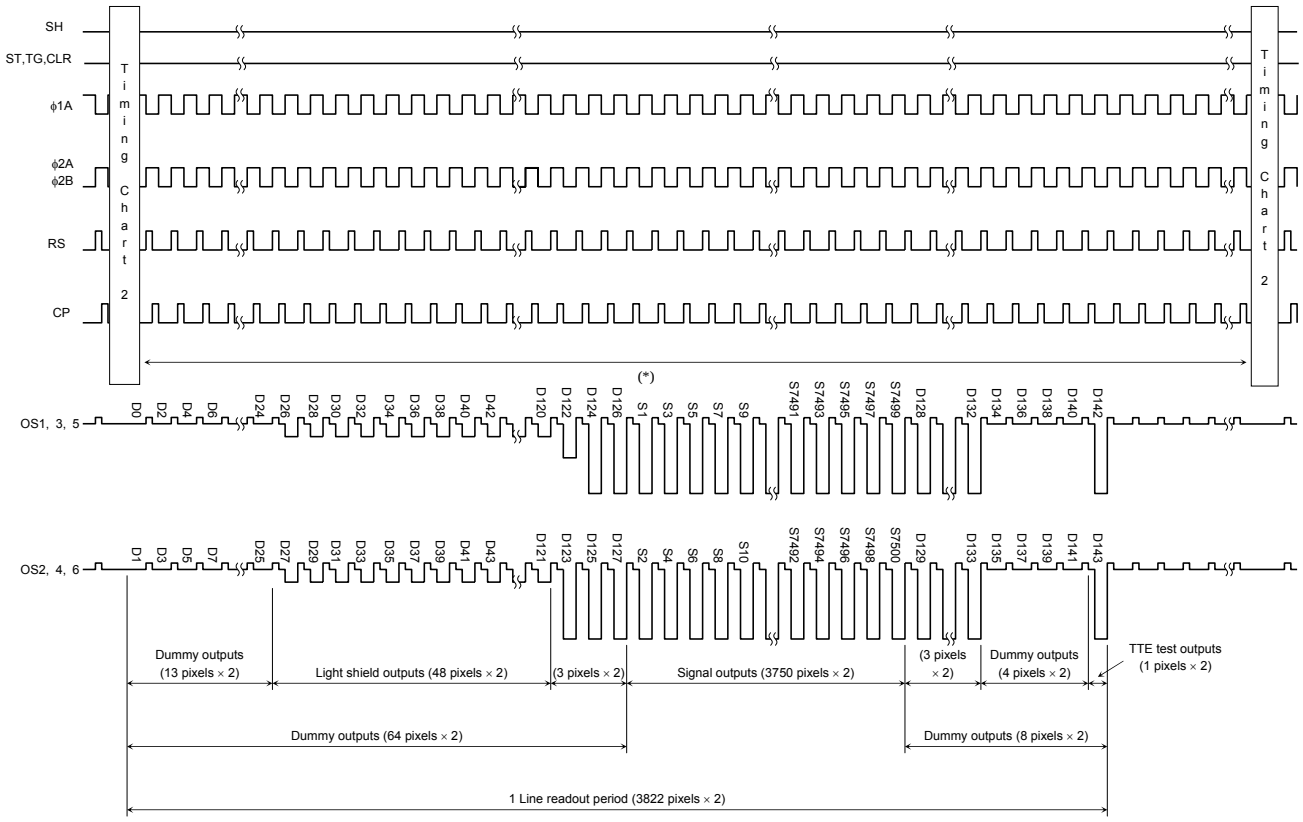
Characteristics		Symbol	Min	Typ.	Max	Unit
Clock pulse voltage	"H" level	$V_{\phi 1A}$	4.75	5	5.5	V
	"L" level	$V_{\phi 2A}$	0	—	0.25	
Final stage clock pulse voltage	"H" level	$V_{\phi 2B}$	4.75	5	5.5	V
	"L" level		0	—	0.25	
Shift pulse voltage (Note 11)	"H" level	V_{SH}	4.75	5	5.5	V
	"L" level		0	—	0.25	
Reset pulse voltage	"H" level	V_{RS}	4.75	5	5.5	V
	"L" level		0	—	0.25	
Clamp pulse voltage	"H" level	V_{CP}	4.75	5	5.5	V
	"L" level		0	—	0.25	
ST pulse voltage	"H" level	V_{ST}	4.75	5	5.5	V
	"L" level		0	—	0.25	
TG pulse voltage	"H" level	V_{TG}	4.75	5	5.5	V
	"L" level		0	—	0.25	
CLR pulse voltage	"H" level	V_{CLR}	4.75	5	5.5	V
	"L" level		0	—	0.25	
Power supply voltage		V_{OD}	9.5	10	10.5	V

Clock Characteristics (Ta = 25°C)

Characteristics	Symbol	Min	Typ.	Max	Unit
Clock pulse frequency	f_{ϕ}	—	1	30	MHz
Reset pulse frequency	f_{RS}	—	1	30	MHz
Clamp pulse frequency	f_{CP}	—	1	30	MHz
Clock capacitance (Note 12)	$C_{\phi 1A}$	—	240	—	pF
	$C_{\phi 2A}$	—	165	—	pF
Final stage clock capacitance	$C_{\phi B}$	—	20	—	pF
Shift gate capacitance	$C_{SH1,2}$	—	40	—	pF
	C_{SH3}	—	70	—	pF
Reset gate capacitance	C_{RS}	—	20	—	pF
Clamp gate capacitance	C_{CP}	—	20	—	pF
ST gate capacitance	C_{ST}	—	40	—	pF
TG gate capacitance	C_{TG}	—	40	—	pF
CLR gate capacitance	C_{CLR}	—	40	—	pF

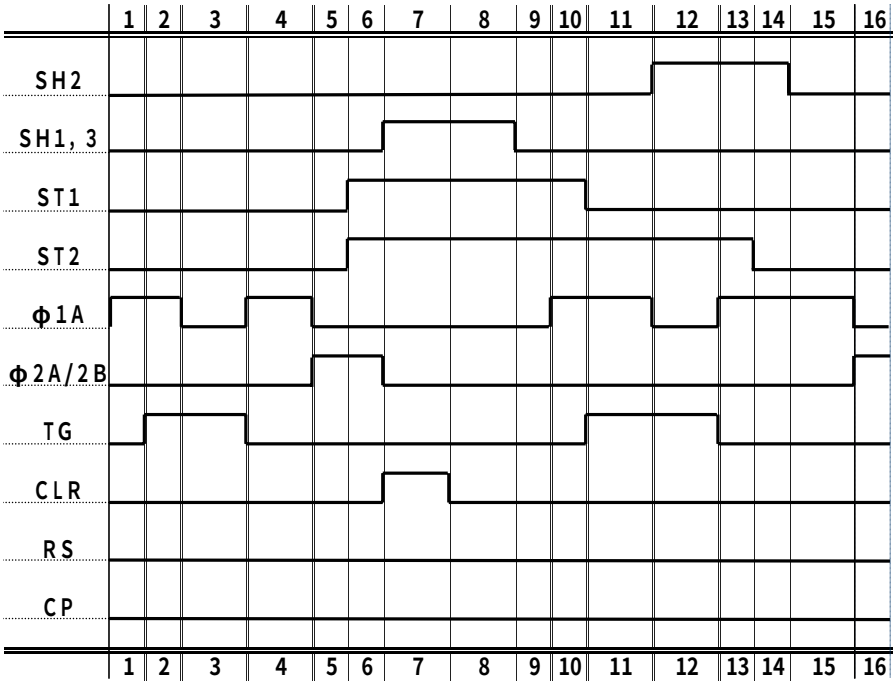
Note 12: V_{OD} = 10 V

Timing Chart 1



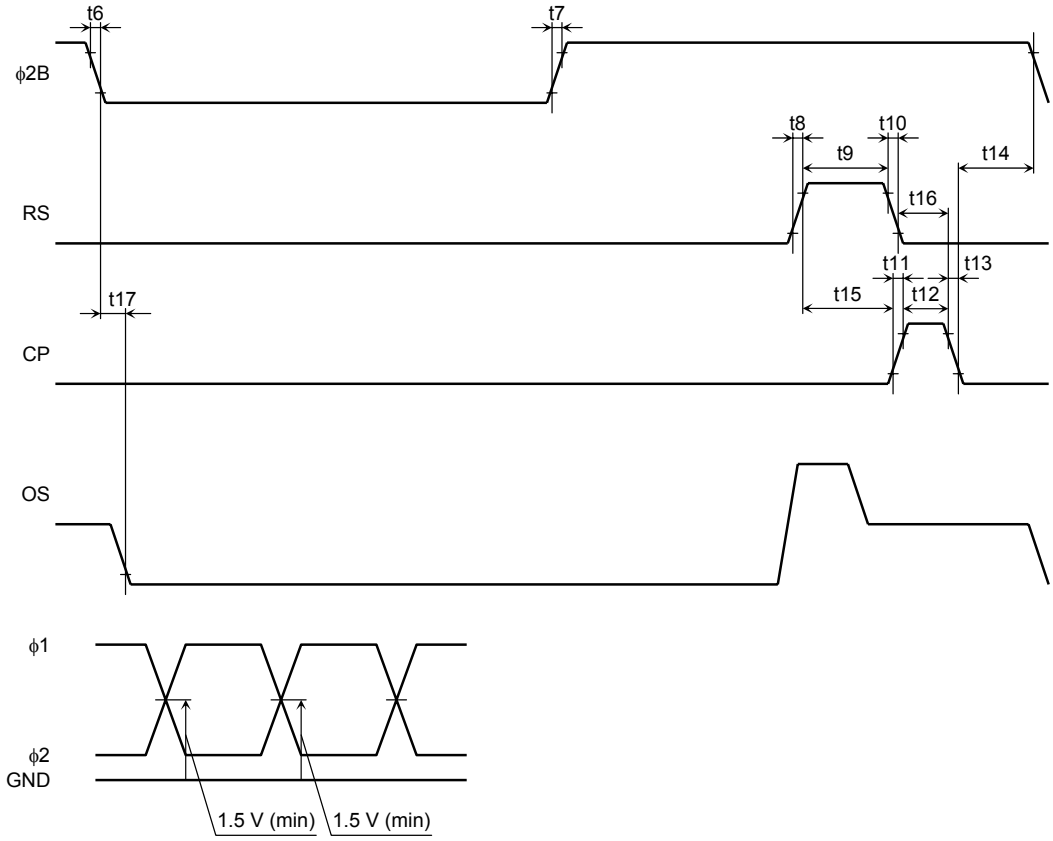
*: Hold the ST, TG, CLR and SH pins at low during this period.

Timing Chart 2



Note13 : Each RS and CP pins put to Low level during the period of the above mentioned address 1 - 15.

Timing Requirements1



Characteristics	Symbol	Min	Typ. (Note 14)	Max	Unit
ϕ1, ϕ2 Pulse rise time, fall time	t6, t7	0	50	—	ns
RS pulse rise time, fall time	t8, t10	0	20	—	ns
RS pulse width	t9	8	100	—	ns
CP pulse rise time, fall time	t11, t13	0	20	—	ns
CP pulse width	t12	8	100	—	ns
Pulse timing of ϕ2B and CP	t14	0	40	—	ns
Pulse timing of RS and CP	t15	0	100	—	ns
	t16	8	100	—	ns
Video data delay time (Note 15)	t17	—	10	—	ns

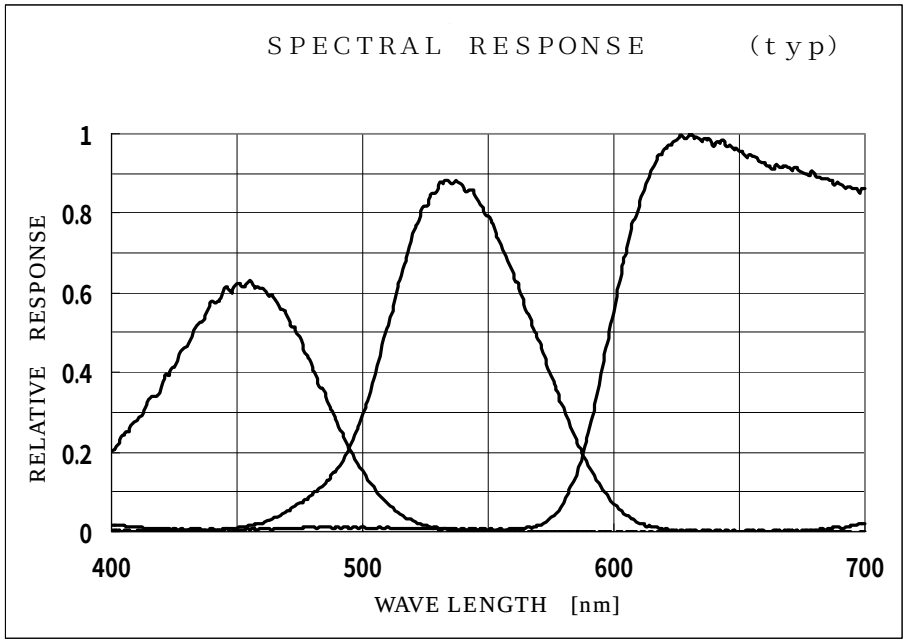
Note14:Measured with fRS=1MHz

Note15:Load resistance is 100kΩ

Timing Requirements 2

Timing Address	Min	Unit
1	250	ns
2	250	
3	500	
4	500	
5	250	
6	250	
7	500	
8	500	
9	250	
10	250	
11	500	
12	500	
13	250	
14	250	
15	500	
Vertical Transfer Time	5.5	μs

Spectral Response



Caution

1. Electrostatic Breakdown

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.
Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N2. Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

Prevent the generation of static electricity due to friction by making the work with bare hands or by putting on cotton gloves and non-charging working clothes.
Discharge the static electricity by providing earth plate or earth wire on the floor, door or stand of the work room.
Ground the tools such as soldering iron, radio cutting pliers of or pincer.
It is not necessarily required to execute all precaution items for static electricity.
It is all right to mitigate the precautions by confirming that the trouble rate within the prescribed range.

2. Window Glass

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.
Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N2. Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

3. Incident Light

CCD sensor is sensitive to infrared light. Note that infrared light component degrades resolution and PRNU of CCD sensor.

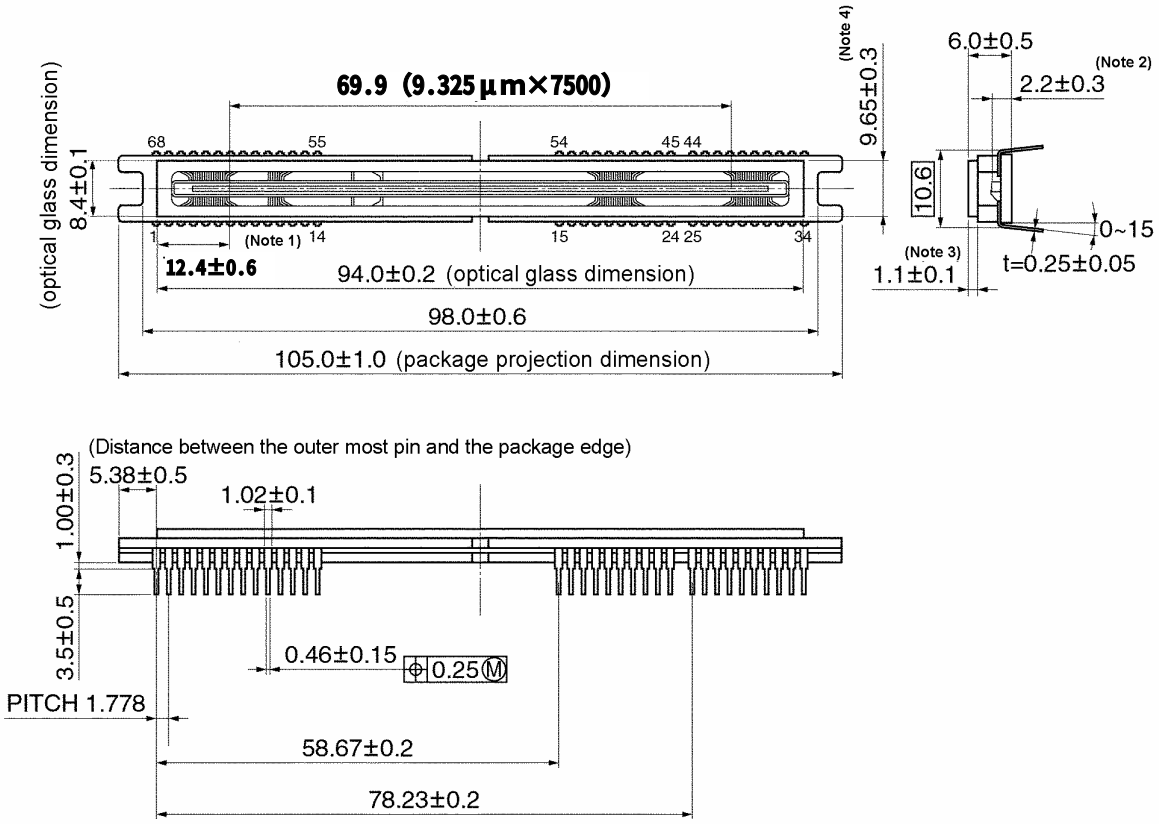
4. Mounting on a PCB

This package is sensitive to mechanical stress.
Toshiba recommends using IC inserters for mounting, instead of using lead forming equipment.

5. Soldering

Soldering by the solder flow method cannot be guaranteed because this method may have deleterious effects on prevention of window glass soiling and heat resistance.
Using a soldering iron, complete soldering within ten seconds for lead temperatures of up to 260°C, or within three seconds for lead temperatures of up to 350°C.

Package Dimensions



Note 1: Distance between the center of the first pin and the first pixel (S1)
Note 2: Distance between the of the chip and bottom of the package.
Note 3: Glass thickness (n = 1.5)
Note 4: Dimensional tolerance is ±0.3 mm for the 10-mm range from each ceramic edge, ±0.4 mm for the 10-mm to 27-mm range and ±0.5 mm for the inner range.

Weight: 16.0 g (typ.)

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