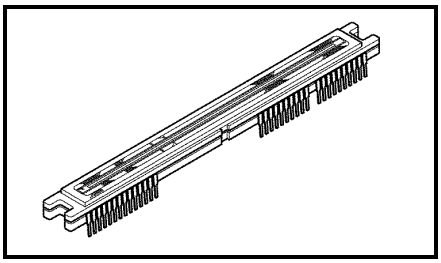
TOSHIBA CCD Linear Image Sensor
CCD (Charge Coupled Device)

TCD2705DG

The TCD2705DG is a high sensitive and low dark current 7300 pixels × 3 line CCD color image sensor.
The sensor is designed for color scanner.
The device contains a row of 7300 pixels × 3 line photodiodes which provide a 24 lines/mm across a A3 size paper. The device is operated by 5-V pulse, and 10-V power supply.

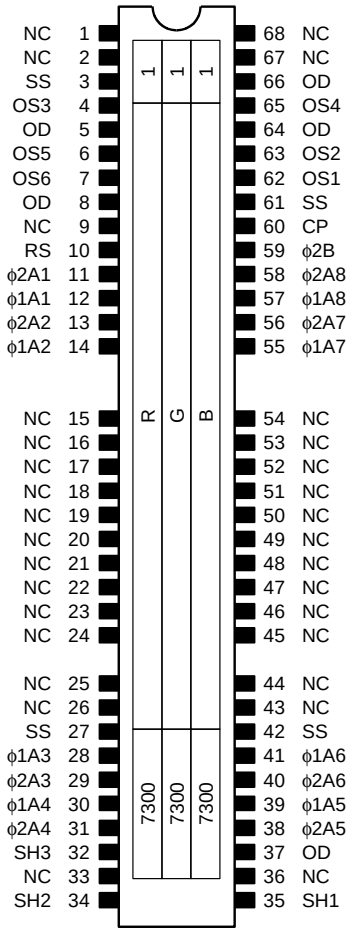


Weight: 16.0 g (typ.)

Features

- Number of image sensing pixels
  : 21900 pixels (7300 pixels × 3 line)
- Image sensing pixels size
  : 10 µm by 10 µm on 10 µm center
- Photo sensing region: High sensitive pn photodiode
- Clock: 2-phase (5 V)
- Distance between photodiode array
  : Pixel R to pixel G: 40 µm (4 lines)
  Pixel G to pixel B: 40 µm (4 lines)
- Internal circuit: Clamp circuit
- Package: 68-pin CERDIP
- Color filter: Red, Green, Blue

Pin Connections (top view)



Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Clock pulse voltage	$V_{\phi}A$	−0.3 to 8	V
Last stage clock pulse voltage	$V_{\phi}B$		
Shift pulse voltage	VSH		
Reset pulse voltage	VRS		
Clamp pulse voltage	VCP		
Power supply voltage	VOD	−0.3 to 15	V
Operating temperature	Topr	0 to 60	°C
Storage temperature	Tstg	−25 to 85	°C

Note 1: All voltages are with respect to SS pins (ground).

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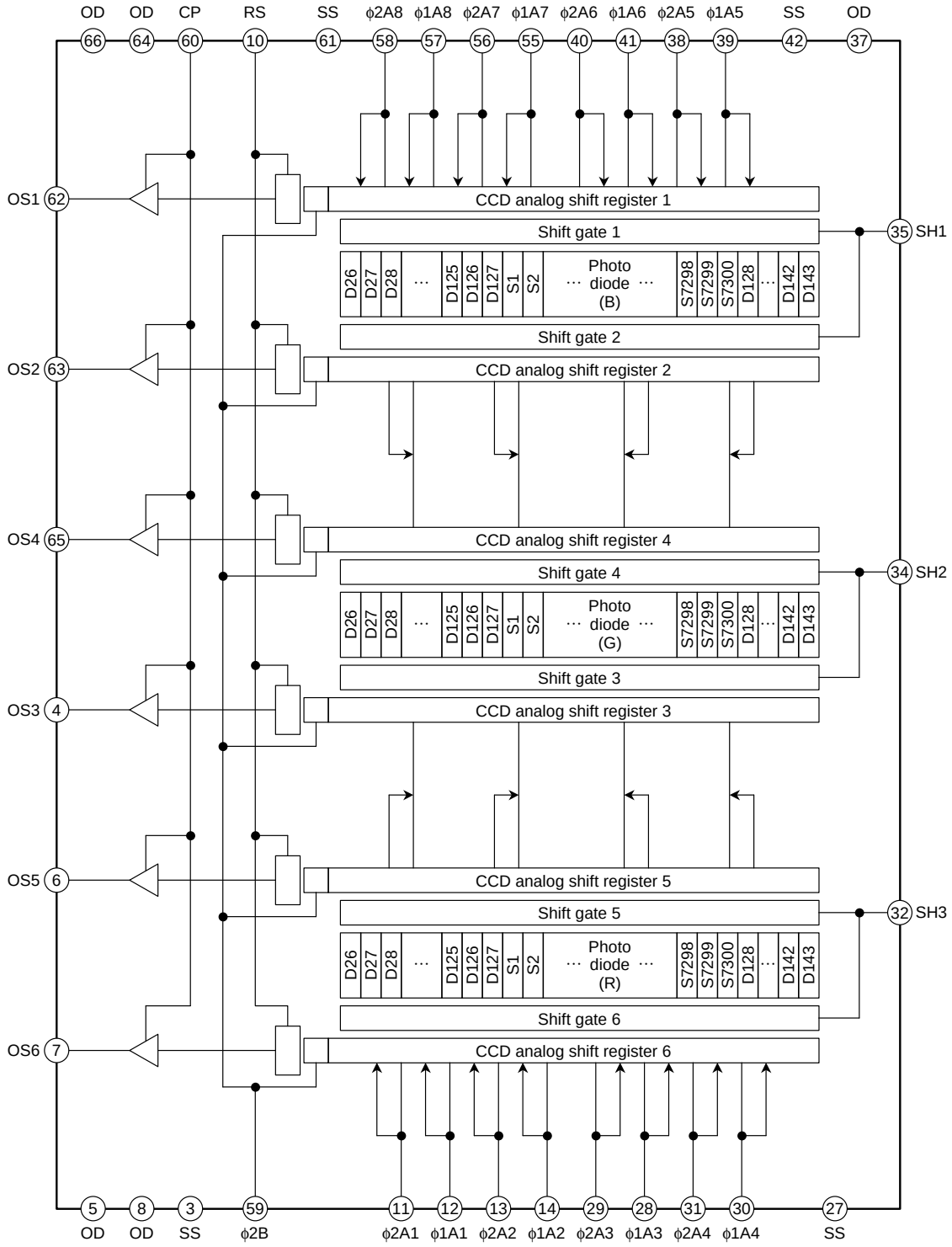
Circuit Diagram



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Pin Names

Pin No.	Symbol	Name	Pin No.	Symbol	Name
1	NC	Non connect	35	SH1	Shift gate 1
2	NC	Non connect	36	NC	Non connect
3	SS	Ground (digital)	37	OD	Power (digital)
4	OS3	Signal output 3 (green)	38	ϕ2A5	Clock 5 (phase 2)
5	OD	Power (analog)	39	ϕ1A5	Clock 5 (phase 1)
6	OS5	Signal output 5 (red)	40	ϕ2A6	Clock 6 (phase 2)
7	OS6	Signal output 6 (red)	41	ϕ1A6	Clock 6 (phase 1)
8	OD	Power (analog)	42	SS	Ground (digital)
9	NC	Non connect	43	NC	Non connect
10	RS	Reset gate	44	NC	Non connect
11	ϕ2A1	Clock 1 (phase 2)	45	NC	Non connect
12	ϕ1A1	Clock 1 (phase 1)	46	NC	Non connect
13	ϕ2A2	Clock 2 (phase 2)	47	NC	Non connect
14	ϕ1A2	Clock 2 (phase 1)	48	NC	Non connect
15	NC	Non connect	49	NC	Non connect
16	NC	Non connect	50	NC	Non connect
17	NC	Non connect	51	NC	Non connect
18	NC	Non connect	52	NC	Non connect
19	NC	Non connect	53	NC	Non connect
20	NC	Non connect	54	NC	Non connect
21	NC	Non connect	55	ϕ1A7	Clock 7 (phase 1)
22	NC	Non connect	56	ϕ2A7	Clock 7 (phase 2)
23	NC	Non connect	57	ϕ1A8	Clock 8 (phase 1)
24	NC	Non connect	58	ϕ2A8	Clock 8 (phase 2)
25	NC	Non connect	59	ϕ2B	Final stage clock
26	NC	Non connect	60	CP	Clamp gate
27	SS	Ground (digital)	61	SS	Ground (analog)
28	ϕ1A3	Clock 3 (phase 1)	62	OS1	Signal output 1 (blue)
29	ϕ2A3	Clock 3 (phase 2)	63	OS2	Signal output 2 (blue)
30	ϕ1A4	Clock 4 (phase 1)	64	OD	Power (analog)
31	ϕ2A4	Clock 4 (phase 2)	65	OS4	Signal output 4 (green)
32	SH3	Shift gate 3	66	OD	Power (digital)
33	NC	Non connect	67	NC	Non connect
34	SH2	Shift gate 2	68	NC	Non connect

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Optical/Electrical Characteristics (bit clamp)

(Ta = 25°C, V_{OD} = 10 V, V_f = V_{RS} = V_{SH} = V_{CP} = 5 V (pulse), f_f = 1 MHz, load resistance = 100 kΩ, t_{INT} (integration time) = 10 ms, light source = A light source + CM500S filter (t = 1.0 mm))

Characteristics		Symbol	Min	Typ.	Max	Unit	Note
Sensitivity	Red	R (R)	2.5	3.6	4.7	V/lx•s	(Note 2)
	Green	R (G)	3.2	4.7	6.2		
	Blue	R (B)	1.8	2.7	3.6		
Photo response non uniformity		PRNU (1)	—	10	20	%	(Note 3)
		PRNU (3)	—	3	12	mV	(Note 4)
Saturation output voltage		V_{SAT}	1.2	1.5	—	V	(Note 5)
Saturation exposure		SE	0.2	0.3	—	lx•s	(Note 6)
Dark signal voltage		V_{DRK}	—	3	6	mV	(Note 7)
Dark signal non uniformity		DSNU	—	8	12	mV	(Note 8)
Dc power dissipation		P_D	—	680	1000	mW	—
Total transfer efficiency		TTE	95	98	—	%	—
Output impedance		Z_O	—	0.2	0.5	kΩ	—
Dc signal output voltage		V_{OS}	3.0	4.5	6.0	V	(Note 9)
Random noise		$N_{D\sigma}$	—	0.6	—	mV	(Note 10)

Note 2: Sensitivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

Note 3: PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

$$\text{PRNU (1)} = \frac{\Delta\chi}{\bar{\chi}} \times 100 \ (\%)$$

$\bar{\chi}$: Average of total signal outputs
$\Delta\chi$: The maximum deviation from $\bar{\chi}$.

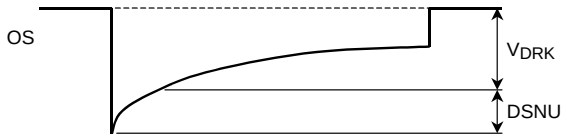
Note 4: PRNU (3) is defined as maximum voltage with next pixel, where measured 5% of SE (typ.).

Note 5: V_{SAT} is defined as minimum saturation output voltage of all effective pixels.

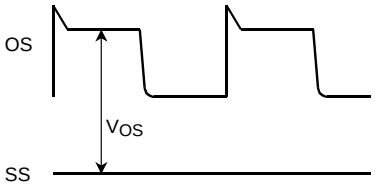
Note 6: Definition of SE: $\text{SE} = \frac{V_{SAT}}{\text{R (G)}}$

Note 7: V_{DRK} is defined as average dark signal voltage of all effective pixels.

Note 8: DSNU is defined by the difference between average value (V_{DRK}) and the maximum value of the dark voltage.



Note 9: DC signal output voltage is defined as follows:



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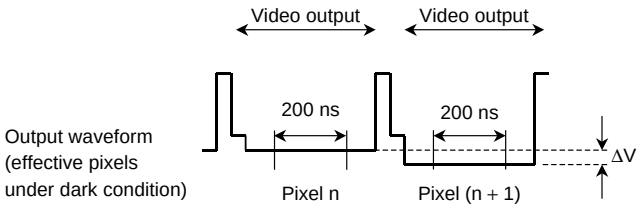
Note 10: Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark condition) calculated by the following procedure.



1) Two adjacent pixels (pixel n and (n + 1)) in one reading are fixed as measurement points.
2) Each of the output levels at video output periods averaged over 200 nanosecond period to get Vn and V (n + 1).
3) V (n + 1) is subtracted from Vn to get ΔV.
   $\Delta V = Vn - V(n+1)$
4) The standard deviation of ΔV is calculated after procedure 2) and 3) are repeated 30 times (30 readings).
   $\overline{\Delta V} = \frac{1}{30}\sum_{i=1}^{30}|\Delta Vi|$ $\qquad$ $\acute{o} = \sqrt{\frac{1}{30}\sum_{i=1}^{30}(|\ddot{A}Vi| - \overline{\ddot{A}V})^2}$
5) Procedure 2), 3) and 4) are repeated 10 times to get 10 sigma values.
   $\bar{\sigma} = \frac{1}{10}\sum_{j=1}^{10}\sigma j$
6) $\bar{\sigma}$ value calculated using the above procedure is observed $\sqrt{2}$ times larger than that measured relative to the ground level. So we specify the random noise as follows.
   Random noise = $\frac{1}{\sqrt{2}}\bar{\sigma}$

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Operating Condition (Ta = 25°C)

Characteristics		Symbol	Min	Typ.	Max	Unit
Clock pulse voltage	"H" Level	$V_{\phi 1A}$, $V_{\phi 2A}$	4.75	5	5.5	V
	"L" Level		0	—	0.25	
Final stage clock pulse voltage	"H" Level	$V_{\phi 2B}$	4.75	5	5.5	V
	"L" Level		0	—	0.25	
Shift pulse voltage	"H" Level	V_{SH}	4.75	5	5.5	V
	"L" Level		0	—	0.25	
Reset pulse voltage	"H" Level	V_{RS}	4.75	5	5.5	V
	"L" Level		0	—	0.25	
Clamp pulse voltage	"H" Level	V_{CP}	4.75	5	5.5	V
	"L" Level		0	—	0.25	
Power supply voltage		V_{OD}	9.5	10.0	11.0	V

Clock Characteristics (Ta = 25°C)

Characteristics	Symbol	Min	Typ.	Max	Unit
Clock pulse frequency	f_{ϕ}	—	1	30	MHz
Reset pulse frequency	f_{RS}	—	1	30	MHz
Clamp pulse frequency	f_{CP}	—	1	30	MHz
Clock capacitance (Note 11)	$C_{\phi A}$	—	117	—	pF
Final stage clock capacitance	$C_{\phi B}$	—	7	—	pF
Shift gate capacitance	C_{SH1}	—	6	—	pF
	C_{SH2}	—	6	—	
	C_{SH3}	—	53	—	
Reset gate capacitance	C_{RS}	—	9	—	pF
Clamp gate capacitance	C_{CP}	—	9	—	pF

Note 11: V_{OD} = 10 V

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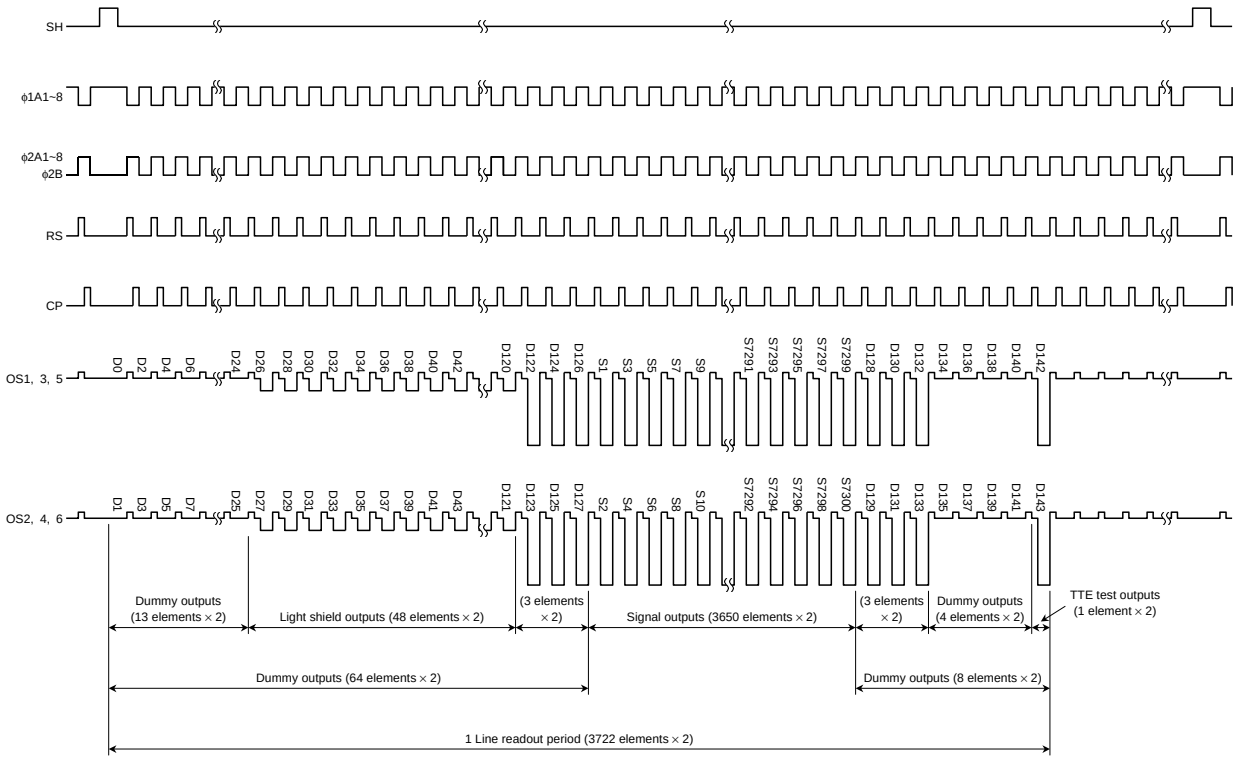
Timing Chart



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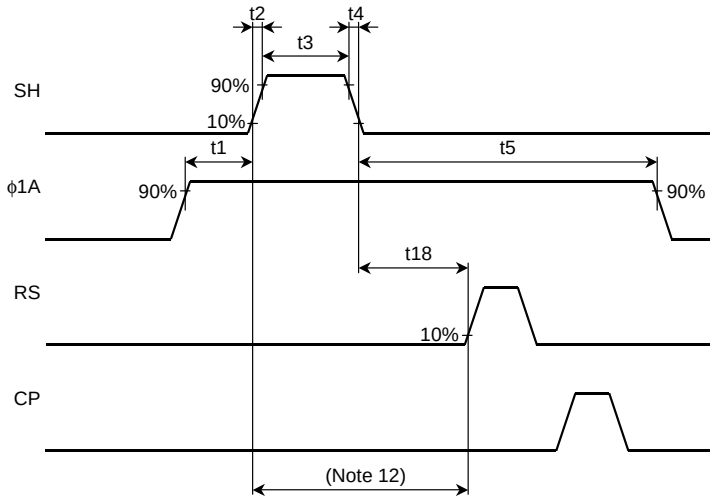
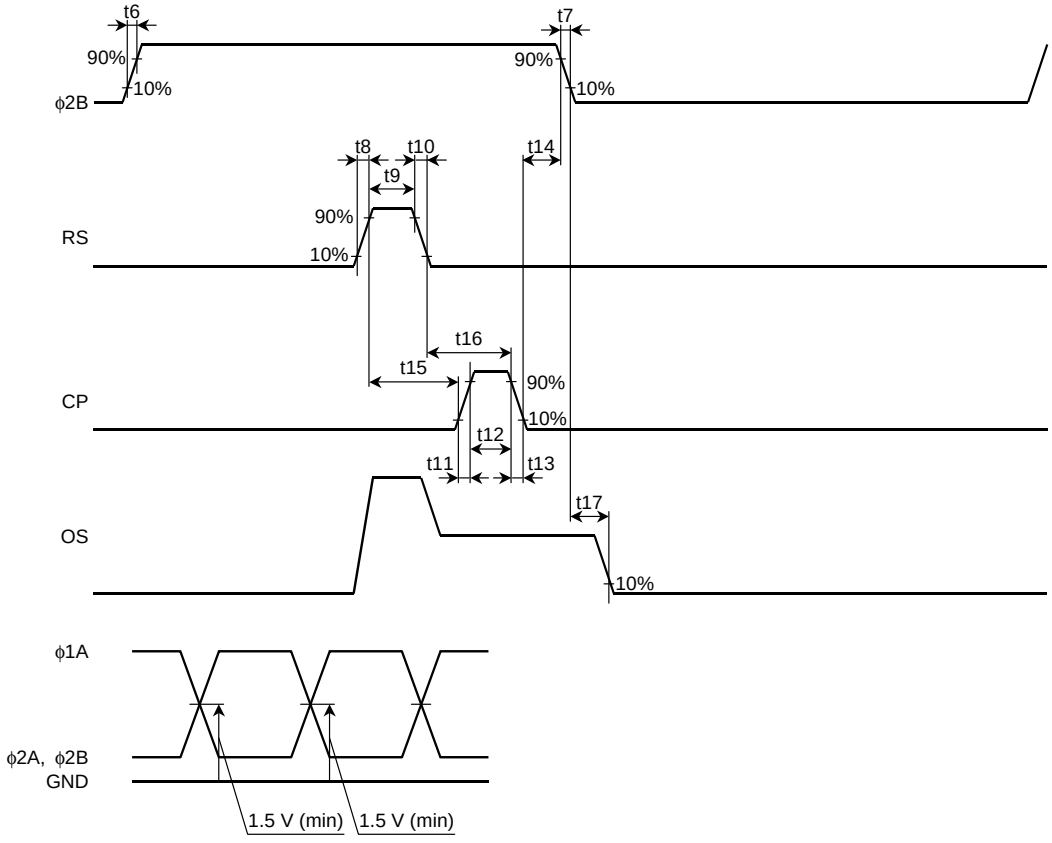
Timing Requirements



Note 12: Hold the RS and CP pins at low during this period.



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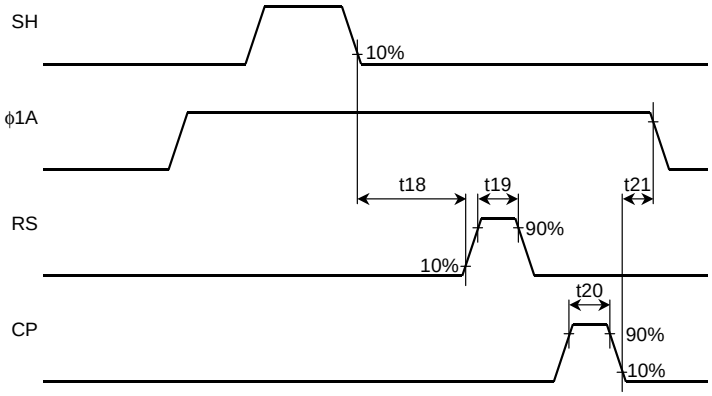
Timing Requirements (line clamp)



Characteristics	Symbol	Min	Typ. (Note 13)	Max	Unit
Pulse timing of SH and ϕ1A	t1	60	1000	—	ns
	t5	500	1000	—	ns
SH pulse rise time, fall time	t2, t4	0	50	—	ns
SH pulse width	t3	1000	2000	—	ns
ϕ1, ϕ2 Pulse rise time, fall time	t6, t7	0	50	—	ns
RS pulse rise time, fall time	t8, t10	0	20	—	ns
RS pulse width	t9	8	100	—	ns
CP pulse rise time, fall time	t11, t13	0	20	—	ns
CP pulse width	t12	8	200	—	ns
Pulse timing of ϕ2B and CP	t14	0	40	—	ns
Pulse timing of RS and CP	t15	0	0	—	ns
	t16	8	100	—	ns
Video data delay time (Note 14)	t17	—	8	—	ns
SH, RS pulse timing	t18	500	—	—	ns
RS pulse width (line clamp)	t19	10	—	—	ns
CP pulse width (line clamp)	t20	10	—	—	ns
CP, ϕ1A pulse timing (line clamp)	t21	5	—	—	ns

Note 13: Measured with f_{RS} = 1 MHz.

Note 14: Load resistance is 100 kΩ.

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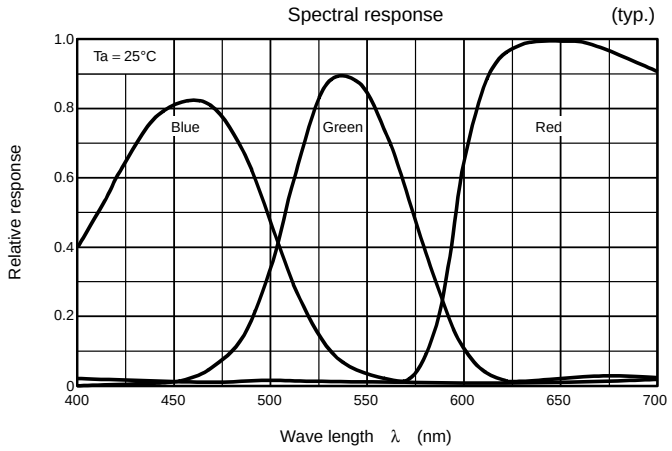
Typical Spectral Response



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Caution

1. Electrostatic Breakdown

The dust and stain on the glass window of the package degrade optical performance of CCD sensor. Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N2. Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

(ア) Prevent the generation of static electricity due to friction by making the work with bare hands or by putting on cotton gloves and non-charging working clothes.
(イ) Discharge the static electricity by providing earth plate or earth wire on the floor, door or stand of the work room.
(ウ) Ground the tools such as soldering iron, radio cutting pliers of or pincer.
It is not necessarily required to execute all precaution items for static electricity.
It is all right to mitigate the precautions by confirming that the trouble rate within the prescribed range.

2. Window Glass

The dust and stain on the glass window of the package degrade optical performance of CCD sensor. Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N2. Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

3. Incident Light

CCD sensor is sensitive to infrared light. Note that infrared light component degrades resolution and PRNU of CCD sensor.

4. Mounting on a PCB

This package is sensitive to mechanical stress.
Toshiba recommends using IC inserters for mounting, instead of using lead forming equipment.

5. Soldering

Soldering by the solder flow method cannot be guaranteed because this method may have deleterious effects on prevention of window glass soiling and heat resistance.
Using a soldering iron, complete soldering within ten seconds for lead temperatures of up to 260°C, or within three seconds for lead temperatures of up to 350°C.

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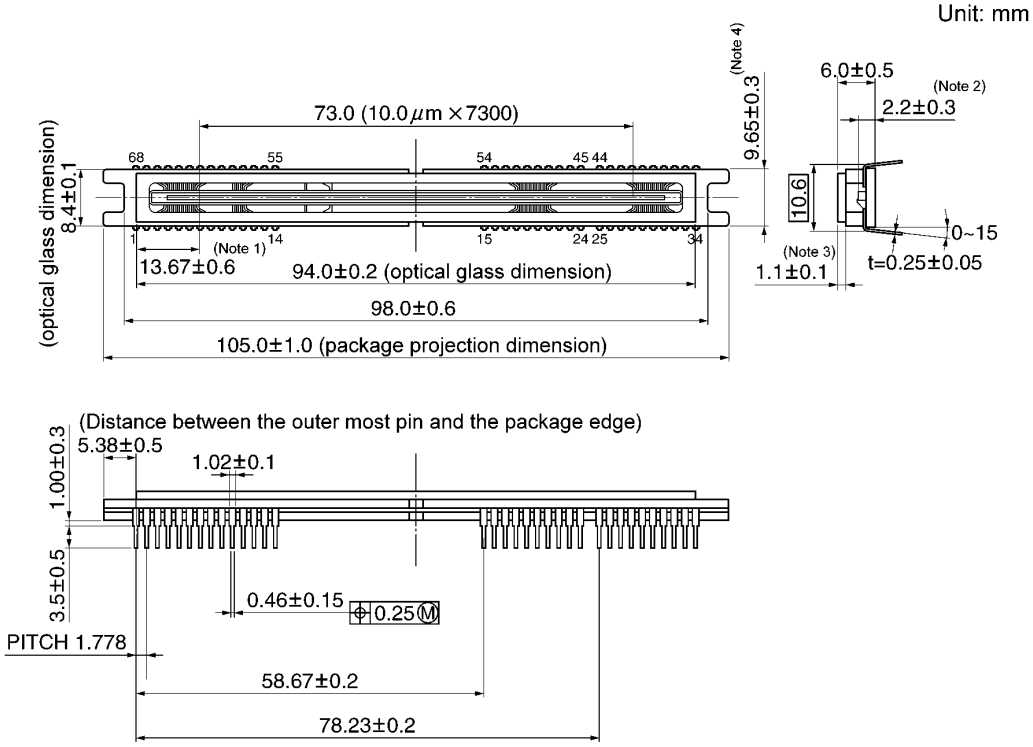
Package Dimensions

Unit: mm



Note 1: Distance between the center of the first pin and the first pixel (S1)
Note 2: Distance between the of the chip and bottom of the package.
Note 3: Glass thickness (n = 1.5)
Note 4: Dimensional tolerance is ±0.3 mm for the 10-mm range from each ceramic edge, ±0.4 mm for the 10-mm to 27-mm range and ±0.5 mm for the inner range.

Weight: 16.0 g (typ.)

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About solderability, following conditions were confirmed

- Solderability

  (1) Use of Sn-63Pb solder Bath
  - solder bath temperature = 230°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder Bath
  - solder bath temperature = 245°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

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