1/3-Inch Wide-VGA CMOS Digital Image Sensor

MT9V022

For the latest data sheet revision, refer to Aptina's Web site: www.aptina.com

Features

- Aptina® DigitalClarity® CMOS imaging technology
- Array format: Wide-VGA, active 752H x 480V (360,960 pixels)
- Global shutter photodiode pixels; simultaneous integration and readout
- Monochrome or color: Near_IR enhanced performance for use with non-visible NIR illumination
- Readout modes: progressive or interlaced
- Shutter efficiency: >99%
- Simple two-wire serial interface
- Register Lock capability
- Window Size: User programmable to any smaller format (QVGA, CIF, QCIF, etc.). Data rate can be maintained independent of window size
- Binning: 2 x 2 and 4 x 4 of the full resolution
- ADC: On-chip, 10-bit column-parallel (option to operate in 12-bit to 10-bit companding mode)
- Automatic Controls: Auto exposure control (AEC) and auto gain control (AGC); variable regional and variable weight AEC/AGC
- Support for four unique serial control register IDs to control multiple imagers on the same bus
- Data output formats:
  - Single sensor mode: 10-bit parallel/stand-alone 8-bit or 10-bit serial LVDS
  - Stereo sensor mode: Interspersed 8-bit serial LVDS

Applications

- Automotive
- Unattended surveillance
- Stereo vision
- Security
- Smart vision
- Automation
- Video as input
- Machine vision

Table 1: Key Performance Parameters

Parameter	Value
Optical format	1/3-inch
Active imager size	4.51mm(H) x 2.88mm(V) 5.35mm diagonal
Active pixels	752H x 480V
Pixel size	6.0µm x 6.0µm
Color filter array	Monochrome or color RGB Bayer pattern
Shutter type	Global shutter—TrueSNAP™
Maximum data rate/ master clock	26.6 MPS/26.6 MHz
Full resolution	752 x 480
Frame rate	60 fps (at full resolution)
ADC resolution	10-bit column-parallel
Responsivity	4.8 V/lux-sec (550nm)
Dynamic range	>55dB linear; >80dB—100dB in HiDy mode
Supply voltage	3.3V ±0.3V (all supplies)
Power consumption	<320mW at maximum data rate; 100?W standby power
Operating temperature	-40°C to +85°C
Packaging	52-Ball IBGA, automotive-qualified; wafer or die

Ordering Information

Table 2: Available Part Numbers

Part Number	Description
MT9V022I77ATM	52-Ball IBGA (monochrome)
MT9V022IA7ATM	52-Ball IBGA (lead-free monochrome)
MT9V022I77ATC	52-Ball IBGA (color)
MT9V022IA7ATC	52-Ball IBGA (lead-free color)

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General Description

The Aptina® MT9V022 is a 1/3-inch wide-VGA format CMOS active-pixel digital image sensor with global shutter and high dynamic range (HDR) operation. The sensor has specifically been designed to support the demanding interior and exterior automotive imaging needs, which makes this part ideal for a wide variety of imaging applications in real-world environments.

This wide-VGA CMOS image sensor features DigitalClarity—Aptina's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The active imaging pixel array is 752H x 480V. It incorporates sophisticated camera functions on-chip—such as binning 2 x 2 and 4 x 4, to improve sensitivity when operating in smaller resolutions—as well as windowing, column and row mirroring. It is programmable through a simple two-wire serial interface.

The MT9V022 can be operated in its default mode or be programmed for frame size, exposure, gain setting, and other parameters. The default mode outputs a wide-VGA-size image at 60 frames per second (fps).

An on-chip analog-to-digital converter (ADC) provides 10 bits per pixel. A 12-bit resolution companded for 10 bits for small signals can be alternatively enabled, allowing more accurate digitization for darker areas in the image.

In addition to a traditional, parallel logic output the MT9V022 also features a serial low-voltage differential signaling (LVDS) output. The sensor can be operated in a stereo-camera, and the sensor, designated as a stereo-master, is able to merge the data from itself and the stereo-slave sensor into one serial LVDS stream.

The sensor is designed to operate in a wide temperature range (–40°C to +85°C).

Figure 1: Block Diagram

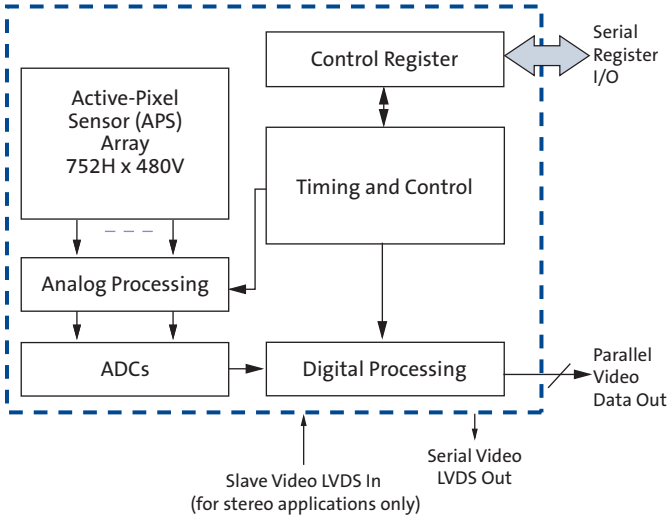
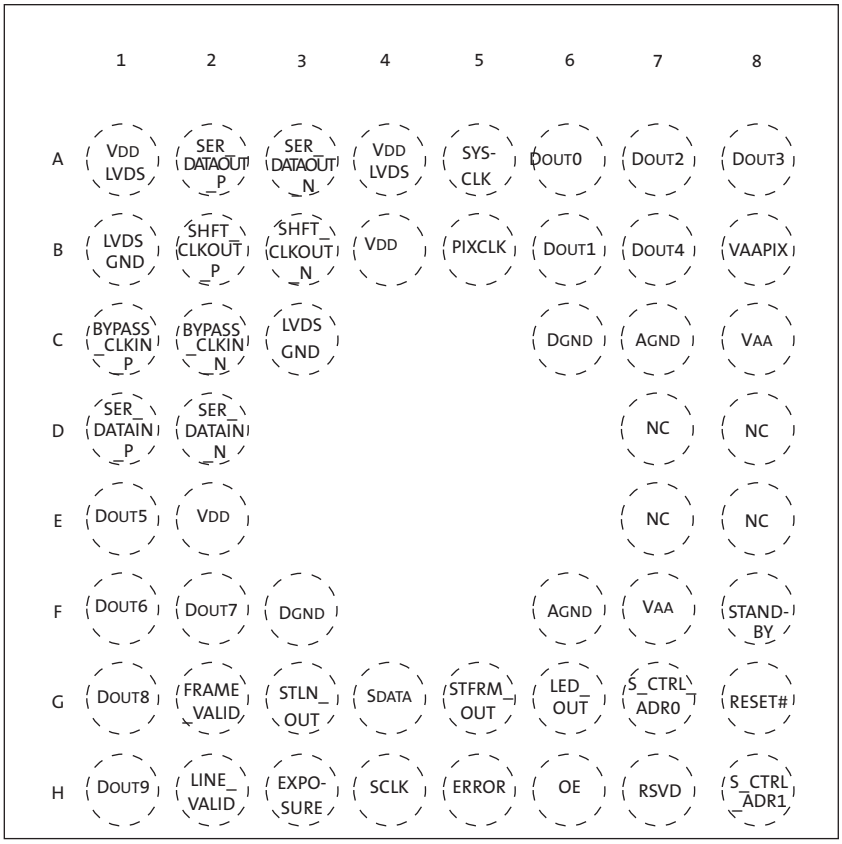


Figure 2: 52-Ball IBGA Package



Top View
(Ball Down)

Ball Descriptions

Table 3: Ball Descriptions
Only pins DOUT0 through DOUT9 may be tri-stated.

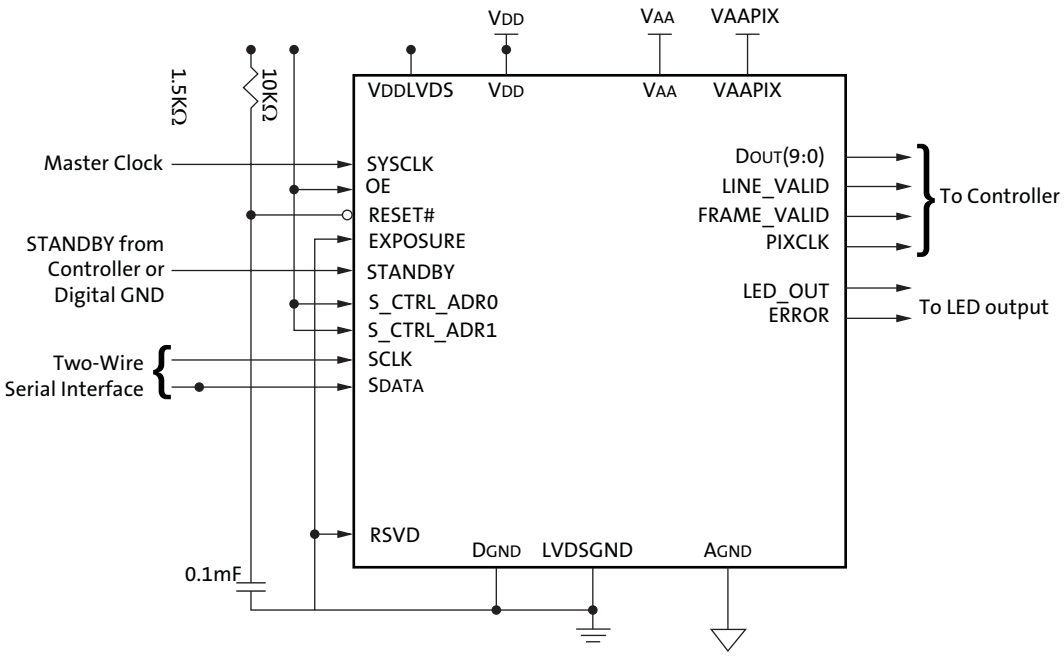
52-Ball IBGA Numbers	Symbol	Type	Description	Note
H7	RSVD	Input	Connect to DGND.	1
D2	SER_DATAIN_N	Input	Serial data in for stereoscopy (differential negative). Tie to 1KΩ pull-up (to 3.3V) in non-stereoscopy mode.	
D1	SER_DATAIN_P	Input	Serial data in for stereoscopy (differential positive). Tie to DGND in non-stereoscopy mode.	
C2	BYPASS_CLKIN_N	Input	Input bypass shift-CLK (differential negative). Tie to 1KΩ pull-up (to 3.3V) in non-stereoscopy mode.	
C1	BYPASS_CLKIN_P	Input	Input bypass shift-CLK (differential positive). Tie to DGND in non-stereoscopy mode.	
H3	EXPOSURE	Input	Rising edge starts exposure in slave mode.	
H4	SCLK	Input	Two-wire serial interface clock. Connect to VDD with 1.5K resistor even when no other two-wire serial interface peripheral is attached.	
H6	OE	Input	DOUT enable pad, active HIGH.	2
G7	S_CTRL_ADR0	Input	Two-wire serial interface slave address bit 3.	
H8	S_CTRL_ADR1	Input	Two-wire serial interface slave address bit 5.	
G8	RESET#	Input	Asynchronous reset. All registers assume defaults.	
F8	STANDBY	Input	Shut down sensor operation for power saving.	
A5	SYSCLK	Input	Master clock (26.6 MHz).	
G4	SDATA	I/O	Two-wire serial interface data. Connect to VDD with 1.5K resistor even when no other two-wire serial interface peripheral is attached.	
G3	STLN_OUT	I/O	Output in master mode—start line sync to drive slave chip in-phase; input in slave mode.	
G5	STFRM_OUT	I/O	Output in master mode—start frame sync to drive a slave chip in-phase; input in slave mode.	
H2	LINE_VALID	Output	Asserted when DOUT data is valid.	
G2	FRAME_VALID	Output	Asserted when DOUT data is valid.	
E1	DOUT5	Output	Parallel pixel data output 5.	
F1	DOUT6	Output	Parallel pixel data output 6.	
F2	DOUT7	Output	Parallel pixel data output 7.	
G1	DOUT8	Output	Parallel pixel data output 8	
H1	DOUT9	Output	Parallel pixel data output 9.	
H5	ERROR	Output	Error detected. Directly connected to STEREO ERROR FLAG.	
G6	LED_OUT	Output	LED strobe output.	
B7	DOUT4	Output	Parallel pixel data output 4.	
A8	DOUT3	Output	Parallel pixel data output 3.	
A7	DOUT2	Output	Parallel pixel data output 2.	
B6	DOUT1	Output	Parallel pixel data output 1.	
A6	DOUT0	Output	Parallel pixel data output 0.	
B5	PIXCLK	Output	Pixel clock out. DOUT is valid on rising edge of this clock.	
B3	SHFT_CLKOUT_N	Output	Output shift CLK (differential negative).	
B2	SHFT_CLKOUT_P	Output	Output shift CLK (differential positive).	
A3	SER_DATAOUT_N	Output	Serial data out (differential negative).	

Table 3: Ball Descriptions (continued)
Only pins DOUT0 through DOUT9 may be tri-stated.

52-Ball IBGA Numbers	Symbol	Type	Description	Note
A2	SER_DATAOUT_P	Output	Serial data out (differential positive).	
B4, E2	VDD	Supply	Digital power 3.3V.	
C8, F7	VAA	Supply	Analog power 3.3V.	
B8	VAAPIX	Supply	Pixel power 3.3V.	
A1, A4	VDDLVDS	Supply	Dedicated power for LVDS pads.	
B1, C3	LVDSGND	Ground	Dedicated GND for LVDS pads.	
C6, F3	DGND	Ground	Digital GND.	
C7, F6	AGND	Ground	Analog GND.	
E7, E8, D7, D8	NC	NC	No connect.	3

Notes:
1. Pin H7 (RSVD) must be tied to GND.
2. Output Enable (OE) tri-states signals DOUT0–DOUT9. No other signals are tri-stated with OE.
3. No connect. These pins must be left floating for proper operation.

Figure 3: Typical Configuration (Connection)—Parallel Output Mode



Note: LVDS signals are to be left floating.

Pixel Data Format

Pixel Array Structure

The MT9V022 pixel array is configured as 782 columns by 492 rows, shown in Figure 4. The left 26 columns and the top eight rows of pixels are optically black and can be used to monitor the black level. The black row data is used internally for the automatic black level adjustment. However, the middle four black rows can also be read out by setting the sensor to raw data output mode. There are 753 columns by 481 rows of optically active pixels. The active area is surrounded with optically transparent dummy columns and rows to improve image uniformity within the active area. One additional active column and active row are used to allow horizontally and vertically mirrored readout to also start on the same color pixel.

Figure 4: Pixel Array Description

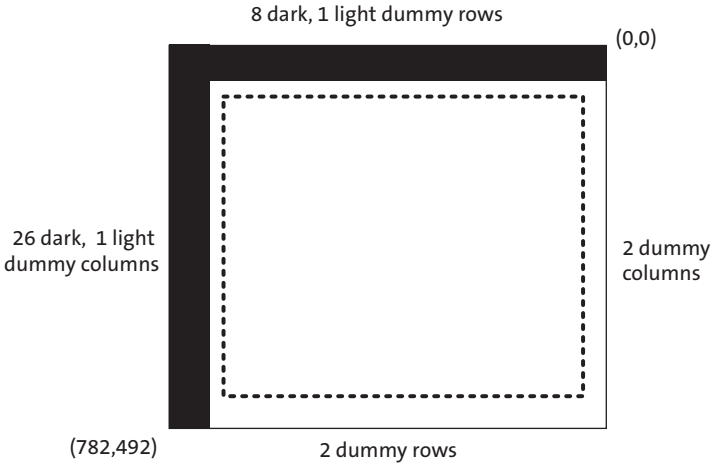
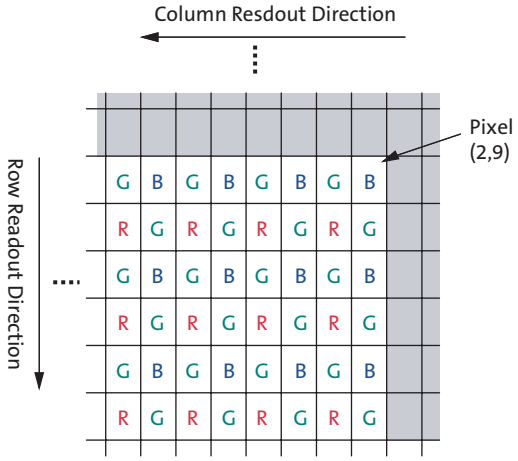


Figure 5: Pixel Color Pattern Detail (Top Right Corner)



Color Device Limitations

The color version of the MT9V022 does not support or offers reduced performance for the following functionalities.

Pixel Binning

Pixel binning is done on immediate neighbor pixels only, no facility is provided to skip pixels according to a Bayer pattern. Therefore, the result of binning combines pixels of different colors. For more information, see "Pixel Binning" on page 34.

Interlaced Readout

Interlaced readout yields one field consisting only of red and green pixels and another consisting only of blue and green pixels. This is due to the Bayer pattern of the CFA.

Automatic Black Level Calibration

When the color bit is set (R0x0F[2]=1), the sensor uses GREEN1 pixels black level correction value, which is applied to all colors. To use calibration value based on all dark pixels offset values, the color bit should be cleared.

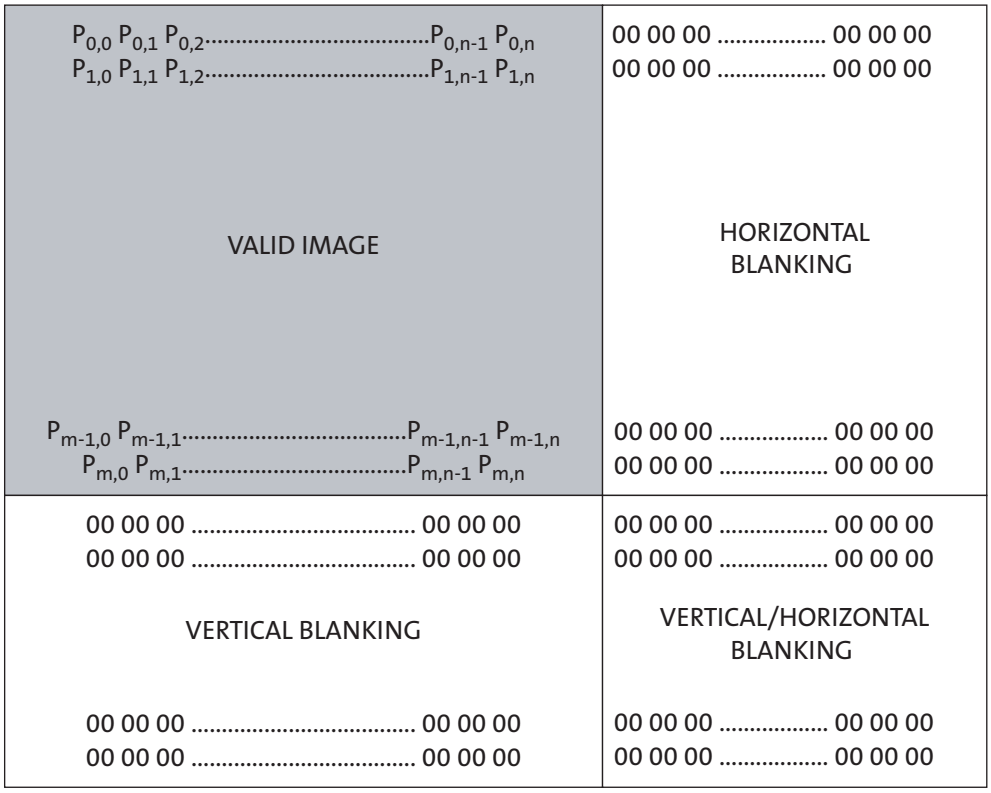
Other Limiting Factors

Black level correction and row-wise noise correction are applied uniformly to each color. Automatic exposure and gain control calculations are made based on all three colors, not just the green luma channel. High dynamic range does operate; however, Aptina strongly recommends limiting use to linear operation if good color fidelity is required.

Output Data Format

The MT9V022 image data can be read out in a progressive scan or interlaced scan mode. Valid image data is surrounded by horizontal and vertical blanking, as shown in Figure 6. The amount of horizontal and vertical blanking is programmable through R0x05 and R0x06, respectively. LINE_VALID is HIGH during the shaded region of the figure. See "Output Data Timing" on page 13 for the description of FRAME_VALID timing.

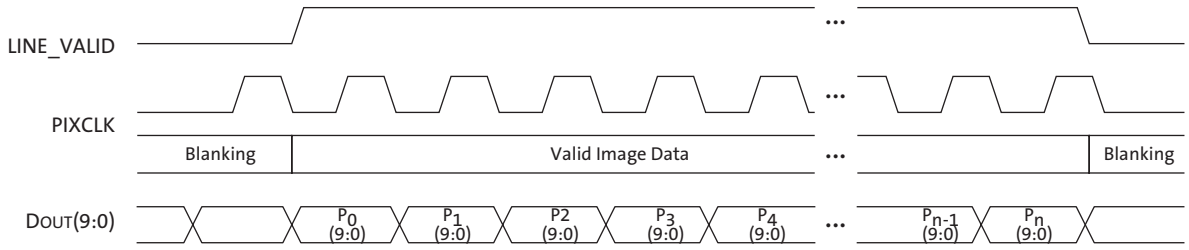
Figure 6: Spatial Illustration of Image Readout



Output Data Timing

The data output of the MT9V022 is synchronized with the PIXCLK output. When LINE_VALID is HIGH, one 10-bit pixel datum is output every PIXCLK period.

Figure 7: Timing Example of Pixel Data



The PIXCLK is a nominally inverted version of the master clock (SYSCLK). This allows PIXCLK to be used as a clock to latch the data. However, when column bin 2 is enabled, the PIXCLK is HIGH for one complete master clock master period and then LOW for one complete master clock period; when column bin 4 is enabled, the PIXCLK is HIGH for two complete master clock periods and then LOW for two complete master clock periods. It is continuously enabled, even during the blanking period. Setting R0x74 bit[4] = 1 causes the MT9V022 to invert the polarity of the PIXCLK.

The parameters P1, A, Q, and P2 in Figure 8 are defined in Table 4.

Figure 8: Row Timing and FRAME_VALID/LINE_VALID Signals

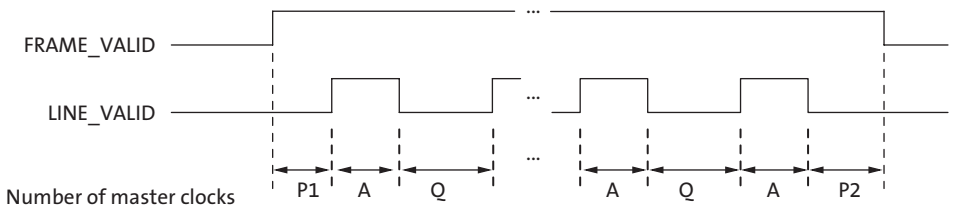


Table 4: Frame Time

Parameter	Name	Equation	Default Timing at 26.66 MHz
A	Active data time	R0x04	752 pixel clocks = 752 master = 28.20µs
P1	Frame start blanking	R0x05 - 23	71 pixel clocks = 71master = 2.66µs
P2	Frame end blanking	23 (fixed)	23 pixel clocks = 23 master = 0.86µs
Q	Horizontal blanking	R0x05	94 pixel clocks = 94 master = 3.52µs

Table 4: Frame Time (continued)

Parameter	Name	Equation	Default Timing at 26.66 MHz
A+Q	Row time	R0x04 + R0x05	846 pixel clocks = 846 master = 31.72µs
V	Vertical blanking	(R0x06) x (A + Q) + 4	38,074 pixel clocks = 38,074 master = 1.43ms
Nrows x (A + Q)	Frame valid time	(R0x03) × (A + Q)	406,080 pixel clocks = 406,080 master = 15.23ms
F	Total frame time	V + (Nrows x (A + Q))	444,154 pixel clocks = 444,154 master = 16.66ms

Sensor timing is shown above in terms of pixel clock and master clock cycles (refer to Figure 7 on page 13). The recommended master clock frequency is 26.66 MHz. The vertical blanking and total frame time equations assume that the number of integration rows (bits 11 through 0 of R0x0B) is less than the number of active rows plus blanking rows minus overhead rows (R0x03 + R0x06 - 2). If this is not the case, the number of integration rows must be used instead to determine the frame time, as shown in Table 5. In this example it is assumed that R0x0B is programmed with 523 rows. For Simultaneous Mode, if the exposure time register (0x0B) exceeds the total readout time, then vertical blanking is internally extended automatically to adjust for the additional integration time required. This extended value is **not** written back to R0x06 (vertical blanking). R0x06 can be used to adjust frame to frame readout time. This register does not effect the exposure time but it may extend the readout time.

Table 5: Frame Time—Long Integration Time

Parameter	Name	Equation (Number of Master Clock Cycles)	Default Timing at 26.66 MHz
V'	Vertical blanking (long integration time)	(R0x0B + 2 - R0x03) × (A + Q) + 4	38,074 pixel clocks = 38,074 master = 1.43ms
F"	Total frame time (long integration time)	(R0x0B + 2) × (A + Q) + 4	444,154 pixel clocks = 444,154 master = 16.66ms

Notes: 1. The MT9V022 uses column parallel analog-digital converters, thus short row timing is not possible. The minimum total row time is 660 columns (horizontal width + horizontal blanking). The minimum horizontal blanking is 43. When the window width is set below 617, horizontal blanking must be increased. The frame rate will not increase for row times less than 660 columns.

Serial Bus Description

Registers are written to and read from the MT9V022 through the two-wire serial interface bus. The MT9V022 is a serial interface slave with four possible IDs (0x90, 0x98, 0xB0 and 0xB8) determined by the S_CTRL_ADR0 and S_CTRL_ADR1 input pins. Data is transferred into the MT9V022 and out through the serial data (SDATA) line. The SDATA line is pulled up to VDD off-chip by a 1.5KΩ resistor. Either the slave or master device can pull the SDATA line down—the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time. The registers are 16-bit wide, and can be accessed through 16- or 8-bit two-wire serial interface sequences.

Protocol

The two-wire serial interface defines several different transmission codes, as follows:

- a start bit
- the slave device 8-bit address
- a(n) (no) acknowledge bit
- an 8-bit message
- a stop bit

Sequence

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request is a read or a write, where a "0" indicates a write and a "1" indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data eight bits at a time, with the slave sending an acknowledge bit after each eight bits. The MT9V022 uses 16-bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write mode slave address and 8-bit register address, just as in the write request. The master then sends a start bit and the read mode slave address. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit. The MT9V022 allows for 8-bit data transfers through the two-wire serial interface by writing (or reading) the most significant 8 bits to the register and then writing (or reading) the least significant 8 bits to R0xF0 (240).

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of 7 bits of address and 1 bit of direction. A "0" in the LSB of the address indicates write mode, and a "1" indicates read mode. As indicated above, the MT9V022 allows four possible slave addresses determined by the two input pins, S_CTRL_ADR0 and S_CTRL_ADR1.

Table 6: Slave Address Modes

{S_CTRL_ADR1, S_CTRL_ADR0}	Slave Address	Write/Read Mode
00	0x90	Write
	0x91	Read
01	0x98	Write
	0x99	Read
10	0xB0	Write
	0xB1	Read
11	0xB8	Write
	0xB9	Read

Data Bit Transfer

One data bit is transferred during each clock pulse. The two-wire serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the serial clock—it can only change when the two-wire serial interface clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

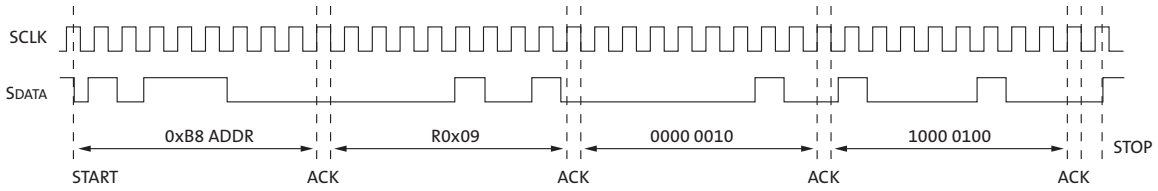
The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Two-Wire Serial Interface Sample Read and Write Sequences

16-Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 9. A start bit given by the master, followed by the write address, starts the sequence. The image sensor then gives an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each 8-bit the image sensor gives an acknowledge bit. All 16 bits must be written before the register is updated. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

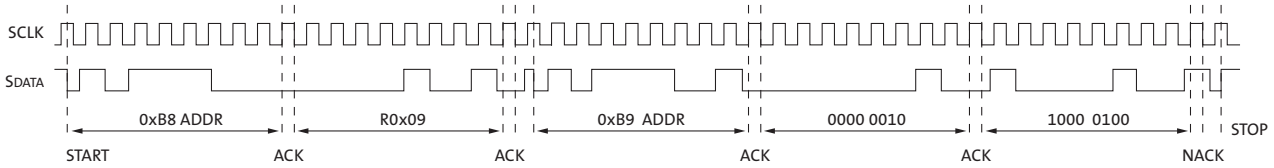
Figure 9: Timing Diagram Showing a Write to R0x09 with the Value 0x0284



16-Bit Read Sequence

A typical read sequence is shown in Figure 10. First the master has to write the register address, as in a write sequence. Then a start bit and the read address specifies that a read is about to happen from the register. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

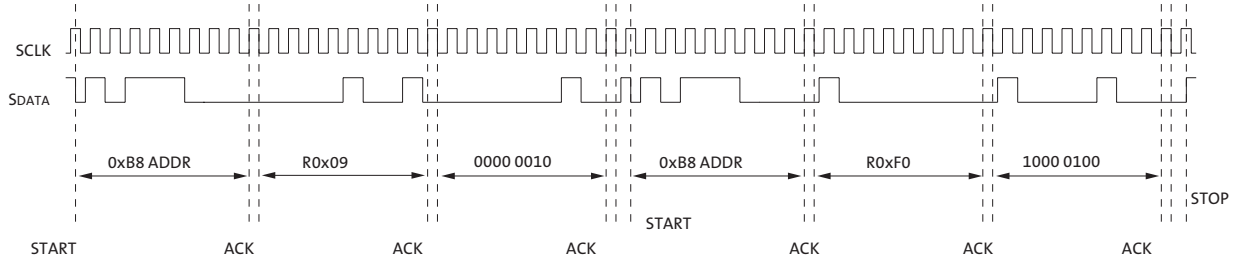
Figure 10: Timing Diagram Showing a Read from R0x09; Returned Value 0x0284



8-Bit Write Sequence

To be able to write 1 byte at a time to the register a special register address is added. The 8-bit write is done by first writing the upper 8 bits to the desired register and then writing the lower 8 bits to the special register address (R0xF0). The register is not updated until all 16 bits have been written. It is not possible to just update half of a register. In Figure 11 on page 18, a typical sequence for 8-bit writing is shown. The second byte is written to the special register (R0xF0).

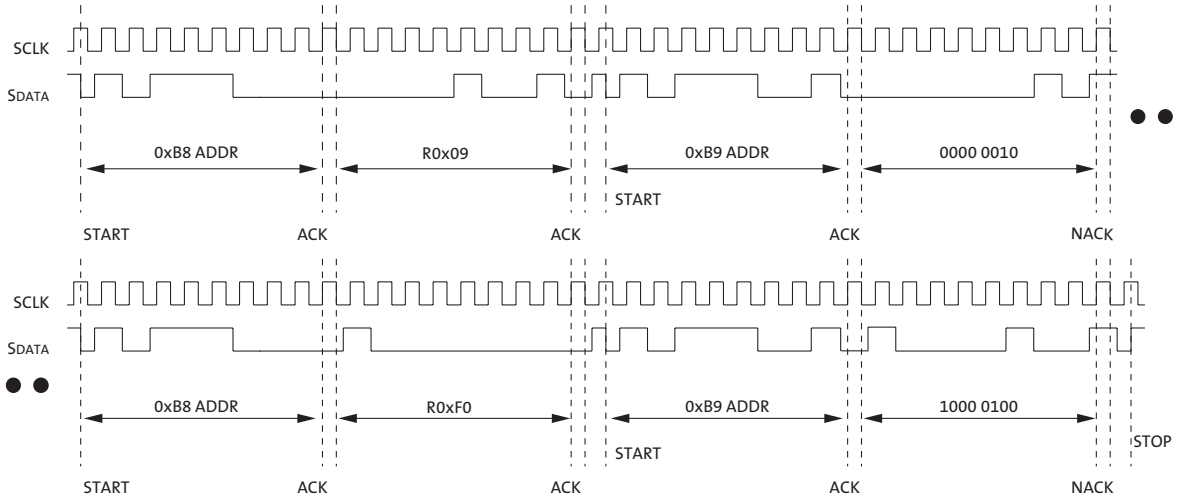
Figure 11: Timing Diagram Showing a Bytewise Write to R0x09 with the Value 0x0284



8-Bit Read Sequence

To read one byte at a time the same special register address is used for the lower byte. The upper 8 bits are read from the desired register. By following this with a read from the special register (R0xF1) the lower 8 bits are accessed (Figure 12). The master sets the no-acknowledge bits shown.

Figure 12: Timing Diagram Showing a Bytewise Read from R0x09; Returned Value 0x0284



Register Lock

Included in the MT9V022 is a register lock (R0xFE) feature that can be used as a solution to reduce the probability of an inadvertent noise-triggered two-wire serial interface write to the sensor. All registers (or read mode register—register 13 only) can be locked; it is important to prevent an inadvertent two-wire serial interface write to register 13 in automotive applications since this register controls the image orientation and any unintended flip to an image can cause serious results.

At power-up, the register lock defaults to a value of 0xBEEF, which implies that all registers are unlocked and any two-wire serial interface writes to the register gets committed.

Lock All Registers

If a unique pattern (0xDEAD) to R0xFE is programmed, any subsequent two-wire serial interface writes to registers (except R0xFE) are NOT committed. Alternatively, if the user writes a 0xBEEF to the register lock register, all registers are unlocked and any subsequent two-wire serial interface writes to the register are committed.

Lock Read Mode Register Only (R0x0D)

If a unique pattern (0xDEAF) to R0xFE is programmed, any subsequent two-wire serial interface writes to register 13 is NOT committed. Alternatively, if the user writes a 0xBEEF to register lock register, register 13 is unlocked and any subsequent two-wire serial interface writes to this register is committed.

Feature Description

Operational Modes

The MT9V022 works in master, snapshot, or slave mode. In master mode the sensor generates the readout timing. In snapshot mode it accepts an external trigger to start integration, then generates the readout timing. In slave mode the sensor accepts both external integration and readout controls. The integration time is programmed through the two-wire serial interface during master or snapshot modes, or controlled via externally generated control signal during slave mode.

Master Mode

There are two possible operation methods for master mode: simultaneous and sequential. One of these operation modes must be selected via the two-wire serial interface.

Simultaneous Master Mode

In simultaneous master mode, the exposure period occurs during readout. The frame synchronization waveforms are shown in Figure 13 and Figure 14. The exposure and readout happen in parallel rather than sequential, making this the fastest mode of operation.

Figure 13: Simultaneous Master Mode Synchronization Waveforms #1

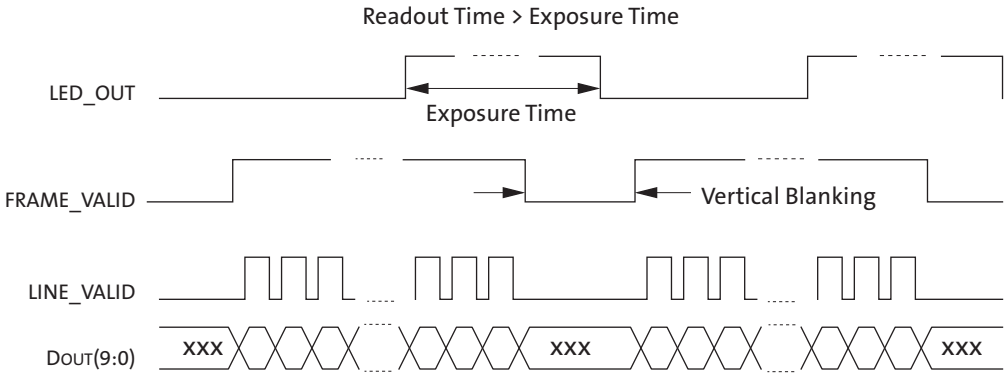
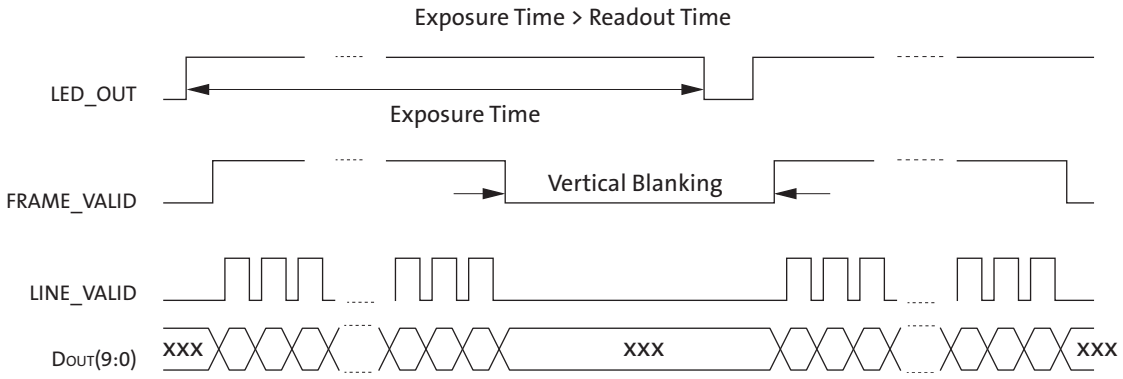


Figure 14: Simultaneous Master Mode Synchronization Waveforms #2

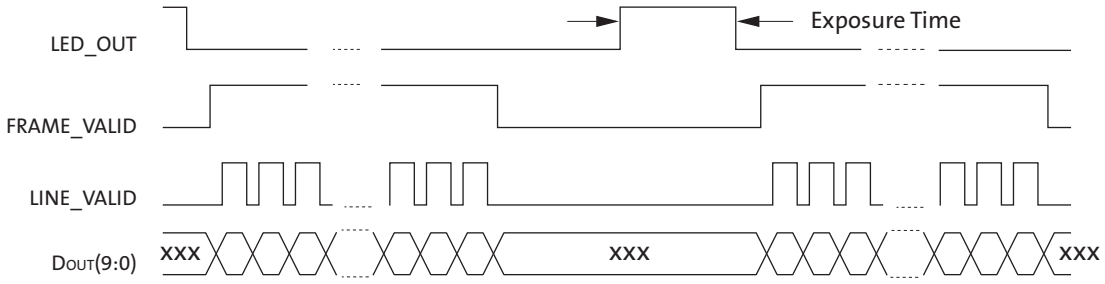


When exposure time is greater than the sum of vertical blank and window height, the number of vertical blank rows is increased automatically to accommodate the exposure time.

Sequential Master Mode

In sequential master mode the exposure period is followed by readout. The frame synchronization waveforms for sequential master mode are shown in Figure 15. The frame rate changes as the integration time changes.

Figure 15: Sequential Master Mode Synchronization Waveforms



Snapshot Mode

In snapshot mode the sensor accepts an input trigger signal which initiates exposure, and is immediately followed by readout. Figure 16 shows the interface signals used in snapshot mode. In snapshot mode, the start of the integration period is determined by the externally applied EXPOSURE pulse that is input to the MT9V022. The integration time is preprogrammed via the two-wire serial interface on R0x0B. After the frame's integration period is complete the readout process commences and the syncs and data are output. Sensor in snapshot mode can capture a single image or a sequence of images. The frame rate may only be controlled by changing the period of the user supplied EXPOSURE pulse train. The frame synchronization waveforms for snapshot mode are shown in Figure 17.

Figure 16: Snapshot Mode Interface Signals

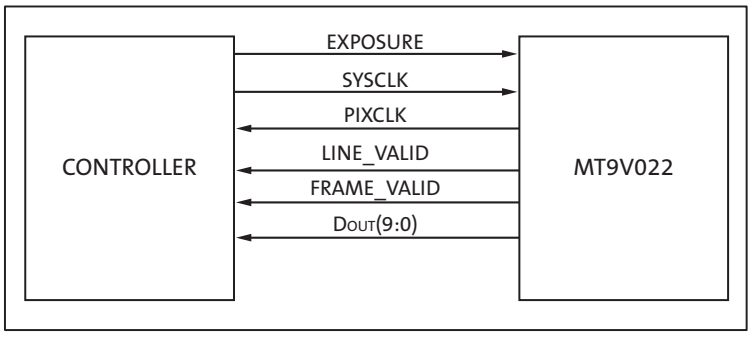
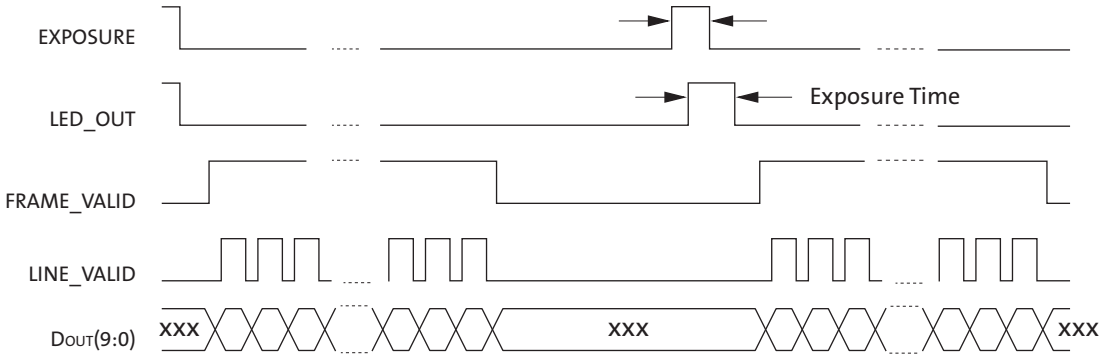


Figure 17: Snapshot Mode Frame Synchronization Waveforms



Slave Mode

In slave mode, the exposure and readout are controlled using the EXPOSURE, STFRM_OUT, and STLN_OUT pins. When the slave mode is enabled, STFRM_OUT and STLN_OUT become input pins.

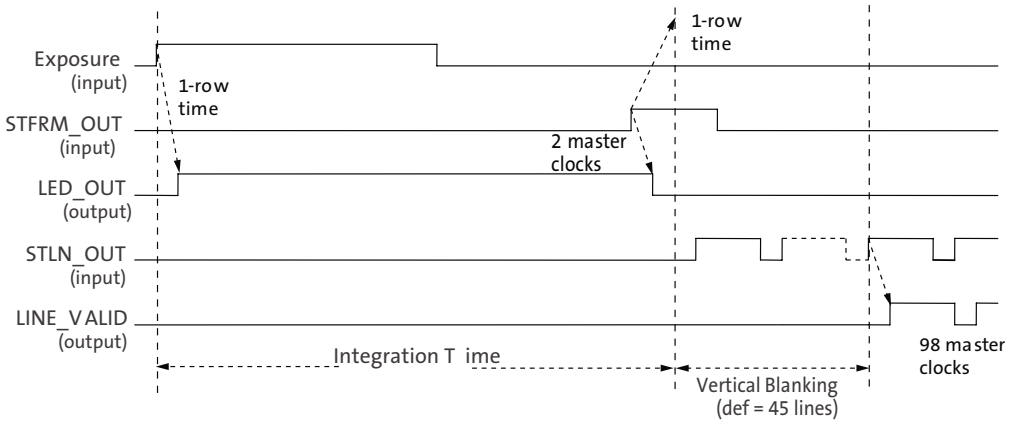
The start and end of integration are controlled by EXPOSURE and STFRM_OUT pulses, respectively. While a STFRM_OUT pulse is used to stop integration, it is also used to enable the readout process.

After integration is stopped, the user provides STLN_OUT pulses to trigger row readout. A full row of data is read out with each STLN_OUT pulse. The user must provide enough time between successive STLN_OUT pulses to allow the complete readout of one row.

It is also important to provide additional STLN_OUT pulses to allow the sensors to read the vertical blanking rows. It is recommended that the user program the vertical blank register (R0x06) with a value of 4, and achieve additional vertical blanking between frames by delaying the application of the STFRM_OUT pulse.

The elapsed time between the rising edge of STLN_OUT and the first valid pixel data is [horizontal blanking register (R0x05) + 4] clock cycles.

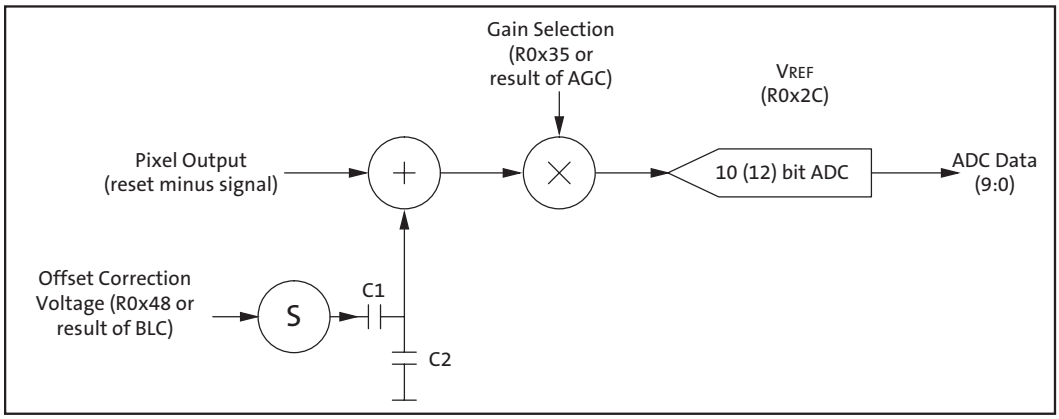
Figure 18: Slave Mode Operation



Signal Path

The MT9V022 signal path consists of a programmable gain, a programmable analog offset, and a 10-bit ADC. See "Black Level Calibration" on page 30 for the programmable offset operation description.

Figure 19: Signal Path



On-Chip Biases

ADC Voltage Reference

The ADC voltage reference is programmed through R0x2C, bits 2:0. The ADC reference ranges from 1.0V to 2.1V. The default value is 1.4V. The increment size of the voltage reference is 0.1V from 1.0V to 1.6V (R0x2C[2:0] values 0 to 6). At R0x2C[2:0] = 7, the reference voltage jumps to 2.1V.

The effect of the ADC calibration does not scale with VREF. Instead it is a fixed value relative to the output of the analog gain stage. At default, one LSB of calibration equals two LSB in output data ($1LSB_{Offset}$ = 2mV, $1LSB_{ADC}$ = 1mV).

It is very important to preserve the correct values of the other bits in R0x2C. The default register setting is 0x0004.

V_Step Voltage Reference

This voltage is used for pixel high dynamic range operations, programmable from R0x31 through R0x34.

Chip Version

Chip version registers R0x00 and R0xFF are read-only.

Window Control

Registers R0x01 column start, R0x02 Row Start, R0x03 window height (row size), and R0x04 Window Width (column size) control the size and starting coordinates of the window.

The values programmed in the window height and width registers are the exact window height and width out of the sensor. The window start value should never be set below four.

To read out the dark rows set bit 6 of R0x0D. In addition, bit 7 of R0x0D can be used to display the dark columns in the image.

Blanking Control

Horizontal blanking and vertical blanking registers R0x05 and R0x06 respectively control the blanking time in a row (horizontal blanking) and between frames (vertical blanking).

- Horizontal blanking is specified in terms of pixel clocks.
- Vertical blanking is specified in terms of numbers of rows.

The actual imager timing can be calculated using Table 4 on page 13 and Table 5 on page 14 which describe "Row Timing and FRAME_VALID/LINE_VALID signals." The minimum number of vertical blank rows is 4.

Pixel Integration Control

Total Integration

R0x0B Total Shutter Width (In Terms of Number of Rows)

This register (along with the window width and horizontal blanking registers) controls the integration time for the pixels.

The actual total integration time, ^{t}INT, is:

^{t}INT = (Number of rows of integration × row time) + Overhead, where:
The number of rows integration is equal to the result of automatic exposure control (AEC) which may vary from frame to frame, or, if AEC is disabled, the value in R0x0B
Row time = (R0x04 + R0x05) master clock periods
Overhead = (R0x04 + R0x05 – 255) master clock periods

Typically, the value of R0x0B (total shutter width) is limited to the number of rows per frame (which includes vertical blanking rows), such that the frame rate is not affected by the integration time. If R0x0B is increased beyond the total number of rows per frame, it is required to add additional blanking rows using R0x06 as needed. A second constraint is that ^{t}INT must be adjusted to avoid banding in the image from light flicker. Under 60Hz flicker, this means frame time must be a multiple of 1/120 of a second. Under 50Hz flicker, frame time must be a multiple of 1/100 of a second.

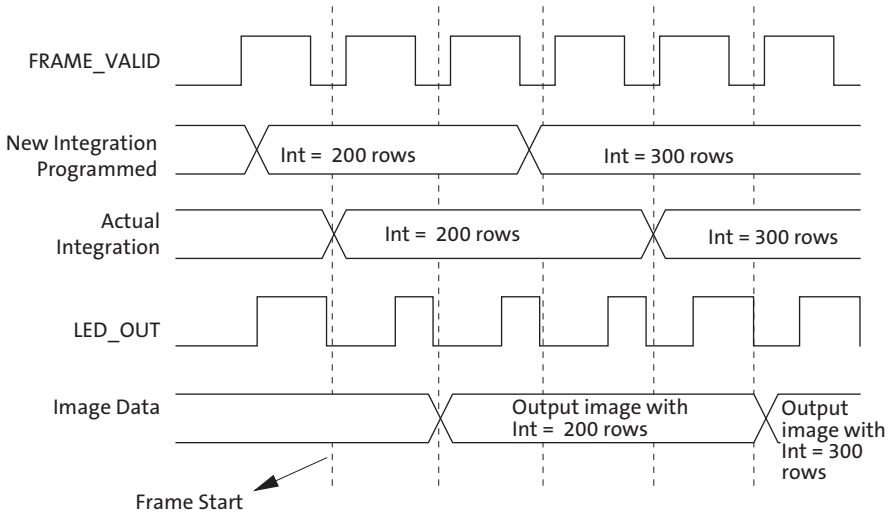
Changes to Integration Time

With automatic exposure control disabled (R0xAF, bit 0 is cleared to LOW), and if the total integration time (R0x0B) is changed via the two-wire serial interface while FRAME_VALID is asserted for frame *n*, the first frame output using the new integration time is frame (*n* + *2*). Similarly, when automatic exposure control is enabled, any change to the integration time for frame *n* first appears in frame (*n* + *2*) output.

The sequence is as follows:

1. During frame *n*, the new integration time is held in the R0x0B live register.
2. At the start of frame (*n* + *1*), the new integration time is transferred to the exposure control module. Integration for each row of frame (*n* + *1*) has been completed using the old integration time. The earliest time that a row can start integrating using the new integration time is immediately after that row has been read for frame (*n* + *1*). The actual time that rows start integrating using the new integration time is dependent on the new value of the integration time.
3. When frame (*n* + *1*) is read out, it is integrated using the new integration time. If the integration time is changed (R0x0B written) on successive frames, each value written is applied to a single frame; the latency between writing a value and it affecting the frame readout remains at two frames.
   However, when automatic exposure control is disabled, if the integration time is changed through the two-wire serial interface after the falling edge of FRAME_VALID for frame *n*, the first frame output using the new integration time becomes frame (*n* + *3*).

Figure 20: Latency When Changing Integration



Exposure Indicator

The exposure indicator is controlled by:

- R0x1B LED_OUT Control

The MT9V022 provides an output pin, LED_OUT, to indicate when the exposure takes place. When R0x1B bit 0 is clear, LED_OUT is HIGH during exposure. By using R0x1B, bit 1, the polarity of the LED_OUT pin can be inverted.

High Dynamic Range

High dynamic range is controlled by:

- R0x08 Shutter Width 1
- R0x09 Shutter Width 2
- R0x0A Shutter Width Control
- R0x31–R0x34 V_Step Voltages

In the MT9V022, high dynamic range (that is, R0x0F, bit 6 = 1) is achieved by controlling the saturation level of the pixel (HDR or high dynamic range gate) during the exposure period. The sequence of the control voltages at the HDR gate is shown in Figure 21. After the pixels are reset, the step voltage, V_Step, which is applied to HDR gate, is setup at V1 for integration time t_1 then to V2 for time t_2, then V3 for time t_3, and finally it is parked at V4, which also serves as an antiblooming voltage for the photodetector. This sequence of voltages leads to a piecewise linear pixel response, illustrated (in approximates) in Figure 21 on page 26.

Figure 21: Sequence of Control Voltages at the HDR Gate

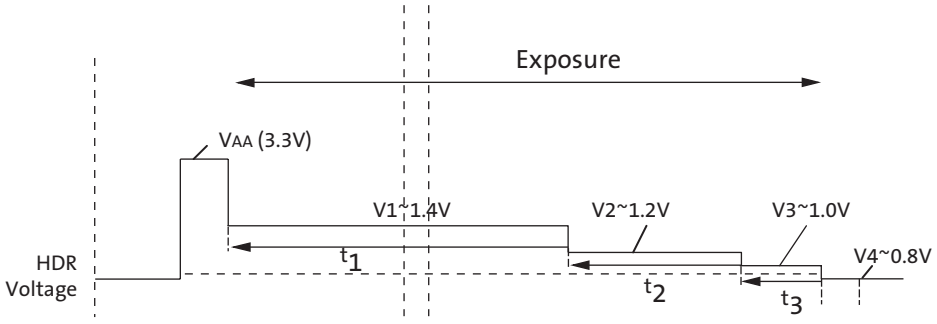
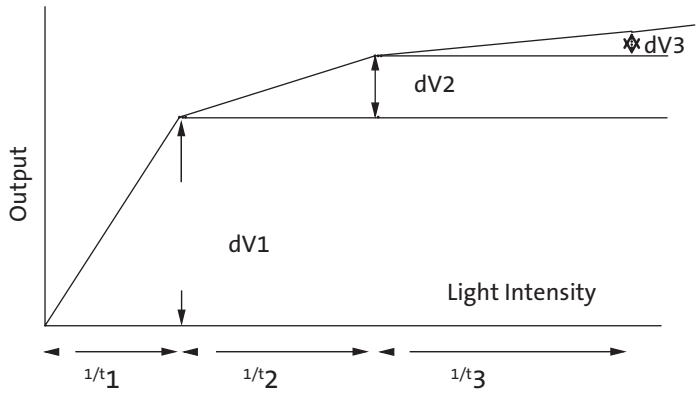


Figure 22: Sequence of Voltages in a Piecewise Linear Pixel Response



The parameters of the step voltage V_Step which takes values V1, V2, and V3 directly affect the position of the knee points in Figure 22.

Light intensities work approximately as a reciprocal of the partial exposure time. Typically, $^{t}1$ is the longest exposure, $^{t}2$ shorter, and so on. Thus the range of light intensities is shortest for the first slope, providing the highest sensitivity.

The register settings for V_Step and partial exposures are:

V1 = R0x31, bits 4:0
V2 = R0x32, bits 4:0
V3 = R0x33, bits 4:0
V4 = R0x34, bits 4:0
$^{t}INT = {}^{t}1 + {}^{t}2 + {}^{t}3$

There are two ways to specify the knee points timing, the first by manual setting (default) and the second by automatic knee point adjustment.

When the auto adjust enabler is set to HIGH (LOW by default), the MT9V022 calculates the knee points automatically using the following equations:

$$^{t}1 = {}^{t}INT - {}^{t}2 - {}^{t}3 \quad \textit{(EQ 1)}$$

$$^{t}2 = {}^{t}INT \times (½)^{R0x0A,\ bits\ 3:0} \quad \textit{(EQ 2)}$$

$$^{t}3 = {}^{t}INT \times (½)^{R0x0A,\ bits\ 7:4} \quad \textit{(EQ 3)}$$

As a default for auto exposure, $^{t}2$ is 1/16 of ^{t}INT, $^{t}3$ is 1/64 of ^{t}INT.

When the auto adjust enabler is disabled (default), $^{t}1$, $^{t}2$, and $^{t}3$ may be programmed through the two-wire serial interface:

$$^{t}1 = R0x08,\ bits\ 14:0 \quad \textit{(EQ 4)}$$

$$^{t}2 = (R0x09,\ bits\ 14:0) - (R0x08,\ bits\ 14:0) \quad \textit{(EQ 5)}$$

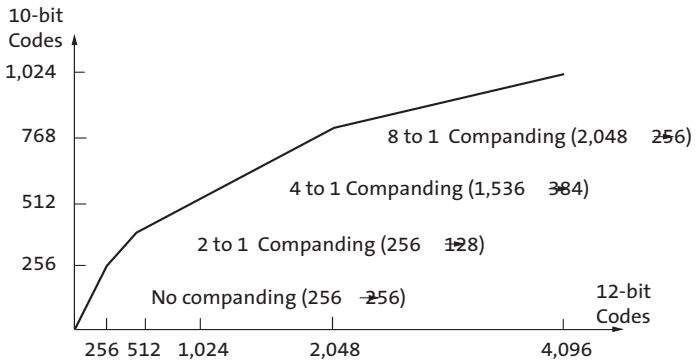
$$^{t}3 = {}^{t}INT - {}^{t}1 - {}^{t}2 \quad \textit{(EQ 6)}$$

^{t}INT may be based on the manual setting of R0x0B or the result of the AEC. If the AEC is enabled then the auto knee adjust must also be enabled.

Variable ADC Resolution

By default, ADC resolution of the sensor is 10-bit. Additionally, a companding scheme of 12-bit into 10-bit is enabled by the R0x1C (28). This mode allows higher ADC resolution which means less quantization noise at low-light, and lower resolution at high light, where good ADC quantization is not so critical because of the high level of the photon's shot noise.

Figure 23: 12- to 10-Bit Companding Chart



Gain Settings

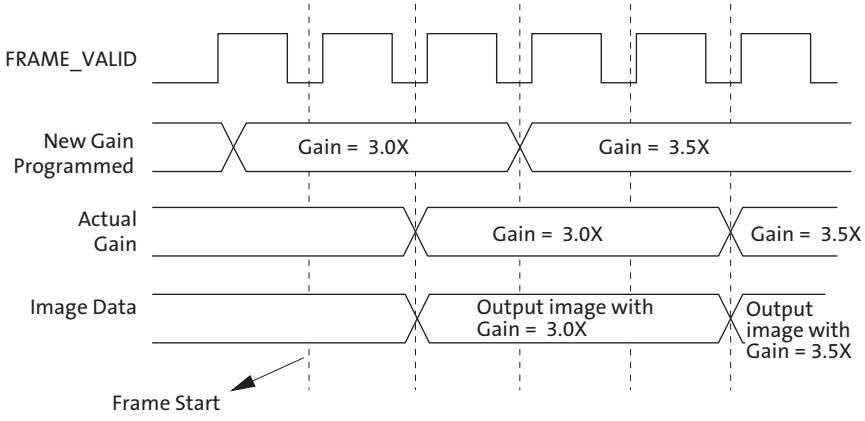
Changes to Gain Settings

When the digital gain settings (R0x80–R0x98) are changed, the gain is updated on the next frame start. However, the latency for an analog gain change to take effect depends on the automatic gain control.

If automatic gain control is enabled (R0xAF, bit 1 is set to HIGH), the gain changed for frame *n* first appears in frame (*n* + *1*); if the automatic gain control is disabled, the gain changed for frame *n* first appears in frame (*n* + *2*).

Both analog and digital gain change regardless of whether the integration time is also changed simultaneously.

Figure 24: Latency of Analog Gain Change When AGC Is Disabled



Analog Gain

Analog gain is controlled by:

- R0x35 Global Gain

The formula for gain setting is:

$$Gain = Bits[6:0] \times 0.0625 \quad \text{(EQ 7)}$$

The analog gain range supported in the MT9V022 is 1X–4X with a step size of 6.25 percent. To control gain manually with this register, the sensor must NOT be in AGC mode. When adjusting the luminosity of an image, it is recommended to alter exposure first and yield to gain increases only when the exposure value has reached a maximum limit.

Analog gain = bits (6:0) x 0.0625 for values 16–31

Analog gain = bits (6:0)/2 x 0.125 for values 32–64

For values 16–31: each LSB increases analog gain 0.0625v/v. A value of 16 = 1X gain. Range: 1X to 1.9375X.

For values 32–64: each 2 LSB increases analog gain 0.125v/v (that is, double the gain increase for 2 LSB). Range: 2X to 4X. Odd values do not result in gain increases; the gain increases by 0.125 for values 32, 34, 36, and so on.

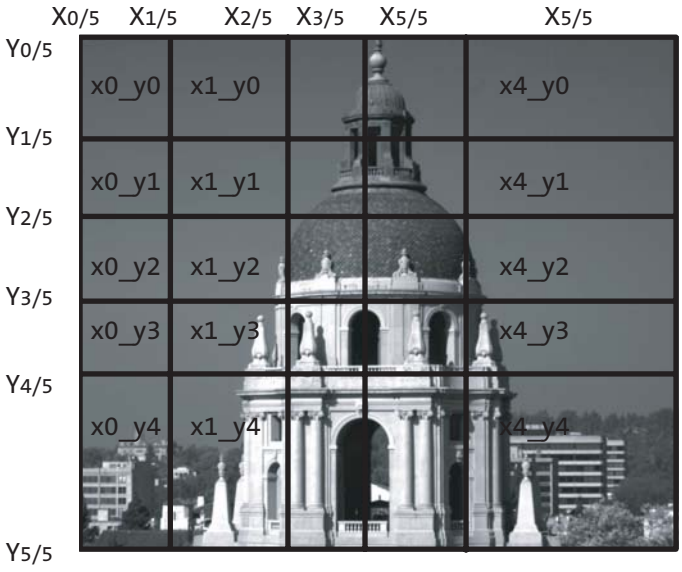
Digital Gain

Digital gain is controlled by:

- R0x99–R0xA4 Tile Coordinates
- R0x80–R0x98 Tiled Digital Gain and Weight

In the MT9V022, the image may be divided into 25 tiles, as shown in Figure 25, through the two-wire serial interface, and apply digital gain individually to each tile.

Figure 25: Tiled Sample



Registers 0x99–0x9E and 0x9F–0xA4 represent the coordinates $X_{0/5}$-$X_{5/5}$ and $Y_{0/5}$-$Y_{5/5}$ in Figure 25, respectively.

Digital gains of registers 0x80–0x98 apply to their corresponding tiles. The MT9V022 supports a digital gain of 0.25-3.75X.

The formula for digital gain setting is:

$$Digital\ Gain = Bits[3:0] \times 0.25 \quad (EQ\ 8)$$

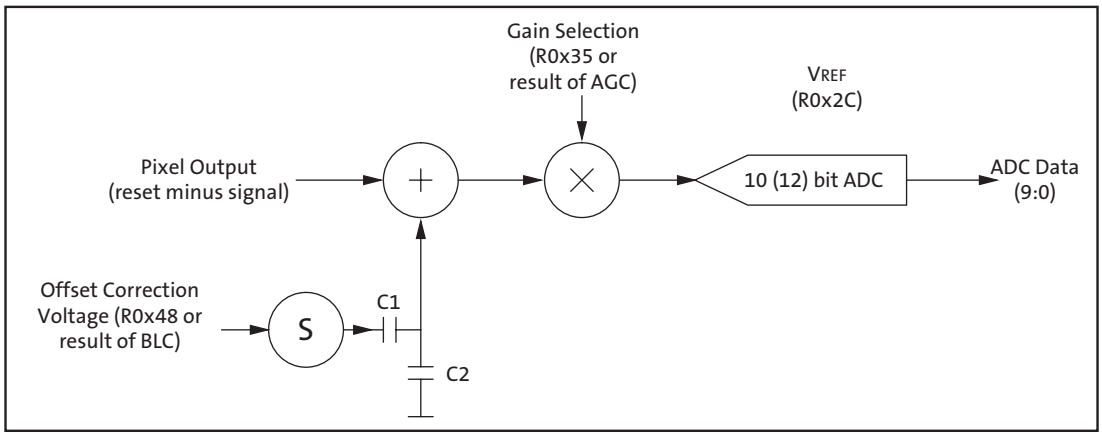
Black Level Calibration

Black level calibration is controlled by:

- R0x4C
- R0x42
- R0x46–R0x48

The MT9V022 has automatic black level calibration on-chip, and if enabled, its result may be used in the offset correction shown in Figure 26.

Figure 26: Black Level Calibration Flow Chart



The automatic black level calibration measures the average value of pixels from 2 dark rows (1 dark row if row bin 4 is enabled) of the chip. (The pixels are averaged as if they were light-sensitive and passed through the appropriate gain.)

This row average is then digitally low-pass filtered over many frames (R0x47, bits 7:5) to remove temporal noise and random instabilities associated with this measurement.

Then, the new filtered average is compared to a minimum acceptable level, low threshold, and a maximum acceptable level, high threshold.

If the average is lower than the minimum acceptable level, the offset correction voltage is increased by a programmable offset LSB in R0x4C. (Default step size is 2 LSB Offset = 1 ADC LSB at analog gain = 1X.)

If it is above the maximum level, the offset correction voltage is decreased by 2 LSB (default).

To avoid oscillation of the black level from below to above, the region the thresholds should be programmed so the difference is at least two times the offset DAC step size.

In normal operation, the black level calibration value/offset correction value is calculated at the beginning of each frame and can be read through the two-wire serial interface from R0x48. This register is an 8-bit signed two's complement value.

However, if R0x47, bit 0 is set to "1," the calibration value in R0x48 may be manually set to override the automatic black level calculation result. This feature can be used in conjunction with the "show dark rows" feature (R0x0D, bit 6) if using an external black level calibration circuit.

The offset correction voltage is generated according to the following formulas:

$$Offset\ Correction\ Voltage = (8\text{-}bit\ signed\ two's\ complement\ calibration\ value, -127\ to\ 127) \times 0.5mV \quad \text{(EQ 9)}$$

$$ADC\ input\ voltage = (Pixel\ Output\ Voltage + Offset\ Correction\ Voltage) \times Analog\ Gain \quad \text{(EQ 10)}$$

Row-wise Noise Correction

Row-wise noise correction is controlled by the following registers:

- R0x70 Row Noise Control
- R0x72 Row Noise Constant
- R0x73 Dark Column Start

When the row-wise noise cancellation algorithm is enabled, the average value of the dark columns read out is used as a correction for the whole row. The row-wise correction is in addition to the general black level correction applied to the whole sensor frame and cannot be used to replace the latter. The dark average is subtracted from each pixel belonging to the same row, and then a positive constant is added (R0x72, bits 7:0). This constant should be set to the dark level targeted by the black level algorithm plus the noise expected on the measurements of the averaged values from dark columns; it is meant to prevent clipping from negative noise fluctuations.

$$Pixel\ value = ADC\ value - dark\ column\ average + row\ noise\ constant \quad (EQ\ 11)$$

On a per-row basis, the dark column average is calculated from a programmable number of dark columns (pixels) values (R0x70, bits 3:0). The default is 10 dark columns. Of these, the maximum and minimum values are removed and then the average is calculated. If R0x70, bits 3:0 are set to "0" (2 pixels), it is essentially equivalent to disabling the dark average calculation since the average is equal to "0" after the maximum and minimum values are removed.

R0x73 is used to indicate the starting column address of dark pixels which row-noise correction algorithm uses for calculation. In the MT9V022, dark columns which may be used are 759–776. R0x73 is used to select the starting column for the calculation.

One additional note in setting the row-noise correction register:

$$777 < (R0x73,\ bits\ 9{:}0) + number\ of\ dark\ pixels\ programmed\ in\ R0x70,\ bits\ 3{:}0 - 1 \quad (EQ\ 12)$$

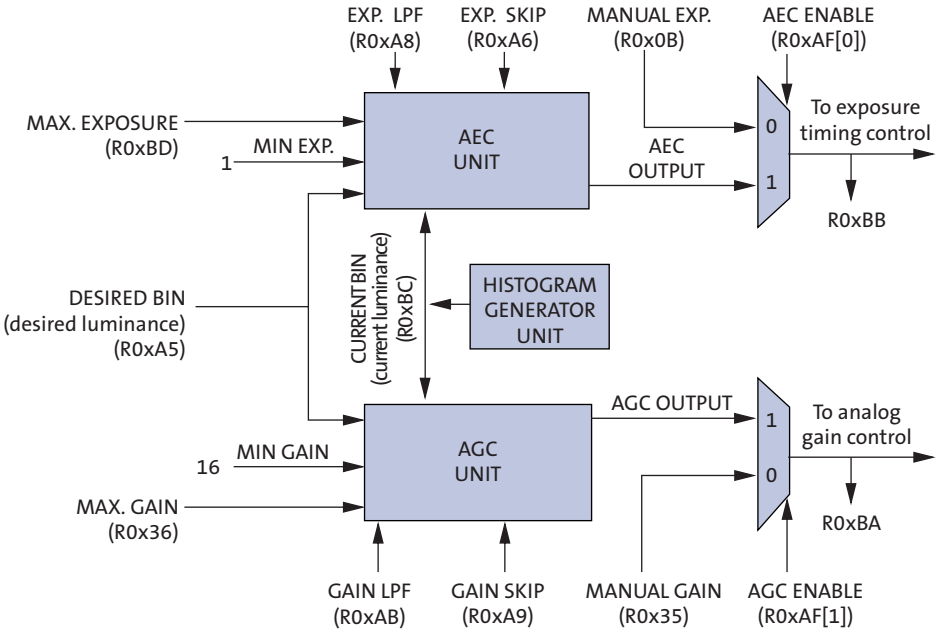
This is to ensure the column pointer does not go beyond the limit the MT9V022 can support.

Automatic Gain Control and Automatic Exposure Control

The integrated AEC/AGC unit is responsible for ensuring that optimal auto settings of exposure and (analog) gain are computed and updated every frame.

AEC and AGC can be individually enabled or disabled by R0xAF. When AEC is disabled (R0xAF[0] = 0), the sensor uses the manual exposure value in R0x0B. When AGC is disabled (R0xAF[1] = 0), the sensor uses the manual gain value in R0x35. See Aptina Technical Note TN-09-17, "MT9V022 AEC and AGC Functions," for further details.

Figure 27: Controllable and Observable AEC/AGC Registers



The exposure is measured in row-time by reading R0xBB. The exposure range is 1 to 2047. The gain is measured in gain-units by reading R0xBA. The gain range is 16 to 63 (unity gain = 16 gain-units; multiply by 1/16 to get the true gain).

When AEC is enabled (R0xAF[0] = 1), the maximum auto exposure value is limited by R0xBD; minimum auto exposure is fixed at 1 row.

When AGC is enabled (R0xAF[1] = 1), the maximum auto gain value is limited by R0x36; minimum auto gain is fixed to 16 gain-units.

The exposure control measures current scene luminosity and desired output luminosity by accumulating a histogram of pixel values while reading out a frame. The desired exposure and gain are then calculated from this for subsequent frame.

Pixel Clock Speed

The pixel clock speed is same as the master clock (SYSCLK) at 26.66 MHz by default. However, when column binning 2 or 4 (R0x0D, bit 2 or 3) is enabled, the pixel clock speed is reduced by half and one-fourth of the master clock speed respectively. See "Read Mode Options" on page 34 and "Column Binning" on page 35 for additional information.

Hard Reset of Logic

The RC circuit for the MT9V022 uses a 10kΩ resistor and a 0.1μF capacitor. The rise time for the RC circuit is 1μs maximum.

Soft Reset of Logic

Soft reset of logic is controlled by:

- R0x0C Reset

Bit 0 is used to reset the digital logic of the sensor while preserving the existing two-wire serial interface configuration. Furthermore, by asserting the soft reset, the sensor aborts the current frame it is processing and starts a new frame. Bit 1 is a shadowed reset control register bit to explicitly reset the automatic gain and exposure control feature.

These two bits are self-resetting bits and also return to “0” during two-wire serial interface reads.

STANDBY Control

The sensor goes into standby mode by setting STANDBY to HIGH. Once the sensor detects that STANDBY is asserted, it completes the current frame before disabling the digital logic, internal clocks, and analog power enable signal. To release the sensor out from the standby mode, reset STANDBY back to LOW. The LVDS must be powered to ensure that the device is in standby mode. See "Appendix B – Power-On Reset and Standby Timing" on page 52 for more information on standby.

Monitor Mode Control

Monitor mode is controlled by:

- R0x0E Monitor Mode Enable
- R0xC0 Monitor Mode Image Capture Control

The sensor goes into monitor mode when R0x0E bit 0 is set to HIGH. In this mode, the sensor first captures a programmable number of frames (R0xC0), then goes into a sleep period for five minutes. The cycle of sleeping for five minutes and waking up to capture a number of frames continues until R0x0E bit 0 is cleared to return to normal operation.

In some applications when monitor mode is enabled, the purpose of capturing frames is to calibrate the gain and exposure of the scene using automatic gain and exposure control feature. This feature typically takes less than 10 frames to settle. In case a larger number of frames is needed, the value of R0xC0 may be increased to capture more frames.

During the sleep period, none of the analog circuitry and a very small fraction of digital logic (including a five-minute timer) is powered. The master clock (SYSCLK) is therefore always required.

Read Mode Options

(Also see "Output Data Format" on page 11 and "Output Data Timing" on page 13.)

Column Flip

By setting bit 5 of R0x0D the readout order of the columns is reversed, as shown in Figure 28 on page 34.

Row Flip

By setting bit 4 of R0x0D the readout order of the rows is reversed, as shown in Figure 29 on page 34.

Figure 28: Readout of Six Pixels in Normal and Column Flip Output Mode

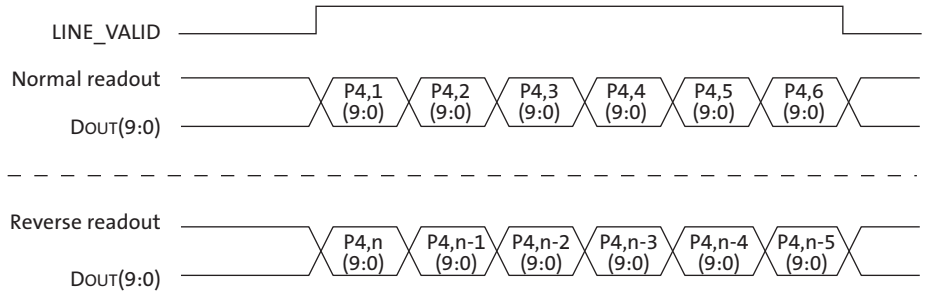
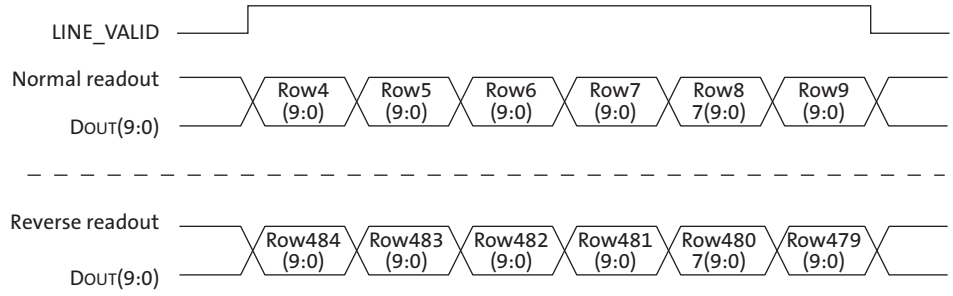


Figure 29: Readout of Six Rows in Normal and Row Flip Output Mode



Pixel Binning

In addition to windowing mode in which smaller resolution (CIF, QCIF) is obtained by selecting small window from the sensor array, the MT9V022 also provides the ability to show the entire image captured by pixel array with smaller resolution by pixel binning. Pixel binning is based on combining signals from adjacent pixels by averaging. There are two options: binning 2 and binning 4. When binning 2 is on, 4 pixel signals from 2 adjacent rows and columns are combined. In binning 4 mode, 16 pixels are combined from 4 adjacent rows and columns. The image mode may work in conjunction with image flip. The binning operation increases SNR but decreases resolution.

Enabling row bin2 and row bin4 improves frame rate by 2x and 4x respectively. The feature of column binning does not increase the frame rate in less resolution modes.

Row Binning

By setting bit 0 or 1 of R0x0D, only half or one-fourth of the row set is read out, as shown in figure below. The number of rows read out is half or one-fourth of what is set in R0x03.

Column Binning

In setting bit 2 or 3 of R0x0D, the pixel data rate is slowed down by a factor of either two or four, respectively. This is due to the overhead time in the digital pixel data processing chain. As a result, the pixel clock speed is also reduced accordingly.

Figure 30: Readout of 8 Pixels in Normal and Row Bin Output Mode

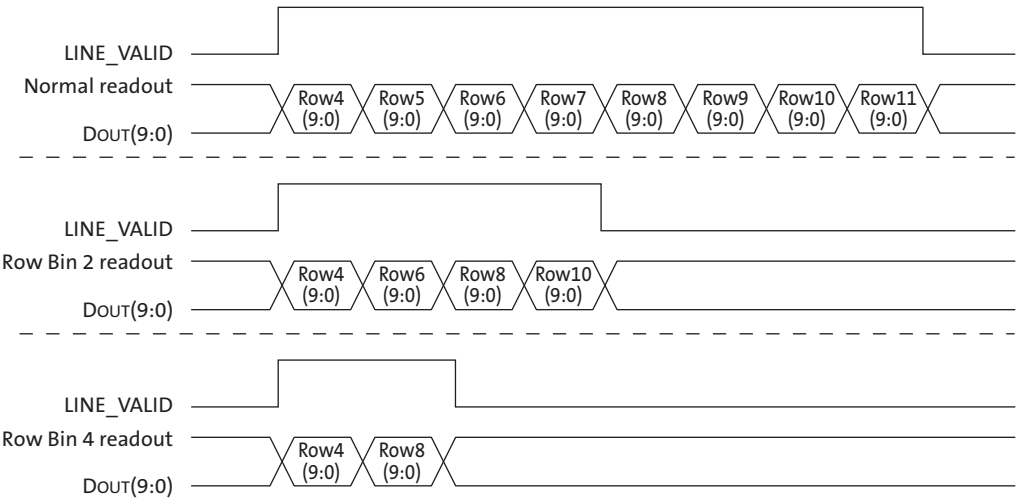
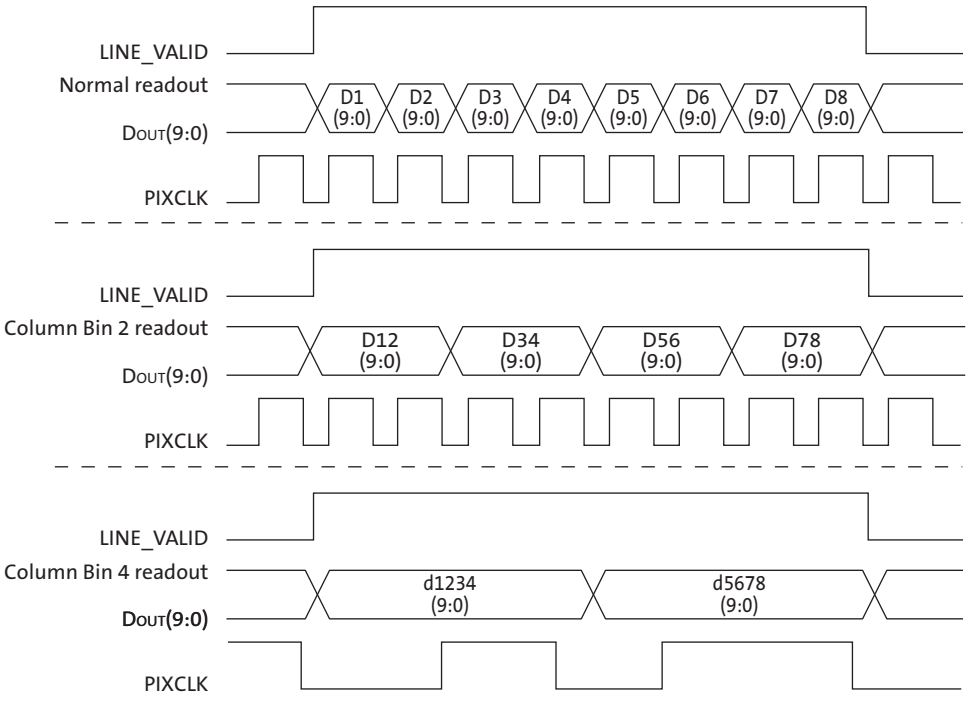


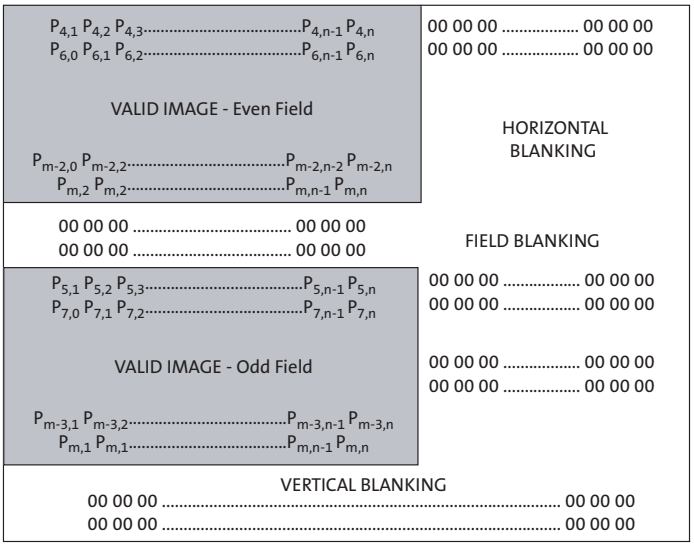
Figure 31: Readout of 8 Pixels in Normal and Column Bin Output Mode



Interlaced Readout

The MT9V022 has two interlaced readout options. By setting R0x07[2:0] = 1, all the even-numbered rows are read out first, followed by a number of programmable field blanking (R0xBF, bits 7:0), and then the odd-numbered rows and finally vertical blanking (minimum is 4 blanking rows). By setting R0x07[2:0] = 2, only one field is read out; consequently, the number of rows read out is half what is set in R0x03. The row start address (R0x02) determines which field gets read out; if the row start address is even, the even field is read out; if row start address is odd, the odd field is read out.

Figure 32: Spatial Illustration of Interlaced Image Readout



When interlaced mode is enabled, the total number of blanking rows are determined by both field blanking register (R0xBF) and vertical blanking register (R0x06). The followings are their equations.

$$Field\ Blanking = R0xBF,\ bits\ 7:0 \quad (EQ\ 13)$$

$$Vertical\ Blanking = R0x06,\ bits\ 8:0 - R0xBF,\ bits\ 7:0 \quad (EQ\ 14)$$

with

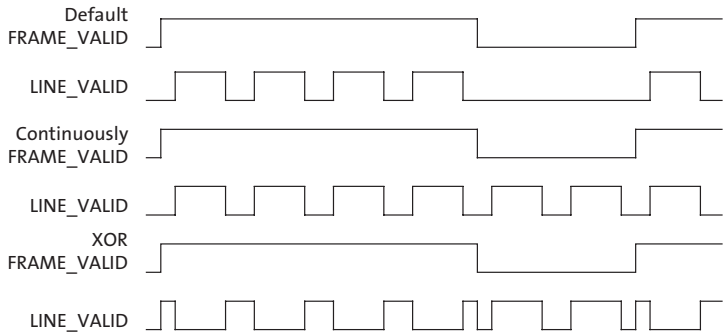
$$minimum\ vertical\ blanking\ requirement = 4 \quad (EQ\ 15)$$

Similar to progressive scan, FRAME_VALID is logic LOW during the valid image row only. Binning should not be used in conjunction with interlaced mode.

LINE_VALID

By setting bit 2 and 3 of R0x74 the LINE_VALID signal can get three different output formats. The formats for reading out four rows and two vertical blanking rows are shown in Figure 33. In the last format, the LINE_VALID signal is the XOR between the continuous LINE_VALID signal and the FRAME_VALID signal.

Figure 33: Different LINE_VALID Formats



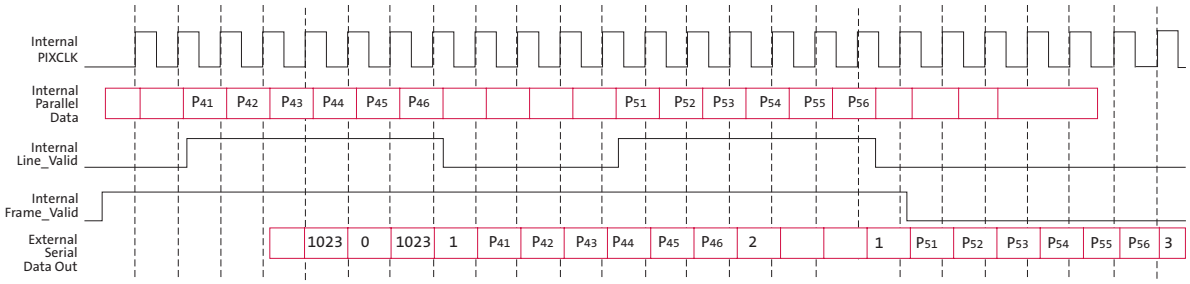
LVDS Serial (Stand-Alone/Stereo) Output

The LVDS interface allows for the streaming of sensor data serially to a standard off-the-shelf deserializer up to five meters away from the sensor. The pixels (and controls) are packeted—12-bit packets for stand-alone mode and 18-bit packets for stereoscopy mode. All serial signalling (CLK and data) is LVDS. The LVDS serial output could either be data from a single sensor (stand-alone) or stream-merged data from two sensors (self and its stereoscopic slave pair). The appendices describe in detail the topologies for both stand-alone and stereoscopic modes.

There are two standard deserializers that can be used. One for a stand-alone sensor stream and the other from a stereoscopic stream. The deserializer attached to a stand-alone sensor is able to reproduce the standard parallel output (8-bit pixel data, LINE_VALID, FRAME_VALID and PIXCLK). The deserializer attached to a stereoscopic sensor is able to reproduce 8-bit pixel data from each sensor (with embedded LINE_VALID and FRAME_VALID) and pixel-clk. An additional (simple) piece of logic is required to extract LINE_VALID and FRAME_VALID from the 8-bit pixel data. Irrespective of the mode (stereoscopy/stand-alone), LINE_VALID and FRAME_VALID are always embedded in the pixel data.

In stereoscopic mode, the two sensors run in lock-step, implying all state machines are in the same state at any given time. This is ensured by the sensor-pair getting their sys-clks and sys-resets in the same instance. Configuration writes through the two-wire serial interface are done in such a way that both sensors can get their configuration updates at once. The inter-sensor serial link is designed in such a way that once the slave PLL locks and the data-dly, shft-clk-dly and stream-latency-sel are configured, the master sensor streams good stereo content irrespective of any variation voltage and/or temperature as long as it is within specification. The configuration values of data-dly, shft-clk-dly and stream-latency-sel are either predetermined from the board-layout or can be empirically determined by reading back the stereo-error flag. This flag gets asserted when the two sensor streams are not in sync when merged. The combo_reg is used for out-of-sync diagnosis.

Figure 34: Serial Output Format for a 6x2 Frame



Notes:
1. External pixel values of 0, 1, 2, 3, are reserved (they only convey control information). Any raw pixel of value 0, 1, 2 and 3 will be substituted with 4.
2. The external pixel sequence 1023, 0 1023 is a reserved sequence (conveys control information). Any raw pixel sequence of 1023, 0, 1023 will be substituted with 1023, 4, 1023.

LVDS Output Format

In stand-alone mode, the packet size is 12 bits (2 frame bits and 10 payload bits); 10-bit pixels or 8-bit pixels can be selected. In 8-bit pixel mode (R0xB6[0] = 0), the packet consists of a start bit, 8-bit pixel data (with sync codes), the line valid bit, the frame valid bit and the stop bit. For 10-bit pixel mode (R0xB6[0] = 1), the packet consists of a start bit, 10-bit pixel data, and the stop bit.

Table 7: LVDS Packet Format in Stand-Alone Mode
(Stereoscopy Mode Bit De-Asserted)

12-Bit Packet	use_10-bit_pixels Bit De-Asserted (8-Bit Mode)	use_10-bit_pixels Bit Asserted (10-Bit Mode)
Bit[0]	1'b1 (Start bit)	1'b1 (Start bit)
Bit[1]	PixelData[2]	PixelData[0]
Bit2]	PixelData[3]	PixelData[1]
Bit[3]	PixelData[4]	PixelData[2]
Bit4]	PixelData[5]	PixelData[3]
Bit[5]	PixelData[6]	PixelData[4]
Bit[6]	PixelData[7]	PixelData[5]
Bit[7]	PixelData[8]	PixelData[6]
Bit[8]	PixelData[9]	PixelData[7]
Bit[9]	Line_Valid	PixelData[8]
Bit[10]	Frame_Valid	PixelData[9]
Bit[11]	1'b0 (Stop bit)	1'b0 (Stop bit)

In stereoscopic mode (see Figure 47 on page 50), the packet size is 18 bits (2 frame bits and 16 payload bits). The packet consists of a start bit, the master pixel byte (with sync codes), the slave byte (with sync codes), and the stop bit.)

Table 8: LVDS Packet Format in Stereoscopy Mode (Stereoscopy Mode Bit Asserted)

18-bit Packet	Function
Bit[0]	1'b1 (Start bit)
Bit[1]	MasterSensorPixelData[2]
Bit[2]	MasterSensorPixelData[3]
Bit[3]	MasterSensorPixelData[4]
Bit[4]	MasterSensorPixelData[5]
Bit[5]	MasterSensorPixelData[6]
Bit[6]	MasterSensorPixelData[7]
Bit[7]	MasterSensorPixelData[8]
Bit[8]	MasterSensorPixelData[9]
Bit[9]	SlaveSensorPixelData[2]
Bit[10]	SlaveSensorPixelData[3]
Bit[11]	SlaveSensorPixelData[4]
Bit[12]	SlaveSensorPixelData[5]
Bit[13]	SlaveSensorPixelData[6]
Bit[14]	SlaveSensorPixelData[7]
Bit[15]	SlaveSensorPixelData[8]
Bit[16]	SlaveSensorPixelData[9]
Bit[17]	1'b0 (Stop bit)

Control signals LINE_VALID and FRAME_VALID can be reconstructed from their respective preceding and succeeding flags that are always embedded within the pixel data in the form of reserved words.

Table 9: Reserved Words in the Pixel Data Stream

Pixel Data Reserved Word	Flag
0	Precedes frame valid assertion
1	Precedes line valid assertion
2	Succeeds line valid de-assertion
3	Succeeds frame valid de-assertion

When LVDS mode is enabled along with column binning (bin 2 or bin 4, R0x0D[3:2], the packet size remains the same but the serial pixel data stream repeats itself depending on whether 2X or 4X binning is set:

- For bin 2, LVDS outputs double the expected data (pixel 0,0 is output twice in sequence, followed by pixel 0,1 twice, . . .).
- For bin 4, LVDS outputs 4 times the expected data (pixel 0,0 is output 4 times in sequence followed by pixel 0,1 times 4, . . .).

The receiving hardware will need to undersample the output stream getting data either every 2 clocks (bin 2) or every 4 (bin 4) clocks.

If the sensor provides a pixel whose value is 0,1, 2, or 3 (that is, the same as a reserved word) then the outgoing serial pixel value is switched to 4.

Electrical Specifications

Table 10: DC Electrical Characteristics
V_{PWR} = 3.3V ±0.3V; T_A = Ambient = 25°C

Symbol	Definition	Condition	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage		V_{PWR} - 0.5	–	V_{PWR} + 0.3	V
V_{IL}	Input low voltage		–0.3	–	0.8	V
I_{IN}	Input leakage current	No pull-up resistor; V_{IN} = V_{PWR} or V_{GND}	–15.0	–	15.0	µA
V_{OH}	Output high voltage	I_{OH} = –4.0mA	V_{PWR} -0.7	–	–	V
V_{OL}	Output low voltage	I_{OL} = 4.0mA	–	–	0.3	V
I_{OH}	Output high current	V_{OH} = V_{DD} - 0.7	–9.0	–	–	mA
I_{OL}	Output low current	V_{OL} = 0.7	–	–	9.0	mA
V_{AA}	Analog power supply	Default settings	3.0	3.3	3.6	V
I_{PWRA}	Analog supply current	Default settings	–	35.0	60.0	mA
V_{DD}	Digital power supply	Default settings	3.0	3.3	3.6	V
I_{PWRD}	Digital supply current	Default settings, C_{LOAD} = 10pF	–	35.0	60	mA
VAAPIX	Pixel array power supply	Default settings	3.0	3.3	3.6	V
I_{PIX}	Pixel supply current	Default settings	0.5	1.4	3.0	mA
V_{LVDS}	LVDS power supply	Default settings	3.0	3.3	3.6	V
I_{LVDS}	LVDS supply current	Default settings	11.0	13.0	15.0	mA
I_{PWRA} Standby	Analog standby supply current	STDBY = V_{DD}	2	3	4	µA
I_{PWRD} Standby Clock Off	Digital standby supply current with clock off	STDBY = V_{DD}, CLKIN = 0 MHz	1	2	4	µA
I_{PWRD} Standby Clock On	Digital standby supply current with clock on	STDBY= V_{DD}, CLKIN = 27 MHz	–	1.05	–	mA
LVDS Driver DC Specifications						
|V_{OD}|	Output differential voltage	R_{LOAD} = 100 Ω ± 1%	250	–	400	mV
|DV_{OD}|	Change in V_{OD} between complementary output states		–	–	50	mV
V_{OS}	Output offset voltage		1.0	1.2	1.4	mV
DV_{OS}	Change in V_{OS} between complementary output states		–	–	35	mV
I_{OS}	Output current when driver shorted to ground			±10	±12	mA
I_{OZ}	Output current when driver is tri-state			±1	±10	µA
LVDS Receiver DC Specifications						
V_{IDTH+}	Input differential	| V_{GPD}| < 925mV	–100	–	100	mV
Iin	Input current		–	–	±20	µA

Table 11: Absolute Maximum Ratings

Caution Stresses greater than those listed may cause permanent damage to the device.

Symbol	Parameter	Minimum	Maximum	Unit
V_{SUPPLY}	Power supply voltage (all supplies)	–0.3	4.5	V
I_{SUPPLY}	Total power supply current	–	200	mA
I_{GND}	Total ground current	–	200	mA
V_{IN}	DC input voltage	–0.3	V_{DD} + 0.3	V
V_{OUT}	DC output voltage	–0.3	V_{DD} + 0.3	V
T_{STG}[1]	Storage temperature	–40	+125	°C

Notes: 1. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 12: AC Electrical Characteristics

V_{PWR} = 3.3V ±0.3V; T_A = Ambient = 25°C; Output Load = 10pF

Symbol	Definition	Condition	Minimum	Typical	Maximum	Unit
SYSCLK	Input clock frequency	Note 1	13.0	26.6	27.0	MHz
	Clock duty cycle		45.0	50.0	55.0	%
t_R	Input clock rise time		1	2	5	ns
t_F	Input clock fall time		1	2	5	ns
t_{PLHP}	SYSCLK to PIXCLK propagation delay	C_{LOAD} = 10pF	3	7	11	ns
t_{PD}	PIXCLK to valid D_{OUT}(9:0) propagation delay	C_{LOAD} = 10pF	–2	0	2	ns
t_{SD}	Data setup time		14	16	–	ns
t_{HD}	Data hold time		14	16	–	
t_{PFLR}	PIXCLK to LINE_VALID propagation delay	C_{LOAD} = 10pF	–2	0	2	ns
t_{PFLF}	PIXCLK to FRAME_VALID propagation delay	C_{LOAD} = 10pF	–2	0	2	ns

Notes: 1. The frequency range specified applies only to the parallel output mode of operation.

Propagation Delays for PIXCLK and Data Out Signals

The pixel clock is inverted and delayed relative to the master clock. The relative delay from the master clock (SYSCLK) rising edge to both the pixel clock (PIXCLK) falling edge and the data output transition is typically 7ns. Note that the falling edge of the pixel clock occurs at approximately the same time as the data output transitions. See Table 12 for data setup and hold times.

Propagation Delays for FRAME_VALID and LINE_VALID Signals

The LINE_VALID and FRAME_VALID signals change on the same rising master clock edge as the data output. The LINE_VALID goes HIGH on the same rising master clock edge as the output of the first valid pixel's data and returns LOW on the same master clock rising edge as the end of the output of the last valid pixel's data.

As shown in the "Output Data Timing" on page 13, FRAME_VALID goes HIGH 143 pixel clocks before the first LINE_VALID goes HIGH. It returns LOW 23 pixel clocks after the last LINE_VALID goes LOW.

Figure 35: Propagation Delays for PIXCLK and Data Out Signals

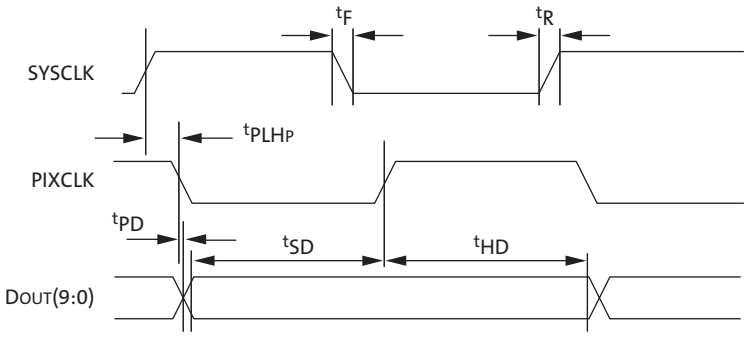
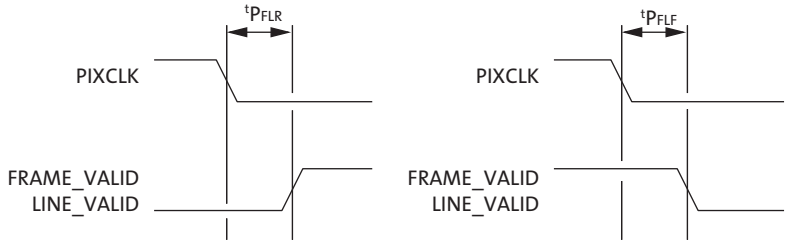


Figure 36: Propagation Delays for FRAME_VALID and LINE_VALID Signals



Performance Specifications

Table 13 summarizes the specification for each performance parameter.

Table 13: Performance Specifications

Parameter	Unit	Minimum	Typical	Maximum	Test Number
Sensitivity	LSB	400	572	745	1
DSNU	LSB	N/A	2.3	7.0	2
PRNU	%	N/A	1.3	4.0	3
Dynamic Range	dB	52.0	54.4	N/A	4
SNR	dB	33.0	37.3	N/A	5

Notes: 1. All specifications address operation is at T_A = 25°C (±3°C) and supply voltage = 3.3V. Image sensor was tested without a lens. Multiple images were captured and analyzed.
Setup: VDD = VAA = VAAPIX = LVDSVDD = 3.3V. Testing was done with default frame timing and default register settings, with the exception of AEC/AGC, row noise correction, and auto black level, which were disabled.

Performance definitions are detailed in the following sections.

Test 1: Sensitivity

A flat-field light source (90 lux, color temperature 4400K, broadband, w/ IR cut filter) is used as an illumination source. Signals are measured in LSB on the sensor output. A series of four frames are captured and averaged to obtain a scalar sensitivity output code.

Test 2: Dark Signal Non-Uniformity (DSNU)

The image sensor is held in the dark. Analog gain is changed to the maximum setting of 4X. Signals are measured in LSB on the sensor output. A series of four frames are captured and averaged (pixel-by-pixel) into one average frame. DSNU is calculated as the standard deviation of this average frame.

Test 3: Photo Response Non-Uniformity (PRNU)

A flat-field light source (90 lux, color temperature 4400K, broadband, with IR cut filter) is used as an illumination source. Signals are measured in LSB on the sensor output. Two series of four frames are captured and averaged (pixel-by-pixel) into one average frame, one series is captured under illuminated conditions, and one is captured in the dark. PRNU is expressed as a percentage relating the standard deviation of the average frames difference (illuminated frame - dark frame) to the average illumination level:

$$PRNU = 100 \times \frac{\sqrt{\frac{1}{N_p}\sum_{i=1}^{N_p}\left(S_{illumination}(i) - S_{dark}(i)\right)^2}}{\frac{1}{N_p}\sum_{i=1}^{N_p}\left(S_{illumination}(i)\right)} \quad \text{(EQ 16)}$$

where $S_{illumination}(i)$ is the signal measured for the i-th pixel from the average illuminated frame, $S_{dark}(i)$ is the signal measured for the i-th pixel from the average dark frame, and N_p is the total number of pixels contained in the array.

Test 4: Dynamic Range

A temporal noise measurement is made with the image sensor in the dark and analog gain changed to the maximum setting of 4X. Signals are measured in LSB on the sensor output. Two consecutive dark frames are captured. Temporal noise is calculated as the average pixel value of the difference frame:

$$\sigma_i = \sqrt{\frac{\sum_{i=1}^{N_p} (S_{1i} - S_{2i})^2}{2 \cdot N_p}} \quad \text{(EQ 17)}$$

Where S_{1i} is the signal measured for the i-th pixel from the first frame, S_{2i} is the signal measured for the i-th pixel from the second frame, and N_p is the total number of pixels contained in the array.

The dynamic range is calculated according to the following formula:

$$DynamicRange = 20 \cdot \log\left[\frac{4 \times 1022}{\sigma_t}\right] \quad \text{(EQ 18)}$$

Where σ_t is the temporal noise measured in the dark at 4X gain.

Test 5: Signal-to-Noise Ratio

A flat-field light source (90 lux, color temperature 4400K, broadband, with IR cut filter) is used as an illumination source. Signals are measured in LSB on the sensor output. Two consecutive illuminated frames are captured. Temporal noise is calculated as the average pixel value of the difference frame (according to the formula shown in Test 4). The signal-to-noise ratio is calculated as the ratio of the average signal level to the temporal noise according to the following formula:

$$Signal-to-Noise-Ratio = 20 \cdot \log\left[\frac{\left(\left(\sum_{i=1}^{N_p} S_{1i}\right) / N_p\right)}{\sigma_t}\right] \quad \text{(EQ 19)}$$

Where σ_t is the temporal noise measured from the illuminated frames, S_{1i} is the signal measured for the i-th pixel from the first frame, and N_p is the total number of pixels contained in the array.

Two-Wire Serial Bus Timing

The two-wire serial bus operation requires certain minimum master clock cycles between transitions. These are specified in the following diagrams in master clock cycles.

Figure 37: Serial Host Interface Start Condition Timing

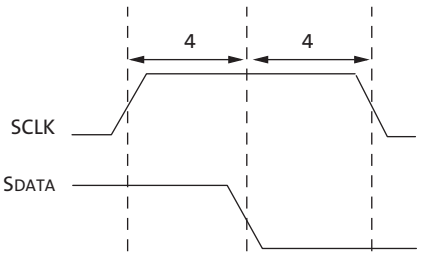
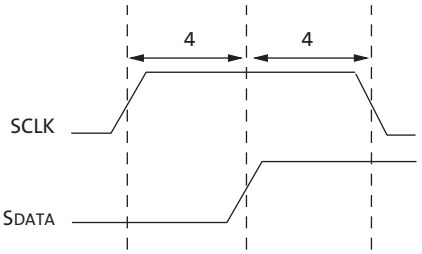
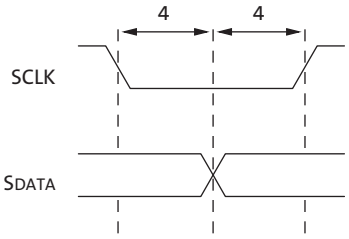


Figure 38: Serial Host Interface Stop Condition Timing



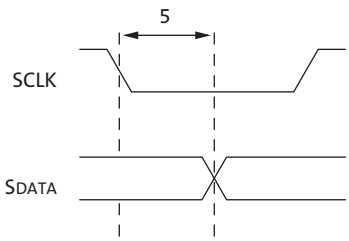
Notes: 1. All timing are in units of master clock cycle.

Figure 39: Serial Host Interface Data Timing for Write



Notes: 1. SDATA is driven by an off-chip transmitter.

Figure 40: Serial Host Interface Data Timing for Read



Notes: 1. SDATA is pulled LOW by the sensor, or allowed to be pulled HIGH by a pull-up resistor off-chip.

Figure 41: Acknowledge Signal Timing After an 8-Bit WRITE to the Sensor

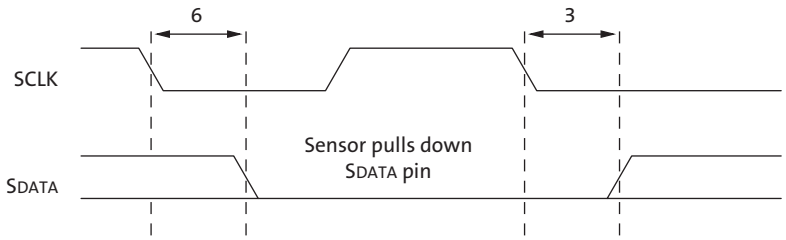
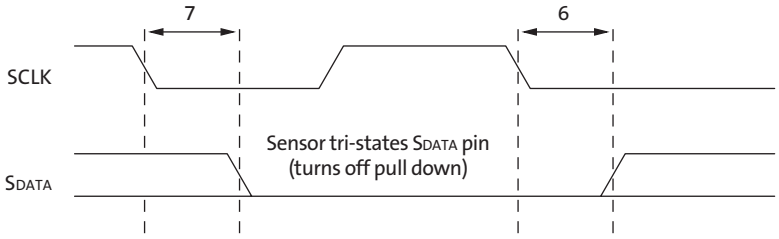


Figure 42: Acknowledge Signal Timing After an 8-Bit READ from the Sensor



Note: After a READ, the master receiver must pull down SDATA to acknowledge receipt of data bits. When read sequence is complete, the master must generate a "No Acknowledge" by leaving SDATA to float HIGH. On the following cycle, a start or stop bit may be used.

Temperature Reference

The MT9V022 contains a temperature reference circuit that can be used to measure relative temperatures. Contact your Aptina field applications engineer (FAE) for more information on using this circuit.

Figure 43: Typical Quantum Efficiency—Color

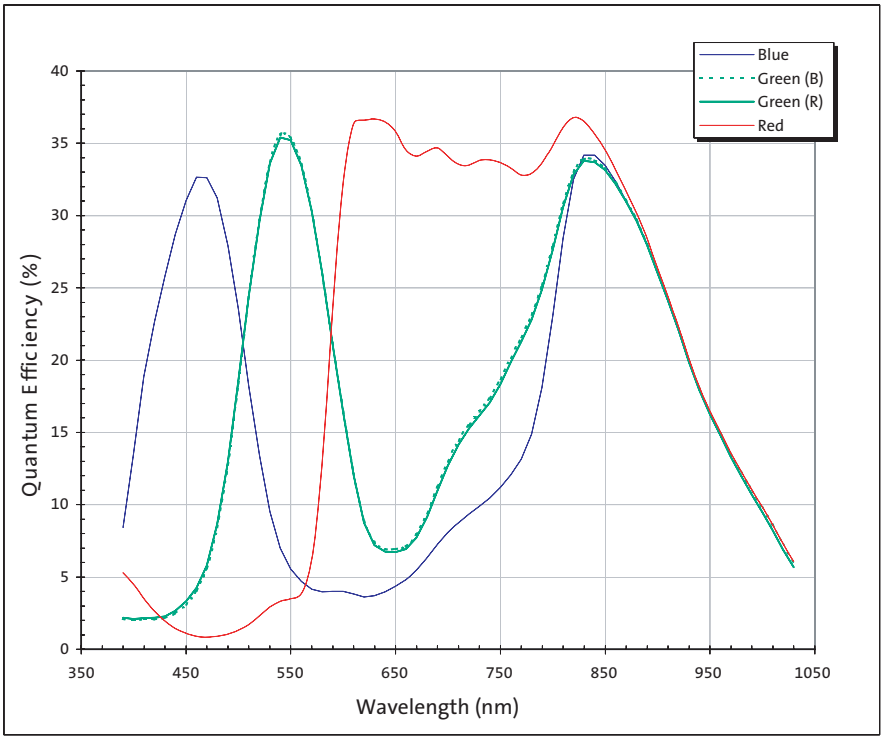
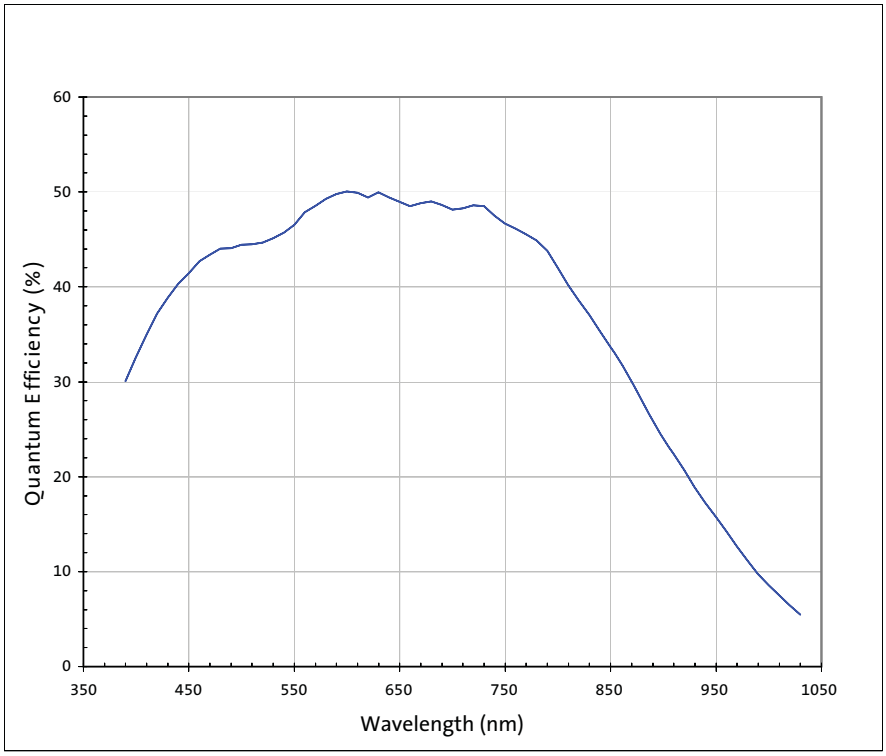
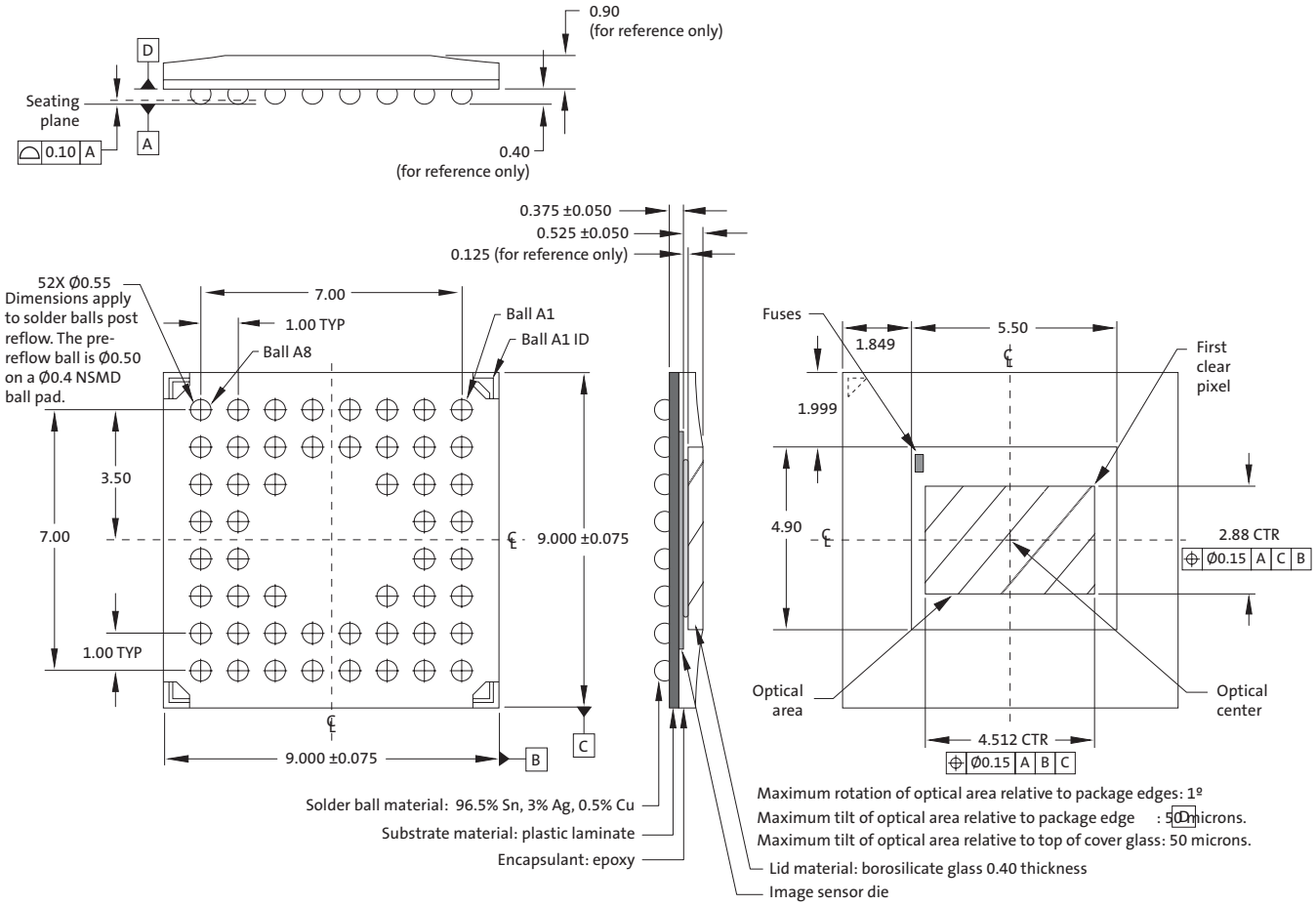


Figure 44: Typical Quantum Efficiency—Monochrome



Package Dimensions

Figure 45: 52-Ball IBGA



Notes: 1. All dimensions in millimeters.

Appendix A – Serial Configurations

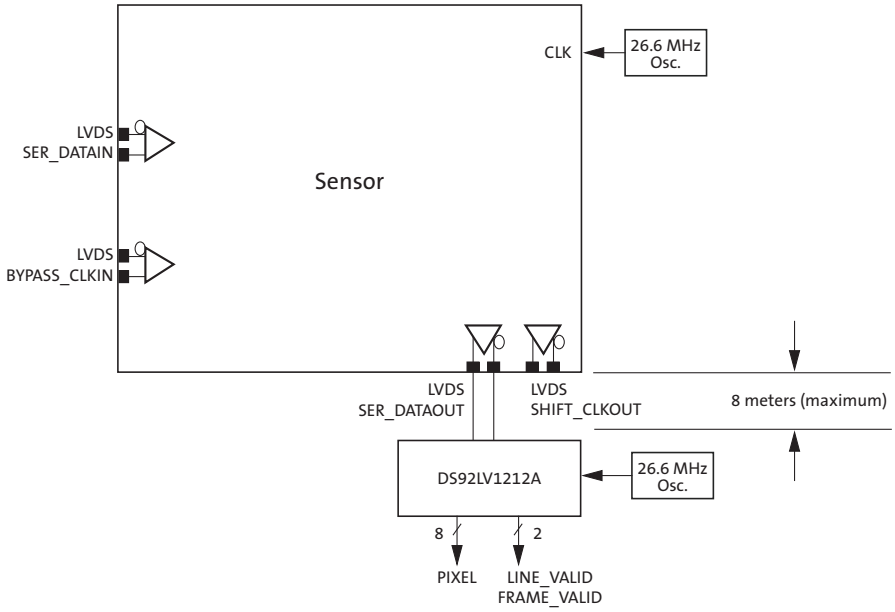
With the LVDS serial video output, the deserializer can be up to 8 meters from the sensor. The serial link can save on the cabling cost of 14 wires (DOUT[9:0], LINE_VALID, FRAME_VALID, PIXCLK, GND). Instead, just 3 wires (2 serial LVDS, 1 GND) are sufficient to carry the video signal.

Configuration of Sensor for Stand-Alone Serial Output with Internal PLL

In this configuration, the internal PLL generates the shift-clk (x12). The LVDS pins SER_DATAOUT_P and SER_DATAOUT_N must be connected to a deserializer (clocked at approximately the same system clock frequency).

Figure 46 shows how a standard off-the-shelf deserializer (National Semiconductor DS92LV1212A) can be used to retrieve the standard parallel video signals of DOUT(9:0), LINE_VALID and FRAME_VALID.

Figure 46: Stand-Alone Topology



8-bit configuration shown

Typical configuration of the sensor:

1. Power-up sensor.
2. Enable LVDS driver (set R0xB3[4]= 0).
3. De-assert LVDS power-down (set R0xB1[1] = 0.
4. Issue a soft reset (set R0x0C[0] = 1 followed by R0x0C[0] = 0.

If necessary:

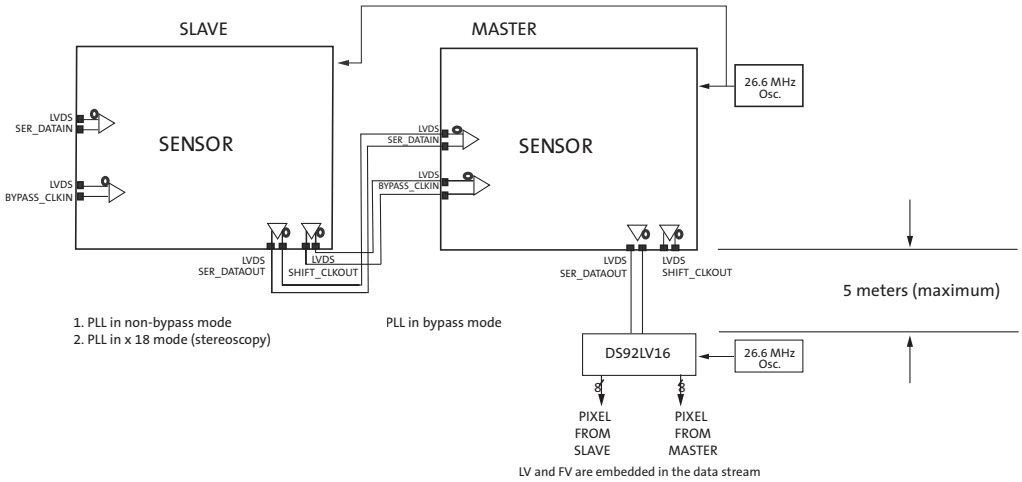
5. Force sync patterns for the deserializer to lock (set R0xB5[0] = 1).
6. Stop applying sync patterns (set R0xB5[0] = 0).

Configuration of Sensor for Stereoscopic Serial Output with Internal PLL

In this configuration the internal PLL generates the shift-clk (x18) in phase with the system-clock. The LVDS pins SER_DATAOUT_P and SER_DATAOUT_N must be connected to a deserializer (clocked at approximately the same system clock frequency).

Figure 47 shows how a standard off-the-shelf deserializer can be used to retrieve back DOUT(9:2) for both the master and slave sensors. Additional logic is required to extract out LINE_VALID and FRAME_VALID embedded within the pixel data stream.

Figure 47: Stereoscopic Topology



Typical configuration of the master and slave sensors:

1. Power up the sensors.
2. Broadcast WRITE to de-assert LVDS power-down (set R0xB1[1] = 0).
3. Individual WRITE to master sensor putting its internal PLL into bypass mode (set R0xB1[0] = 1).
4. Broadcast WRITE to both sensors to set the stereoscopy bit (set R0x07[5] = 1).
5. Make sure all resolution, vertical blanking, horizontal blanking, window size, and AEC/AGC configurations are done through broadcast WRITE to maintain lockstep.
6. Broadcast WRITE to enable LVDS driver (set R0xB3[4] = 0).
7. Broadcast WRITE to enable LVDS receiver (set R0xB2[4] = 0).
8. Individual WRITE to master sensor, putting its internal PLL into bypass mode (set R0xB1[0] = 1).
9. Individual WRITE to slave sensor, enabling its internal PLL (set R0xB1[0] = 0).
10. Individual WRITE to slave sensor, setting it as a stereo slave (set R0x07[6] = 1).
11. Individual WRITEs to master sensor to minimize the inter-sensor skew (set R0xB2[2:0], R0xB3[2:0], and R0xB4[1:0] appropriately). Use R0xB7 and R0xB8 to get lockstep feedback from stereo_error_flag.
12. Broadcast WRITE to issue a soft reset (set R0x0C[0] = 1 followed by R0x0C[0] = 0).

Note: The stereo_error_flag is set if a mismatch has occurred at a reserved byte (slave and master sensor's codes at this reserved byte must match). If the flag is set, steps 11 and 12 are repeated until the stereo_error_flag remains cleared.

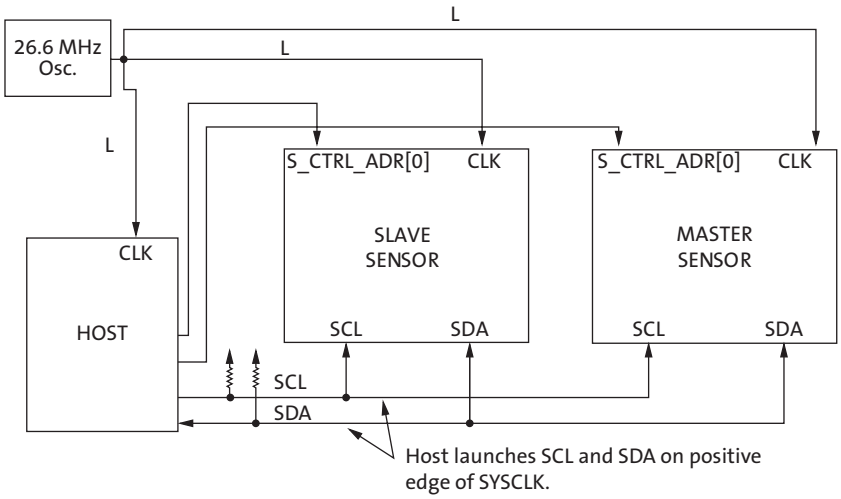
Broadcast and Individual Writes for Stereoscopic Topology

In stereoscopic mode, the two sensors are required to run in lockstep. This implies that control logic in each sensor is in exactly the same state as its pair on every clock. To ensure this, all inputs that affect control logic must be identical and arrive at the same time at each sensor.

These inputs include:

- system clock
- system reset
- two-wire serial interface clk - SCL
- two-wire serial interface data - SDA

Figure 48: Two-Wire Serial Interface Configuration in Stereoscopic Mode



All system clock lengths (L) must be equal.
SCL and SDA lengths to each sensor (from the host) must also be equal.

The setup in Figure 48 shows how the two sensors can maintain lockstep when their configuration registers are written through the two-wire serial interface. A WRITE to configuration registers would either be broadcast (simultaneous WRITES to both sensors) or individual (WRITE to just one sensor at a time). READs from configuration registers would be individual (READs from just one sensor at a time).

One of the two serial interface slave address bits of the sensor is hardwired. The other is controlled by the host. This allows the host to perform either a broadcast or a one-to-one access.

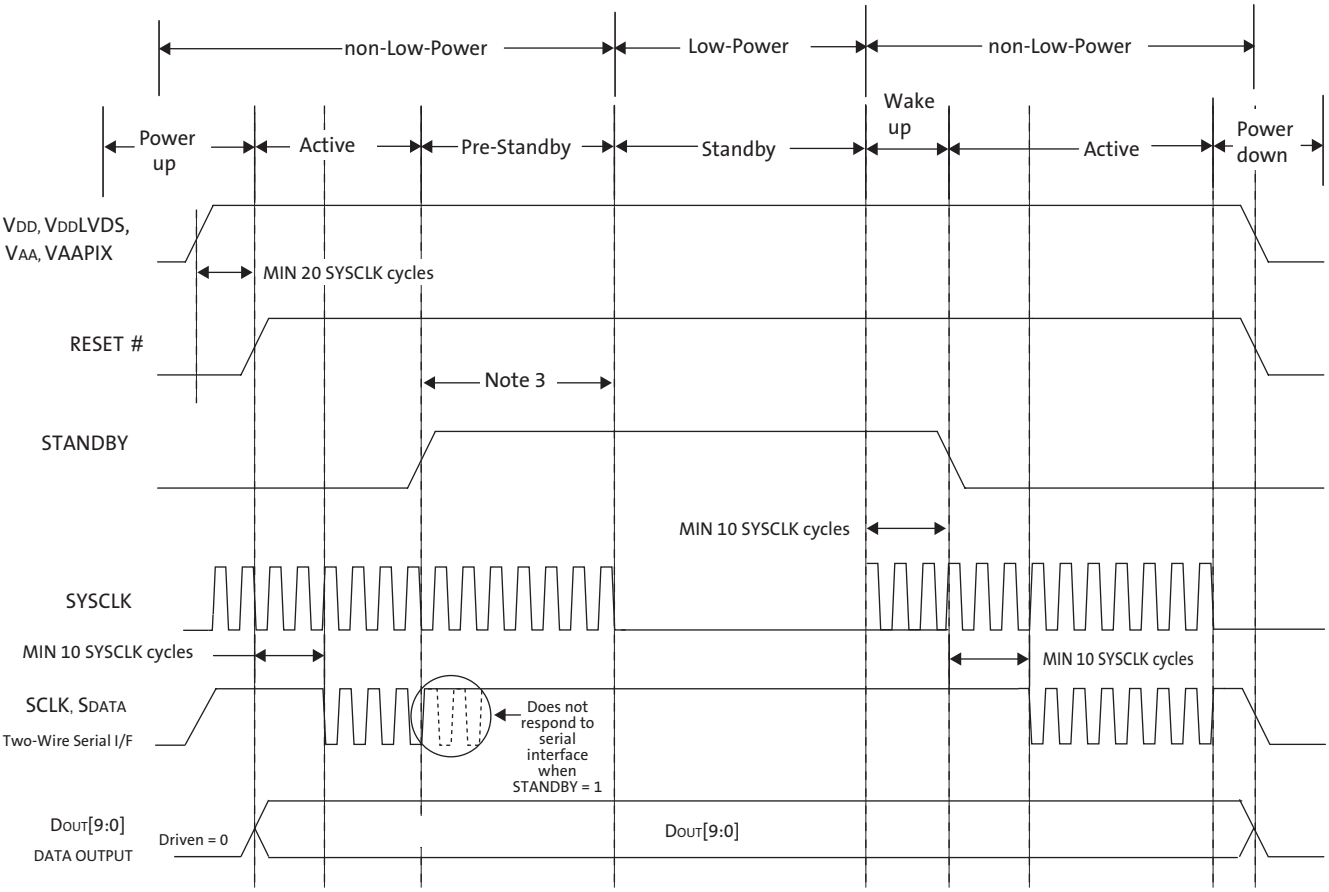
Broadcast WRITES are performed by setting the same S_CTRL_ADR input bit for both slave and master sensor. Individual WRITES are performed by setting opposite S_CTRL_ADR input bit for both slave and master sensor. Similarly, individual READs are performed by setting opposite S_CTRL_ADR input bit for both slave and master sensor.

Appendix B – Power-On Reset and Standby Timing

Reset, Clocks, and Standby

There are no constraints concerning the order in which the various power supplies are applied; however, the MT9V022 requires reset in order operate properly at power-up. Refer to Figure 49 for the power-up, reset, and standby sequences.

Figure 49: Power-up, Reset, Clock and Standby Sequence



Notes:
1. All output signals are defined during initial power-up with RESET# held LOW without SYSCLK being active. To properly reset the rest of the sensor, during initial power-up, assert RESET# (set to LOW state) for at least 750ns after all power supplies have stabilized and SYSCLK is active (being clocked). Driving RESET# to LOW state does not put the part in a low power state.
2. Before using two-wire serial interface, wait for 10 SYSCLK rising edges after RESET# is de-asserted.
3. Once the sensor detects that STANDBY has been asserted, it completes the current frame readout before entering standby mode. The user must supply enough SYSCLKs to allow a complete frame readout. See Table 4, "Frame Time," on page 13 for more information.
4. In standby, all video data and synchronization output signals are High-Z.
5. In standby, the two-wire serial interface is not active.

Standby Assertion Restrictions

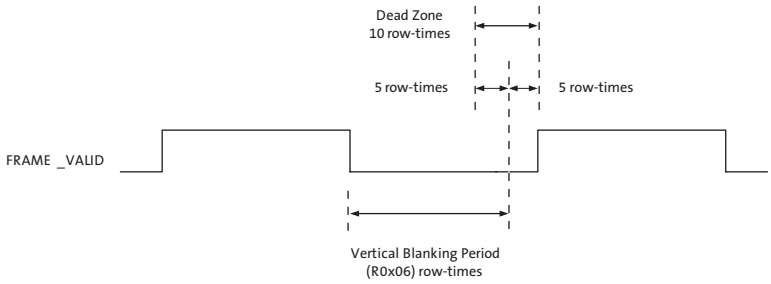
STANDBY cannot be asserted at any time. If STANDBY is asserted during a specific window within the vertical blanking period, the MT9V022 may enter a permanent standby state. This window (that is, dead zone) occurs prior to the beginning of the new frame readout. The permanent standby state is identified by the absence of the FRAME_VALID signal on frame readouts. Issuing a hardware reset (RESET# set to LOW state) will return the image sensor to default startup conditions.

This dead zone can be avoided by:

1. Asserting STANDBY during the valid frame readout time (FRAME_VALID is HIGH) and maintaining STANDBY assertion for a minimum of one frame period.
2. Asserting STANDBY at the end of valid frame readout (falling edge of FRAME_VALID) and maintaining STANDBY assertion for a minimum of [5 + R0x06] row-times.

When STANDBY is asserted during the vertical blanking period (FRAME_VALID is LOW), the STANDBY signal must not change state between [Vertical Blanking Register (R0x06) - 5] row-times and [Vertical Blanking Register + 5] row-times after the falling edge of FRAME_VALID.

Figure 50: STANDBY Restricted Location



Revision History

Rev. H 6/10

- Updated to non-confidential

Rev. G 5/10

- Updated to Aptina template

Rev. F 12/06

- Changed description text in Table 3 on page 8, row H5, to "Error detected. Directly connected to STEREO ERROR FLAG."
- Changed text in “Automatic Black Level Calibration” on page 11
- Changed “writing (or reading) the least significant 8 bits to R0x80 (128)” on page 15 to “writing (or reading) the least significant 8 bits to R0xF0 (240)”
- Changed “the special register address (R0xF1)” on page 18 to “the special register address (R0xF0)”
- Changed wording in Table 7 on page 15 row 0x00, on page 23 row 0xFF, and in Table 8 on page 19 row 0x00/0xFF from “Rev1,” etc. to “Iter1”, etc.
- Updated legal values for R0x08, R0x09, R0x0B in Table 8 on page 19
- Updated Figure 24: “Latency of Analog Gain Change When AGC Is Disabled,” on page 28
- Changed signal name in Table 11 on page 41 in Maximum column, V_{IN} and V_{OUT} rows, from V_{DDQ} to V_{DD}
- Moved “Propagation Delays for PIXCLK and Data Out Signals” up to follow Table 12 on page 41
- Added section on “Performance Specifications” on page 43
- Updated Figure 45 “52-Ball IBGA” on page 48
- Updated Figure 46: “Stand-Alone Topology,” on page 49

Rev. E 5/06

- Added "Automatic Black Level Calibration" on page 11
- Updated Table 8, “Register Descriptions,” on page 19 (R0x73[9:0])
- Updated "Automatic Gain Control and Automatic Exposure Control" on page 32
- Updated "Row-wise Noise Correction" on page 31
- Updated Table 12, “AC Electrical Characteristics,” on page 41
- Updated "Appendix A – Serial Configurations" on page 49
- Updated "Configuration of Sensor for Stand-Alone Serial Output with Internal PLL" on page 49
- Updated Figure 46, Stand-Alone Topology, on page 49
- Updated "Configuration of Sensor for Stereoscopic Serial Output with Internal PLL" on page 50
- Updated Figure 47, Stereoscopic Topology, on page 50

Rev. D 12/05

- Added lead-free part numbers, page 1
- Added three notes to Table 3, “Ball Descriptions,” on page 8
- Updated Figure 3, Typical Configuration (Connection)—Parallel Output Mode, on page 9

- Updated Table 7, “Default Register Descriptions,” on page 15. Updated Registers 0x00, 0x0D, 0xF0, 0xF1 and 0xFF. Updated Registers 0x10, 0x15, 0x20 and 0xC2 with Rev 3 default values.
- Updated Table 8, “Register Descriptions,” on page 19
  0x00, 0xFF – Chip Version: added Rev 1, 2, and 3 values
  0x06 – Vertical Blank: minimum number is 4
  0x07 – Chip Control bit 5 - PLL generates 480 MHz clock
  0x0D – Added reserve bits [9:8]
  0x35 – Added calculation for lower and upper register ranges
  0xF0 – Bytewise Address register corrected
- Added "Simultaneous Master Mode" on page 20
- Added "Sequential Master Mode" on page 21
- Updated "Snapshot Mode" on page 21
- Updated "Slave Mode" on page 22
- Updated "Pixel Clock Speed" on page 32
- Added "Hard Reset of Logic" on page 33
- Updated Table 10, “DC Electrical Characteristics,” on page 40
- Added Table 11, “Absolute Maximum Ratings,” on page 41
- Updated Figure 35, Propagation Delays for PIXCLK and Data Out Signals, on page 42
- Updated "Appendix A – Serial Configurations" on page 49
- Updated Figure 46, Stand-Alone Topology, on page 49
- Updated Figure 47, Stereoscopic Topology, on page 50
- Added "Appendix B – Power-On Reset and Standby Timing" on page 52

Rev. C 9/05

- Several text changes
- Corrected steps in “Configuration of Sensor for Stereoscopic Serial Output with Internal PLL” on page 50

Rev. B 6/05

- Updated part number and header on each page
- Updated Table 1, “Key Performance Parameters,” on page 1 (Power Consumption).
- Updated Figure 1, Block Diagram, on page 6; Update “General Description” on page 6
- Updated Table 3, “Ball Descriptions,” on page 8
- Updated Table 7, “Default Register Descriptions,” on page 15 (0xBE - Reserved)
- Updated Table 8, “Register Descriptions,” on page 19 (R0x7F, R0x07[1:0], R0xB2[4], 0xB3[4], 0xBA, remove 0xBE)
- Updated “Pixel Integration Control” on page 24
- Updated Table 10, “DC Electrical Characteristics,” on page 40
- Updated Table 12, “AC Electrical Characteristics,” on page 41
- Replaced “Thermometer” section and figure with section titled “Temperature Reference” on page 46
- Added Figure 45, 52-Ball IBGA, on page 48

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Rev. A 2/05

- Initial release