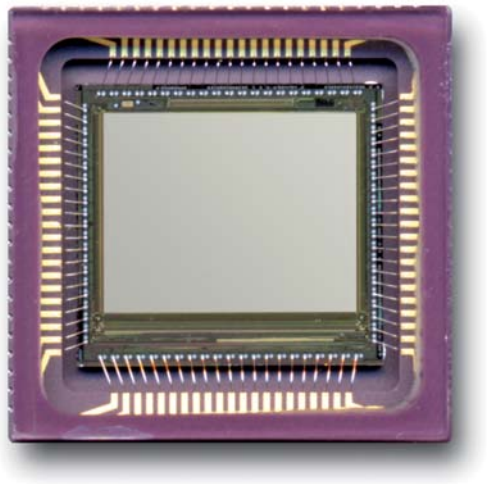
IBIS5-A-1300

1.3M Pixel
Dual Shutter Mode
CMOS Image Sensor



Datasheet

TABLE OF CONTENT

1 Introduction

Overview

The IBIS5-A-1300 is a solid state CMOS image sensor that integrates the functionality of complete analog image acquisition, digitizer and digital signal processing system on a single chip. This 1.3-mega pixel (1280 x 1024) CMOS active pixel sensor dedicated to industrial vision features both rolling and snapshot shutter. Full frame readout time is 36 ms (max. 27.5 fps), and readout speed can be boosted by windowed region of interest (ROI) readout. High dynamic range scenes can be captured using the double and multiples slope functionality. The sensor is available in a Monochrome version or Bayer (RGB) patterned color filter array.

User programmable row and column start/stop positions allow windowing down to 2x1 pixel window for digital zoom. Sub sampling reduces resolution while maintaining the constant field of view and an increased frame rate. The analog video output of the pixel array is processed by an on-chip analog signal pipeline. Double Sampling (DS) eliminates the fixed pattern noise. The programmable gain and offset amplifier maps the signal swing to the ADC input range. A 10-bit ADC converts the analog data to a 10-bit digital word stream. The sensor uses a 3-wire Serial-Parallel (SPI) interface or a 16-bit parallel interface. It operates with a 3.3V power supply and requires only one master clock for operation up to 40 MHz. It is housed in an 84-pin ceramic LCC package.

The IBIS5-A-1300 is designed taking into consideration interfacing requirements to standard video encoders. In addition to the 10-bit pixel data stream, the sensor outputs the valid frame, line and pixel sync signals needed for encoding.

This datasheet allows the user to develop a camera system based on the described timing and interfacing.

Key features

The main features of the image sensor are identified as:

- SXGA resolution: 1280 by 1024 pixels.
- 6.7 µm high fill factor square pixels (based on the high-fill factor active pixel sensor technology of FillFactory (US patent No. 6,225,670 and others)).
- Peak QE x FF of 30%.
- Optical format: 2/3" (8.6mm x 6.9mm).
- Pixel rate of 40 MHz using a 40 MHz system clock.
- Optical dynamic range: 64dB (1600:1) in single slope operation and 80…100dB in multiple slope operation.
- On-chip 10 bit, 40Msamples/s ADC.
- Programmable gain and offset output amplifier.
- Both rolling curtain shutter and synchronous shutter.
- Random programmable windowing and sub-sampling modes.
- Low fixed pattern noise (<0.5% RMS).
- On-chip timing and control logic sequencer.
- Processing is done in a CMOS 0.35 µm triple metal process.

Part number

Part number	Package	Monochrome/ color die	Glass lid
IBIS5-A-1300-M-1 CYII5SM1300AA-HBC (Preliminary)	84 pins JLCC package*	Monochrome	Monochrome**
IBIS5-A-1300-M-2 CYII5SM1300AA-QBC (Preliminary)	84 pins LCC package	Monochrome	Monochrome
IBIS5-A-1300-C-1 CYII5SC1300AA-HAC (Preliminary)	84 pins JLCC package	Color	Color***
IBIS5-A-1300-C-2 CYII5SC1300AA-QAC (Preliminary)	84 pins LCC package	Color	Color

* JLCC package for use in evaluation kits only.
** D263 is used as monochrome glass lid (see Figure 36 for spectral transmittance).
*** S8612 is used as color glass lid (see Figure 37 for spectral transmittance).
Other packaging combinations are available upon special request.

2 Specifications

2.1 Pixel characteristics

Table 1: Pixel characteristics

Parameter	Specification	Remarks
Pixel architecture	*4-transistor active pixel sensor*	Allows for both rolling and synchronous (snapshot) shutter.
Pixel size	*6.7 µm x 6.7 µm*	The resolution and pixel size results in a 2/3" optical format.
Resolution	*1280 x 1024*	
Pixel rate	*40 MHz*	Using a 40 MHz system clock.
Shutter types	*- Rolling* *- Snapshot*	- Continuous imaging. - Triggered synchronous shutter with integration and readout separate in time.
Full frame rate	*27.5 fps*	Depending on shutter type and integration time.

2.2 Electro-optical specifications

2.2.1 Overview

Table 2: Electro-optical specifications

Parameter	Specification	Remarks
FPN (on chip corrected)	*< 0.2% RMS*	Synchronous (snapshot) shutter. Rolling curtain shutter.
PRNU	*<10% p-p*	*2% RMS.*
Conversion gain	*17.6 uV/electron*	@ output.
Output signal amplitude	*1.1V* *1.8V*	Unity gain. Maximum output signal amplitude.
Saturation charge	*62.500 e-*	
Sensitivity	*592 V.m2/W.s*	Average white light.
	3.29 V/lux.s	Visible band only (180 lx = 1 W/m2).
	8.46 V/lux.s	Visible + NIR (70 lx = 1 W/m2).
Peak QE * FF Peak SR * FF	*>30%* *0.16 A/W*	Average QE*FF = 25-30%. Average SR*FF = 0.12 A/W. See spectral response curve.
Dark current *(@ RT)*	*7.22 mV/s* *or ~ 410 e-/s*	Auto saturation time in the order of 150s.
Noise electrons	*< 40 e-*	Synchronous shutter. Rolling curtain shutter.
S/N ratio	*1600:1 (64 dB)*	Synchronous shutter. Rolling curtain shutter.

Parameter	Specification	Remarks
Spectral sensitivity range	*400 – 1000 nm*	
Parasitic sensitivity	*< 1%*	I.e. sensitivity of the storage node during read out (after integration).
Optical cross talk	*8%*	Cross talk to the nearest neighbor.
Power dissipation	*175 mWatt*	Typical.

2.2.2 Spectral response curve

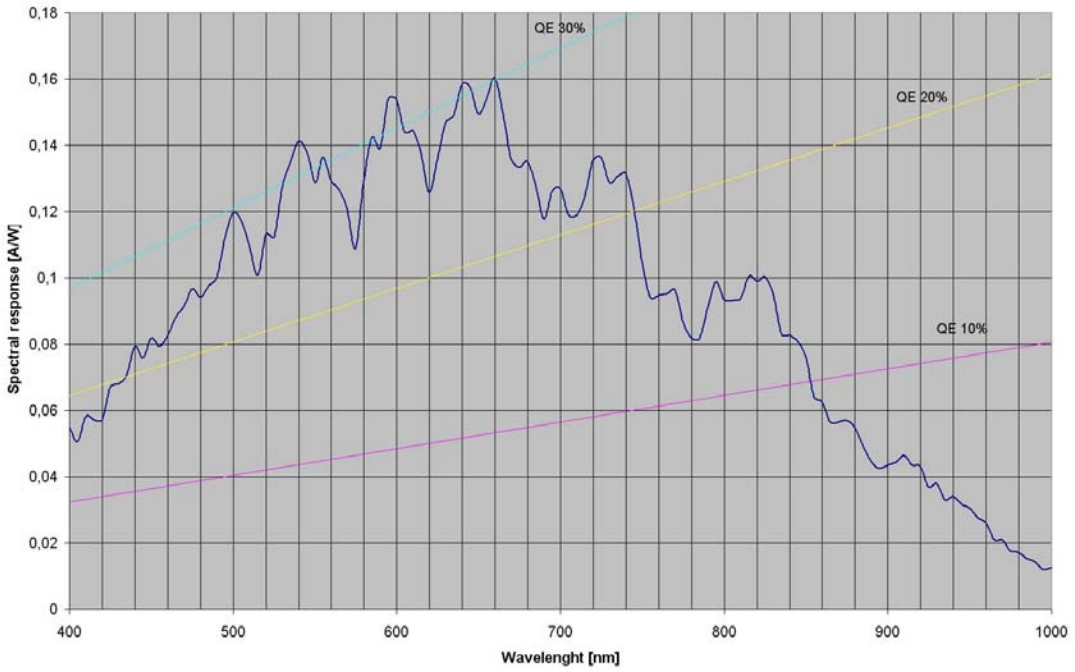


Figure 1: Spectral response curve

Figure 1 shows the spectral response characteristic. The curve is measured directly on the pixels. It includes effects of non-sensitive areas in the pixel, e.g. interconnection lines. The sensor is light sensitive between 400 and 1000 nm. The peak QE * FF is approximately 30% between 500 and 700 nm. In view of a fill factor of 50%, the QE is thus larger than 60% between 500 and 700 nm.

2.2.3 Photo-voltaic response curve

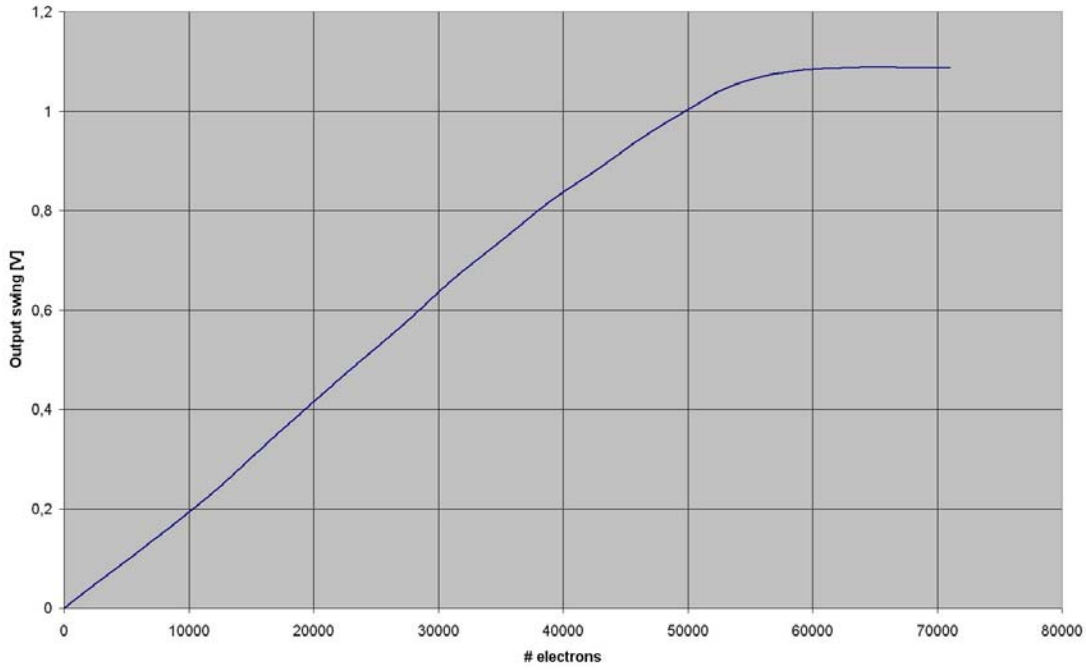


Figure 2: photo-voltaic response curve

Figure 2 shows the pixel response curve in linear response mode. This curve is the relation between the electrons detected in the pixel and the output signal. The voltage to electrons conversion gain of the pixel is 17.6 µV/electron.

2.3 Features and general specifications

Table 3: Features and general specifications

Feature	Specification/Description
Electronic shutter types	1. Rolling curtain shutter. 2. Synchronous (snapshot) shutter.
Windowing (ROI)	Implemented as scanning of lines/columns from an uploaded position.
Sub-sampling modes: • X-direction • Y-direction	1:2 sub-sampling. Sub-sampling patterns: a. XXOOXXOO (for Bayer pattern color filter) b. OOXXOOXX (for Bayer pattern color filter) c. XOXOXOXO d. OXOXOXOX Identical sub-sample patterns as X-direction.

Feature	Specification/Description
Extended dynamic range	In rolling shutter: Normal (1) or double (2) slope. In Synchronous shutter: 1, 2, 3 or 4 slopes.
Digital output	10 bit ADC @ 40 MSamples/s.
Programmable gain range	x1 to x12, in 16 steps of approx. 1.5 dB using 4-bits programming.
Programmable offset	128 steps (7 bit).
Supply voltage VDD	Image core supply: Range from 3.3 V to 4.5 V Analog supply: Nominal 3.3 V Digital: Nominal 3.3 V
Logic levels	3.3 V (Digital supply).
Operational temperature range	0°C to 60°C, with degradation of dark current.
Die size (with scribe lines)	10.1 mm by 9.3 mm (x by y).
Package	84 pins LCC.

2.4 Electrical specifications

2.4.1 Absolute maximum ratings

Table 4: Absolute maximum ratings

Symbol	Parameter	Value	Unit
VDD	DC supply voltage	-0.5 to 4.5	V
V_{IN}	DC input voltage	-0.5 to 3.8	V
V_{OUT}	DC output voltage	-0.5 to 3.8	V
I_{IO}	DC current drain per pin; any single input or output.	± 50	mA
T_L	Lead temperature (5 seconds soldering).	350	°C

- Absolute Ratings are those values beyond which damage to the device may occur.
- VDD = VDDD = VDDA (VDDD is supply to digital circuit, VDDA to analog circuit).

2.4.2 Recommended operating conditions

Table 5: Recommended operation conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDDH	Voltage on HOLD switches.	+3.3	+4.5	+4.5	V
VDDR_LEFT	Highest reset voltage.	+3.3	+4.5	+4.5	V
VDDC	Pixel core voltage.	+2.5	+3.0	+3.3	V
VDDA	Analog supply voltage of the image core.	+3.0	+3.3	+3.6	V
VDDD	Digital supply voltage of the image core.	+3.0	+3.3	+3.6	V

Symbol	Parameter	Min	Typ	Max	Unit
GNDA	Analog ground	-0.5	0	+0.5	V
GNDD	Digital ground	-0.5	0	+0.5	V
GND_AB	Anti-blooming ground.	-0.5	0	+0.5	V
T_A	Commercial operating temperature.	0	30	60	°C

- All parameters are characterized for DC conditions after thermal equilibrium has been established.
- Unused inputs must always be tied to an appropriate logic level, e.g. either VDD or GND.
- This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high impedance circuit.

2.4.3 DC electrical characteristics

Table 6: DC electrical characteristics

Symbol	Characteristic	Condition	Min	Max	Unit
V_{IH}	Input high voltage		2.1		V
V_{IL}	Input low voltage			0.6	V
I_{IN}	Input leakage current	V_{IN} = VDD or GND	-10	+10	µA
V_{OH}	Output high voltage	VDD=min; I_{OH}= -100mA	2.2		V
V_{OL}	Output low voltage	VDD=min; I_{OH}= 100mA		0.5	V
I_{DD}	Maximum operating current	System clock <= 40MHz	40	60	mA

3 Architecture and operation

In this part the most important blocks of the sensor are described in more detail.

3.1 Floor plan

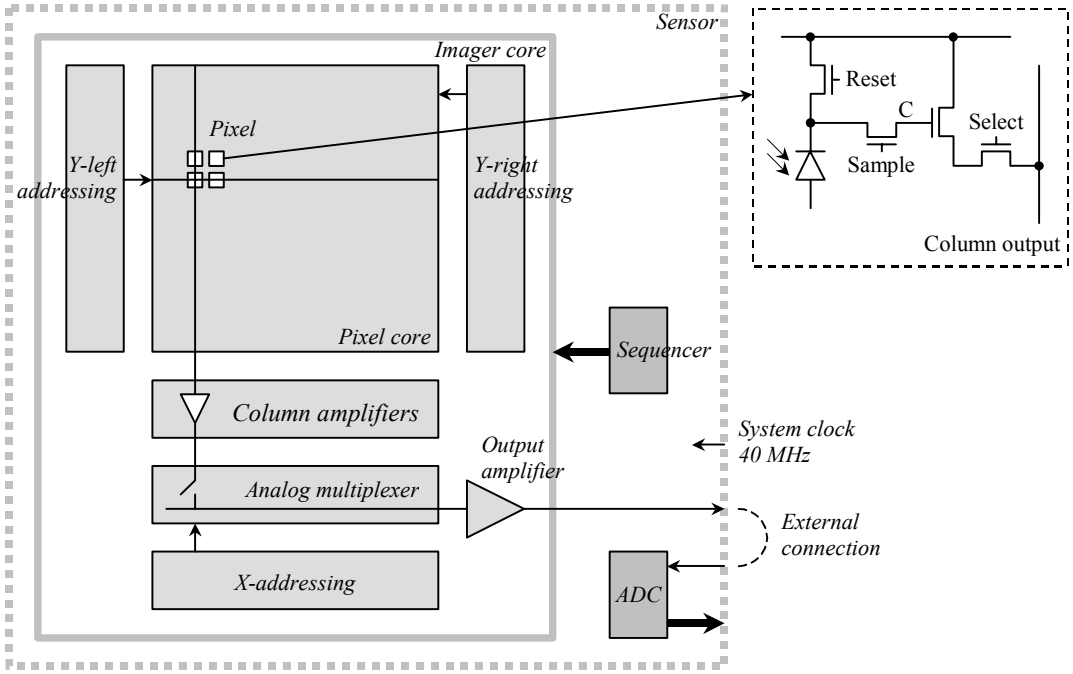


Figure 3: Block diagram of the IBIS5-A-1300 image sensor

Figure 3 shows the architecture of the IBIS5-A-1300 image sensor. It consists basically of a pixel array, one X- and two Y-addressing registers for the readout in X- and Y-direction, column amplifiers that correct for the fixed pattern noise, an analog multiplexer and an analog output amplifier.

The left Y-addressing register is used for readout operation. The right Y-addressing register is used for reset of pixel row(s):

- In multiple slope synchronous shutter mode, the right Y-addressing register resets the whole pixel core with a lowered reset voltage.
- In rolling curtain shutter mode, the right Y-addressing register is used for the reset pointer in single and double slope operation to reset 1 pixel row.

Most of the signals for the image core are generated by the on-chip sequencer. Some basic signals (like start/stop integration, line and frame sync signals, etc…) have to be generated externally.

A 10-bit ADC is implemented on chip but electrically isolated from the image core. The analog pixel output has to be routed to the analog ADC input on the outside.

3.2 Pixel

3.2.1 Architecture

The pixel architecture used in the IBIS5-A-1300 is a 4-transistor pixel as shown in Figure 4. The pixel has been implemented using the high fill factor technique as patented by FillFactory (US patent No. 6,225,670 and others).

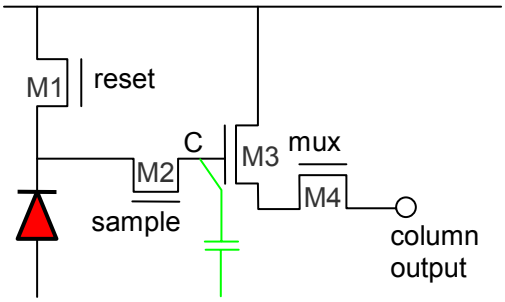


Figure 4: Architecture of the 4T-pixel

The 4T-pixel features a snapshot shutter but can also emulate the 3T-pixel by continuously closing sampling switch M2. Using M4 as a global sample transistor for all pixels enables the snapshot shutter mode. Due to this pixel architecture integration during read out is not possible in synchronous shutter mode.

3.2.2 Color filter array

The IBIS5-A-1300 can also be processed with a Bayer RGB color pattern. Pixel (0,0) has a green filter and is situated on a green-blue row.

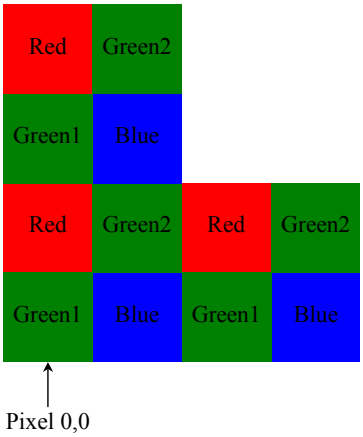


Figure 5: Color filter arrangement on the pixels. Green1 and green2 have a slight different spectral

response due to crosstalk from neighboring pixels. Green1 pixels are located on a blue-green row, green2 pixels are located on a green-red row.

Figure 6 below shows the response of the color filter array as function of the wavelength. Note that this response curve includes the optical cross talk of the pixels. A NIR filter on the color glass lid is used as well (see 6.3.2 for response of the color glass lid) to preserve correct color information.

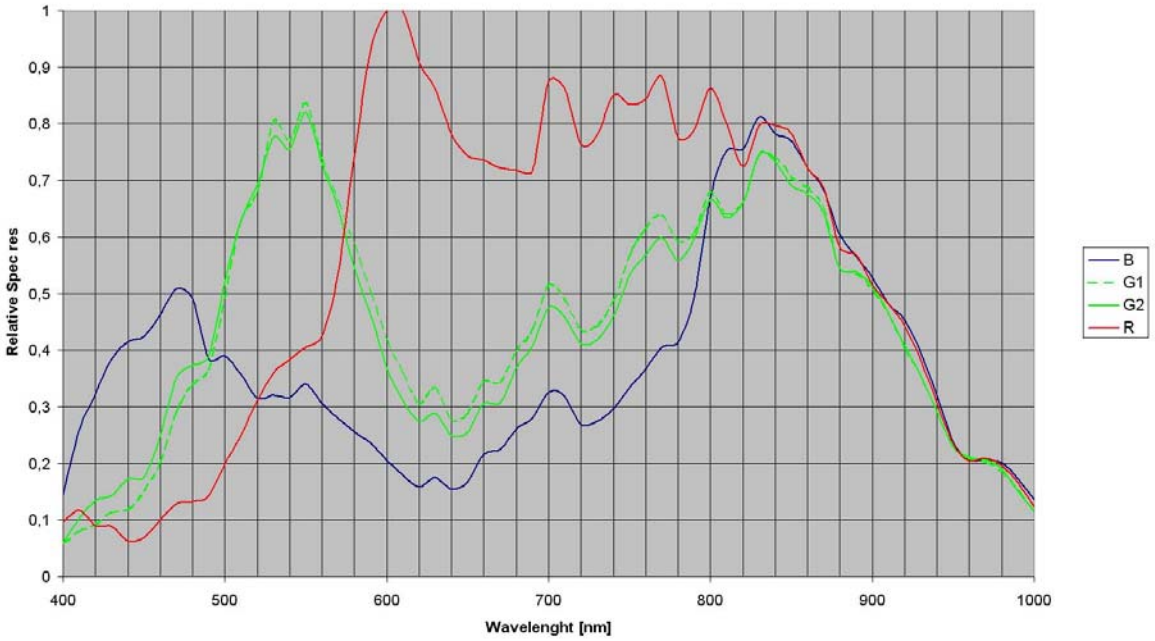


Figure 6: Color filter response curve

3.3 Frame rate

The pixel rate for this sensor is high enough to support a frame rate of >100 Hz for a window size of 640 x 480 pixels (VGA format). Taking into account a row blanking time of 3.5 µs (as baseline, see also 3.10.2.1.4), this requires a minimum pixel rate of nearly 40 MHz. The final bandwidth of the column amplifiers, output stage etc. is determined by external bias resistors. With a nominal pixel rate of 40 MHz a full frame rate of a little more than 27 frames/s is obtained.

The frame period of the IBIS5-A-1300 sensor depends on the shutter type and can be calculated as follows:

3.3.1 Rolling shutter

=> Frame period = (Nr. Lines * (RBT + pixel period * Nr. Pixels))

with: Nr. Lines: Number of Lines read out each frame (Y).
Nr. Pixels: Number of pixels read out each line (X).
RBT: Row Blanking Time = 3.5 µs (typical).
Pixel period: 1/40 MHz = 25 ns.

Example: read out time of the full resolution at nominal speed (40 MHz pixel rate):
=> Frame period = (1024 * (3.5 µs + 25 ns * 1280)) = 36.4 ms => 27.5 fps.

3.3.2 Snapshot shutter

=> Frame period = Tint + Tread out
= Tint + (Nr. Lines * (RBT + pixel period * Nr. Pixels))

with: Tint: Integration (exposure) time.
Nr. Lines: Number of Lines read out each frame (Y).
Nr. Pixels: Number of pixels read out each line (X).
RBT: Row Blanking Time = 3.5 µs (typical).
Pixel period: 1/40 MHz = 25 ns.

Example: read out time of the full resolution at nominal speed (40 MHz pixel rate) with an integration time of 1 ms:
=> Frame period = 1 ms + (1024 * (3.5 µs + 25 ns * 1280)) = 37.4 ms => 26.8 fps.

3.3.3 Region-Of-Interest (ROI) read out

Windowing can easily be achieved by uploading the starting point of the x- and y-shift registers in the sensor registers (see 3.10) using the various interfaces. This downloaded starting point initiates the shift register in the x- and y-direction triggered by the Y_START (initiates the Y-shift register) and the Y_CLK (initiates the X-shift register) pulse. The minimum step size for the x-address is 2 (only even start addresses can be chosen) and 1 for the Y-address (every line can be addressed). The frame rate increases almost linearly when fewer pixels are read out. Table 7 gives an overview of the achievable frame rates (in rolling shutter mode) with various ROI dimensions.

Table 7: Frame rate vs. resolution

Image Resolution (X*Y)	Frame rate [frames/s]	Frame readout time [ms]	Comment
1280 x 1024	*27*	*36*	Full resolution.
640 x 480	*100*	*10*	ROI read out.
100 x 100	*1657*	*0.6*	ROI read out.

3.4 Image core operation

This section describes the functional operation of the image core signalling and supplies considerations.

3.4.1 Image core operation and signalling

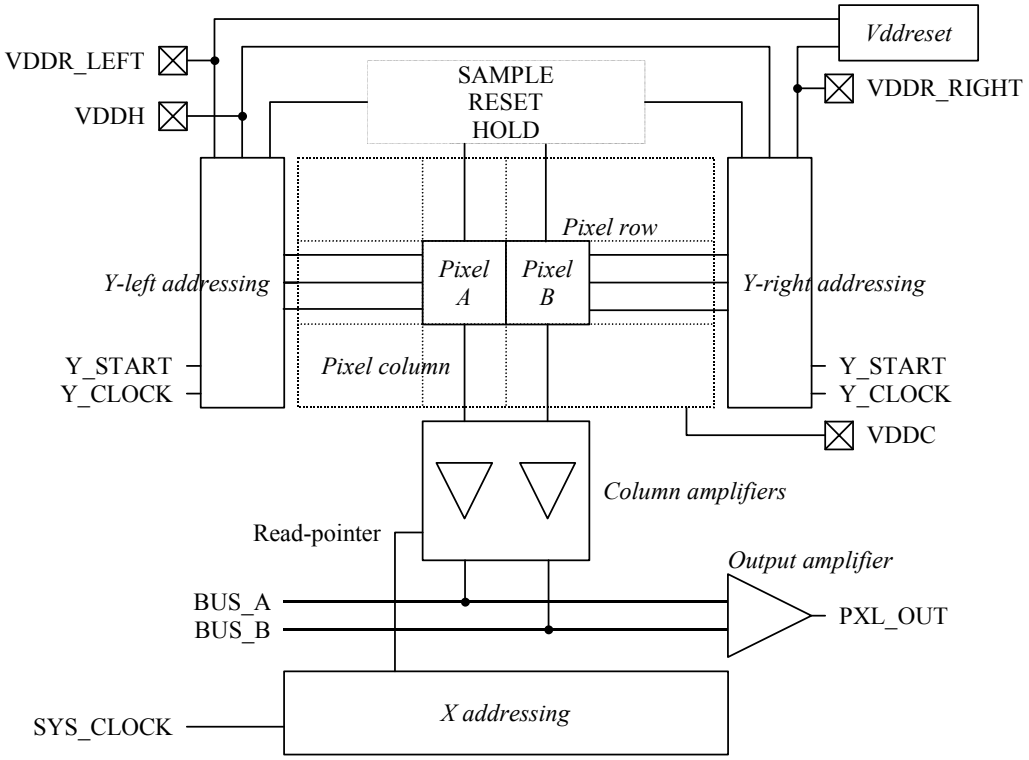


Figure 7: Image core

Figure 7 is a functional representation of the image core without sub-sampling and column/row swapping circuits. Most of the involved signals are not available from the outside because they are generated by the X-sequencer and SS-sequencer blocks.

The integration of the pixels is controlled by internal signals such as reset, sample, hold are generated by the on-chip SS-sequencer that is controlled with the external signals SS_START and SS_STOP. Reading out the pixel array starts by applying a Y_START together with a Y_CLOCK signal; internally this is followed by a calibration sequence to calibrate the output amplifiers (during the row blanking time); signals necessary to do this calibration are generated by the on-chip X-sequencer. This calibration sequence takes typically 3.5 us and is necessary to remove Fixed Pattern Noise of the pixels and of the column amplifiers themselves by means of a Double Sampling technique. After the row blanking time the pixels are fed to the output amplifier. The pixel rate is equal to the

SYS_CLOCK frequency.

3.4.2 Image core supply considerations

The image sensor has several supply voltages:

- *VDDH* is the voltage that controls the sample switches and should always be the highest voltage that is applied to the chip.
- The *VDDR_LEFT* voltage is the highest (nominal) reset voltage of the pixel core.
- The *VDDR_RIGHT* voltage is generated from the *VDDR_LEFT* voltage using a circuit that can be programmed with the KNEEPOINT_LSB/MSB bits in the sequencer register (see also 3.10.2.1.5). By setting the VDDR_RIGHT_EXT bit in the SEQUENCER register, the *VDDR_RIGHT* pin can be disconnected from the circuit and an external voltage can be applied to supply the multiple slope reset voltage. When no external voltage is applied (recommended) the *VDDR_RIGHT* pin should be connected to a capacitor (recommended value = 1µF).
- *VDDC* is the supply of the pixel core.
- *VDDA* is the analog supply of the image core and periphery.
- *VDDD* is the digital supply of the image core and periphery.

Note that the IBIS5-A-1300 image sensor has no power rejection circuitry on-chip. As a consequence all variations on the analog supply voltages can contribute to random variations (noise) on the analog pixel signal, which is seen as random noise in the image. During the camera design precautions have to be taken to supply the sensor with very stable supply voltages to avoid this additional noise.

3.4.2.1 Snapshot shutter supply considerations

When using the IBIS5-A-1300 sensor in snapshot shutter mode only the recommended supply voltage settings are listed below in Table 8.

Table 8: Snapshot shutter recommended supply settings

Symbol	Parameter	Typ	Unit
VDDH	Voltage on HOLD switches.	+4.5	V
VDDR_LEFT	Highest reset voltage.	+4.5	V
VDDC	Pixel core voltage.	+3.3	V
VDDA	Analog supply voltage of the image core.	+3.3	V
VDDD	Digital supply voltage of the image core.	+3.3	V
GNDA	Analog ground.	0	V
GNDD	Digital ground.	0	V
GND_AB	Anti-blooming ground.	0	V

3.4.2.2 Dual shutter supply considerations

With the supply settings listed in Table 8 some fixed column non-uniformities (FPN) can be seen when operating in rolling shutter mode. If a dual shutter mode (both rolling and snapshot shutter) is required during operation one need to apply the supply settings listed in Table 9 below to achieve the best possible image quality.

Table 9: Dual shutter recommended supply settings

Symbol	Parameter	Typ	Unit
VDDH	Voltage on HOLD switches.	+4.5	V
VDDR_LEFT	Highest reset voltage.	+4.5	V
VDDC	Pixel core voltage.	+3.0	V
VDDA	Analog supply voltage of the image core.	+3.3	V
VDDD	Digital supply voltage of the image core.	+3.3	V
GNDA	Analog ground.	0	V
GNDD	Digital ground.	0	V
GND_AB	Anti-blooming ground.	0	V

3.4.3 Image core biasing signals

Table 10 summarizes the biasing signals required to drive the IBIS5-A-1300. For optimizations reasons with respect to speed and power dissipation of all internal block several biasing resistors are needed.

Table 10: Overview of bias signals

Signal	Comment	Related module	DC-level
DEC_CMD	Connect to VDDA with R = 50kΩ and decouple to GNDA with C = 100 nF.	Decoder stage.	1.0 V
DAC_VHIGH	Connect to VDDA with R = 0 Ω.	High level of DAC.	3.3 V
DAC_VLOW	Connect to GNDA with R = 0 Ω.	Low level of DAC.	0.0 V
AMP_CMD	Connect to VDDA with R = 50kΩ and decouple to GNDA with C = 100 nF.	Output amplifier stage.	1.2 V
COL_CMD	Connect to VDDA with R = 50kΩ and decouple to GNDA with C = 100 nF.	Columns amplifiers stage.	1.0 V
PC_CMD	Connect to VDDA with R = 25kΩ and decouple to GNDA with C = 100 nF.	Pre-charge of column busses.	1.1 V
ADC_CMD	Connect to VDDA with R = 50kΩ and decouple to GNDA with C = 100 nF.	Analog stage of ADC.	1.0 V
ADC_VHIGH	Connect to VDDA with R = 90Ω and decouple to GNDA with C = 100 nF.	High level of ADC.	2.9 V
ADC_VLOW	Connect to GNDA with R = 360Ω and	Low level of ADC.	1.4 V

Signal	Comment	Related module	DC-level
	decouple to GNDA with C = 100 nF.		

Each biasing signal determines the operation of a corresponding module in the sense that it controls the speed and power dissipation. The tolerance on the DC-level of the bias levels can vary +/- 150 mV due to process variations.

3.4.4 Pins involved in the image core circuitry

Table 11 gives an overview of the IBIS5-A-1300 pins used by the image core with a short functional description. Power and ground lines are shared between the output amplifier and the image sensor.

Table 11: Pins involved in the image core circuitry

Name	No.	Function
Supply and ground connections		
VDDC	*7, 37*	*Supply of the pixel core.*
VDDA	*8, 36*	*Analog supply of the image core.*
GNDA	*9, 35*	*Analog ground of the image core.*
GNDD	*10, 34*	*Digital ground of the image core.*
VDDD	*11, 33*	*Digital supply of the image core.*
GNDAB	*51*	*Anti-blooming ground.*
VDDR_LEFT	*76*	*High level reset*
VDDH	*77*	*High supply voltage for hold switches in the image core.*
VDDR_RIGHT	*52*	*Multiple slope reset voltage.*
Digital controls		
Y_START	*14 (input)*	*Start frame read out.*
Y_CLOCK	*15 (input)*	*Line clock.*
LAST_LINE	*16 (output)*	*Generates a high level when the last line is read out.*
X_LOAD	*17 (input)*	*Loads new X-position during read out.*
SYS_CLOCK	*18 (input)*	*System (pixel) clock (max. 40MHz).*
PXL_VALID	*19 (output)*	*Pixel valid signal; high during row read out.*
SS_START	*20 (input)*	*Start synchronous shutter operation.*
SS_STOP	*21 (input)*	*Stop synchronous shutter operation.*
TIME_OUT	*22 (output)*	*Synchronous shutter: pulse when integration time is elapsed. Can be used to trigger SS_STOP although both signals can't be tied together.* *Rolling shutter: pulse when second Y-sync appears*
SYS_RESET	*23 (input)*	*Active high signal; have to be pulsed for minimal 5 clock cycles. All registers are set to 0 and sensor is put in a default state. SYS_RESET should be pulsed each time at start up of the sensor.*
EOS_X	*25 (output)*	*Diagnostic end of scan of X-register.*
Reference voltages		
DEC_CMD	*13*	*Decoder bias voltage.*
COL_CMD	*31*	*Column amplifier bias.*
PC_CMD	*32*	*Pre-charge bias voltage.*

3.5 X-addressing

Because of the high pixel rate, the X-shift register selects 2 columns at the time for readout, so it runs at half the system clock speed. All even columns are connected to bus A; all odd columns to bus B. In the output amplifier, bus A and bus B are combined into one stream of pixel data at system clock speed.

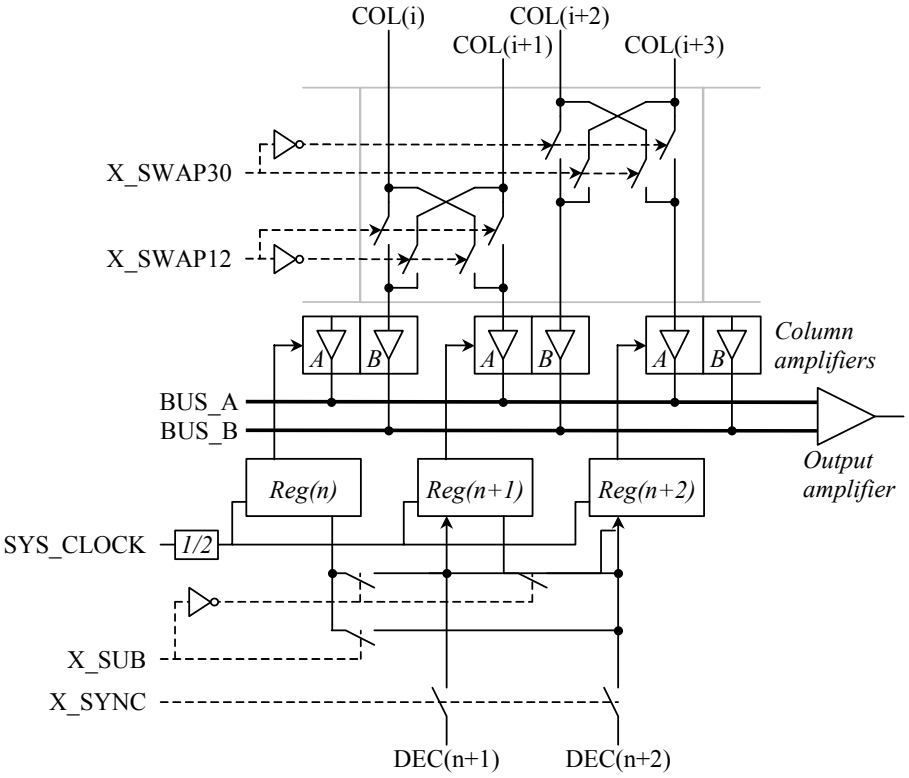


Figure 8: Column structure

At the end of the row blanking time, the X_SYNC switch is closed while all other switches are open and the decoder output is fed to the register. The decoder loads a logical one in one of the registers and a logical zero in the rest. This defines the starting point of the window in the X direction. As soon as the X_SYNC signal is released, the register starts shifting from the start position.

When no sub-sampling is required, X_SUB is inactive. The pointer in the shift-register moves 1 bit at the time. When sub-sampling is enabled, X_SUB is activated. The shift register moves 2 bits at the time. Taking into account that every register selects 2 columns, hence 2 pixels, sub-sampling results in the pattern "XXOOXXOO" when 8 pixels are considered.

Suppose the columns are numbered from left to right starting with 0 (zero) and sub-sampling is enabled:

- If columns 1 and 2, 5 and 6, 9 and 10 … are swapped using the SWAP_12 switches, a normal sub-sampling pattern of "XOXOXOXO" is obtained.
- If columns 3 and 4, 7 and 8, 11 and 12 … are swapped using the SWAP_30 switches, the pattern is "OXOXOXOX".
- If both the SWAP_12 and SWAP_30 switches are closed, pattern "OOXXOOXX" is obtained.

Table 12: X-sub sample patterns

X_SUB	X_SWAP12	X_SWAP30	Sub sample pattern
0	*0*	*0*	XXXXXXXX
1	*0*	*0*	XXOOXXOO
1	*1*	*0*	XOXOXOXO
1	*0*	*1*	OXOXOXOX
1	*1*	*1*	OOXXOOXX

Because every register addresses 2 columns at the time, the addressable pixels range in sub-sample mode is from 0 to half the maximum number of pixels in a row (only even values!). For instance: 0, 2, 4, 6, 8… 638.

3.6 Y-addressing

For symmetry reasons, the sub-sampling modes in the Y-direction are the same as in X-direction.

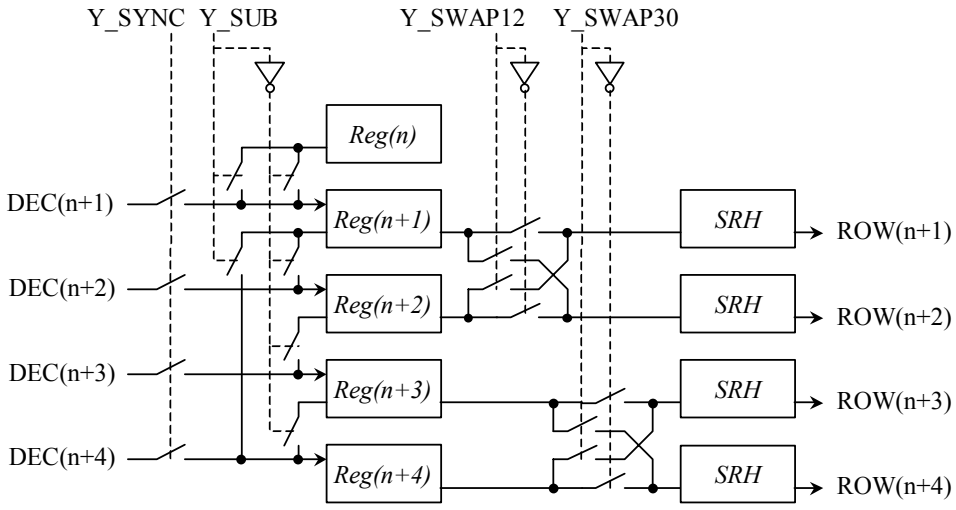


Figure 9: Row structure

Table 13: Y-sub sample patterns

Y_SUB	Y_SWAP12	Y_SWAP30	Sub-sample pattern
0	*0*	*0*	XXXXXXXX
1	*0*	*0*	XXOOXXOO
1	*1*	*0*	XOXOXOXO
1	*0*	*1*	OXOXOXOX
1	*1*	*1*	OOXXOOXX

In normal mode the pointer for the pixel row is shifted one at the time.

When sub-sampling is enabled, Y_SYNC is activated. The Y-shift register shifts 2 succeeding bits and skips the 2 next bits. This results in pattern "XXOOXXOO".

Activating Y_SWAP12 results in pattern "XOXOXOXO".
Activating Y_SWAP30 results in pattern "OXOXOXOX".
Activating both Y_SWAP12 and Y_SWAP30 results in pattern "OOXXOOXX".

The addressable pixels range when Y-sub sampling is enabled is:
0-1, 4-5, 8-9, 12-13, … 1020-1021.

3.7 Output amplifier

3.7.1 Architecture and settings

The output amplifier stage is user-programmable for gain and offset level. Gain is controlled by 4-bit wide word; offset by a 7-bit wide word. Gain settings are on an exponential scale. Offset is controlled by a 7-bit wide DAC, which selects the offset voltage between 2 reference voltages (DAC_VHIGH & DAC_VLOW) on a linear scale.

The amplifier is designed to match the specifications of the output of the imager array. This signal has a data rate of 40 MHz and is located between 1.17V and 2.95V. The output impedance of the amplifier is 260 Ω.

The output signal has a range between 1.17V and 2.95V, depending on the gain and offset settings of the amplifier. At unity gain and with a mid-range offset value the amplifier outputs a signal in between 1.59 V (light) and 2.70 V (dark). This analog range should fit to the input range of the ADC, external or internal. The output swing in unity gain is approximately 1.11V and maximum 1.78V at the highest gain settings.

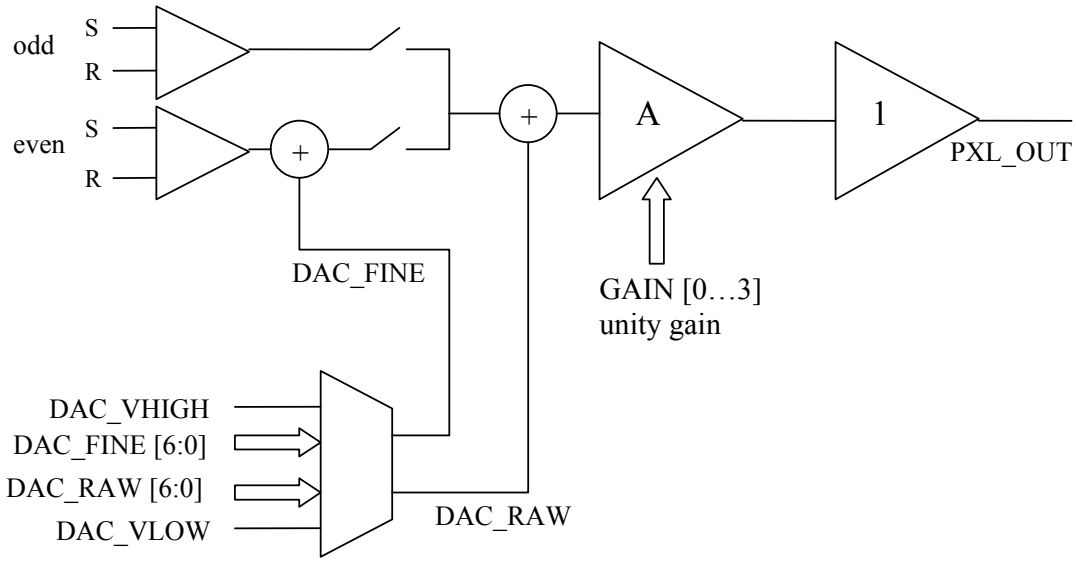


Figure 10: output structure

Figure 10 shows the architecture of the output amplifier. The odd and even column amplifiers sample both pixel and reset value to perform a double sampling FPN - correction. There are 2 different offsets that can be adjusted using the on-chip DAC (7 bit): DAC_FINE and DAC_RAW. DAC_FINE is used to tune the difference between odd and even columns; DAC_RAW is used to add a general (both even and odd columns) to the

FPN corrected pixel value. This pixel value is fed to the first amplifier stage which has an adjustable gain, controlled by a 4-bit word ("GAIN [0…3]").
After this, a unity feedback amplifier buffers the signal and the signal leaves the chip. This 2nd amplifier stage determines the maximal readout speed, i.e. the bandwidth and the slew rate of the output signal. The whole amplifier chain is designed for a data rate of 40 Mpix/s (@20 pF).

3.7.2 Output amplifier gain control

The output amplifier gain is controlled by a 4-bit word set in the AMPLIFIER register (see section 3.10.2.8). An overview of the gain settings is given in Table 14.

Table 14: Overview gain settings

bits	DC gain	bits	DC gain
0000	*1.37*	1000	*6.25*
0001	*1.62*	1001	*7.89*
0010	*1.96*	1010	*9.21*
0011	*2.33*	1011	*11.00*
0100	*2.76*	1100	*11.37*
0101	*3.50*	1101	*11.84*
0110	*4.25*	1110	*12.32*
0111	*5.20*	1111	*12.42*

3.7.3 Setting of the DAC reference voltages

In the output amplifier, the offset can be trimmed by loading registers DACRAW_REG and DACFINE_REG. DAC_RAW is used to adjust the offset of the output amplifier and DAC_FINE is used to tune the offset between the even and odd columns.
These registers are inputs for 2 DACs (see Figure 10) that operate on the same resistor that is connected between pins DAC_VHIGH and DAC_VLOW. The range of the DAC is defined using a resistive division with R_{VHIGH}, R_{DAC} and R_{VLOW}.

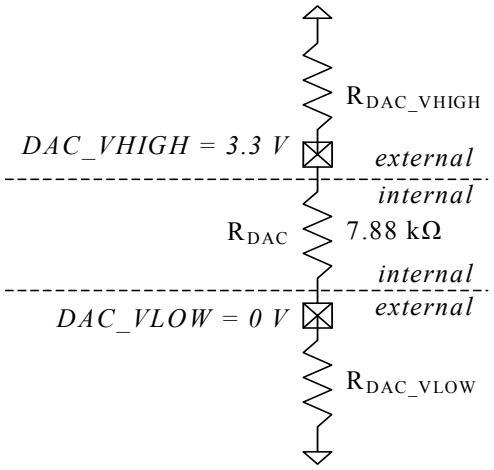


Figure 11: In- and external DAC connections

The internal resistor R_{DAC} has a value of approximately 7.88 kΩ.
The recommend resistor values for both DAC_VLOW and DAC_VHIGH are 0Ω.

3.7.4 Pins involved in the output amplifier circuitry

Table 15 gives an overview of the IBIS5-A-1300 pins used by the output amplifier with a short functional description. Power and ground lines are shared between the output amplifier and the image sensor.

Table 15: Pins involved in the output amplifier circuitry

Name	No.	Function
Analog signals		
PXL_OUT1	*28*	*Analog output signal* *To be connected to the input of the ADC (ADC_IN, pin 69)*
PXL_OUT2	*29*	*Analog output signal* *To be connected to the input of the ADC (ADC_IN, pin 69)* *Note: 2 Outputs were designed for debugging reasons but it seemed not necessary. It is possible to use them both if you want to send even and odd pixels (or lines) to 2 outputs. There is no speed gain when using 2 outputs because the 2 outputs run at a halved output rate (20MHz). It recommended to use only one analog output (connect PXL_OUT1 to ADC_IN).*
Digital Controls		
EL_BLACK	*24*	*Active high digital input.* *When this signal is pulsed a hardware black level is fed to the output amplifier instead of the normal pixel values. The hardware black level can be changed by the DAC_RAW register.*
Reference voltages		
DAC_VHIGH	*26*	*High reference voltage of the DAC.*
DAC_VLOW	*27*	*Low reference voltage of the DAC.*
AMP_CMD	*30*	*Output amplifier speed/power bias voltage. Can be used to enhance the speed of the output stage.*

3.8 Analog to digital converter

The IBIS5-A-1300 has a 10 bit flash analog digital converter running nominally at 40 Msamples/s. The ADC is electrically separated from the image sensor. The input of the ADC (ADC_IN; pin 69) should be tied externally to the output (PXL_OUT1; pin 28) of the output amplifier.

Table 16: ADC specifications

Input range	*1 – 3V (*)*
Quantization	*10 Bits*
Nominal data rate	*40 Msamples/s*
DNL (linear conversion mode)	*Typ. < 0.5 LSB*
INL (linear conversion mode)	*Typ. < 3 LSB*
Input capacitance	*< 20 pF*
Power dissipation @ 40 MHz	*Typ. 45 mA * 3.3V = 150 mW*
Conversion law	*Linear / Gamma-corrected*

(*): The internal ADC range will be typically 100mV lower then the external applied ADC_VHIGH and ADC_VLOW voltages due to voltage drops over parasitic internal resistors in the ADC.

3.8.1 ADC timing

At the rising edge of SYS_CLOCK the next pixel is fed to the input of the output amplifier. Due to internal delays of the SYS_CLOCK signal it takes approximately 20 ns before the output amplifier outputs the analog value of the pixel as shown in Figure 12.
The ADC converts the pixel data on the rising edge of the ADC_CLOCK but it takes 2 clock cycles before this pixel data is at the output of the ADC. This pipeline delay is shown in Figure 12.
Due to these delays it is advised that a variable phase difference is foreseen between the ADC_CLOCK and the SYS_CLOCK to tune the optimal sample moment of the ADC.

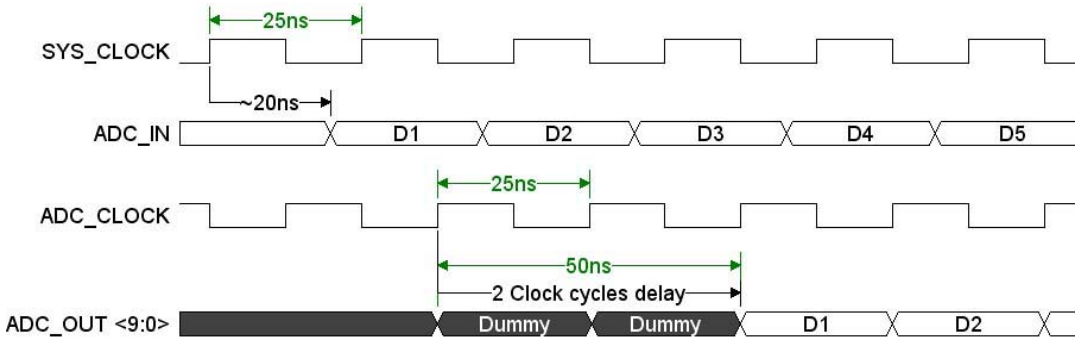


Figure 12: ADC timing

3.8.2 Setting of the ADC reference voltages

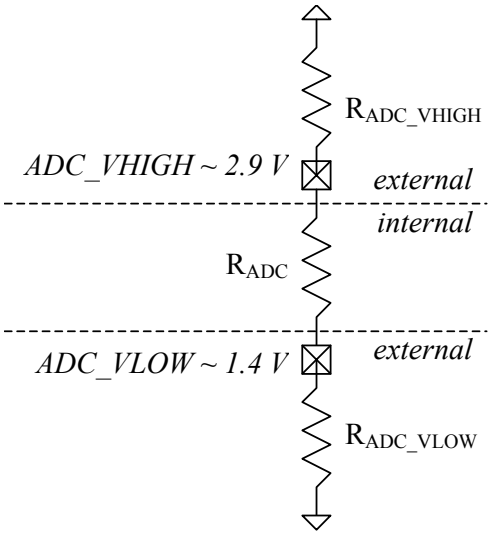


Figure 13: In- and external ADC connections

The internal resistor R_{ADC} has a value of approximately 385 Ω. This results in the following values for the external resistors:

Resistor	Value (Ω)
R_{ADC_VHIGH}	*90*
R_{ADC}	*385*
R_{ADC_VLOW}	*360*

Note that the recommended ADC resistors value yields in a conversion of the full analog output swing at unity gain (V_{DARK_ANALOG} < ADC_VHIGH and V_{LIGHT_ANALOG} > ADC_VLOW).

The values of the resistors depend on the value of R_{ADC}. The voltage difference between ADC_VLOW and ADC_VHIGH should be at least 1.0V to assure proper working of the ADC.

3.8.3 Non-linear and linear conversion mode – "gamma" correction

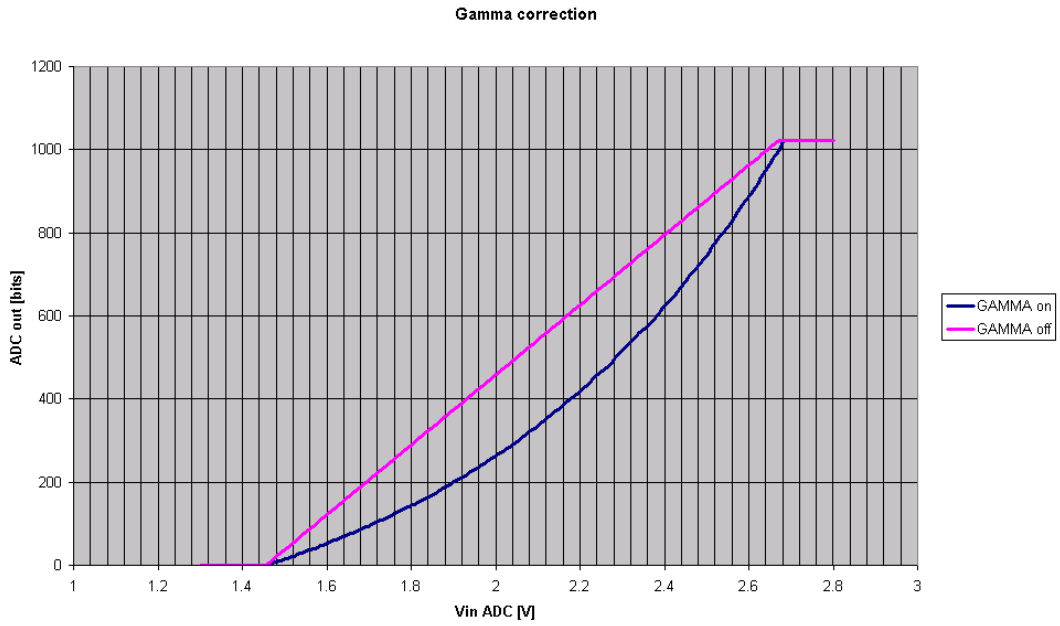


Figure 14: linear and non-linear ADC conversion characteristic

Figure 14 shows the ADC transfer characteristic. The non-linear (exponentional) ADC conversion is intended for gamma-correction of the images. It increases contrast in dark areas and reduces contrast in bright areas. The non-linear transfer function is given by:

$$Vin = ADC\_VHIGH + (ADC\_VHIGH - ADC\_VLOW) * \frac{a*x + b*x^2}{a*1023+b*1023^2}$$

With: $a=5$
$b=0.027$
x=digital output code

3.8.4 Pins involved in the ADC circuitry

Table 17 gives an overview of the IBIS5-A-1300 pins involved in the ADC circuitry.

Table 17: Pins involved in the ADC circuitry

Name	No.	Description
Analog signals		
ADC_IN	*69*	*Input, connect to sensor's output (PXL_OUT1; pin 28)*
Digital Controls		
ADC_CLOCK	*58 (input)*	*ADC clock; ADC converts on rising edge.*
Digital output		
ADC_OUT<9>..<0>	*59…68*	*Output bits; <0> = LSB, <9> = MSB*
Reference voltages		
ADC_VHIGH	*75*	*ADC high reference voltage*
ADC_VLOW	*53*	*ADC low reference voltage*
ADC_CMD	*70*	*ADC speed/power bias voltage.*
Power & Ground		
ADC_VDDD	*57, 71*	*ADC digital supply (3.3V)*
ADC_GNDA	*54, 72*	*ADC analog ground (0.0V)*
ADC_GNDD	*56, 73*	*ADC digital ground (0.0V)*
ADC_VDDA	*55, 74*	*ADC analog supply (3.3V)*

3.9 Electronic shutter types

The IBIS5-A-1300 has 2 different shutter types: a rolling (curtain) shutter and a snapshot (synchronous) shutter.

3.9.1 Rolling (curtain) shutter

The name is due to the fact that the effect is similar to a curtain shutter of a SLR film camera. Although it is a pure electronic operation, the shutter seems to slide over the image. A rolling shutter is easy and elegant to implement in a CMOS sensor. As can be seen in Figure 15, there are two Y shift registers. One of them points to the row that is currently being read out. The other shift register points to the row that is currently being reset. Both pointers are shifted by the same Y-clock and move over the focal plane. The integration time is set by the delay between both pointers.

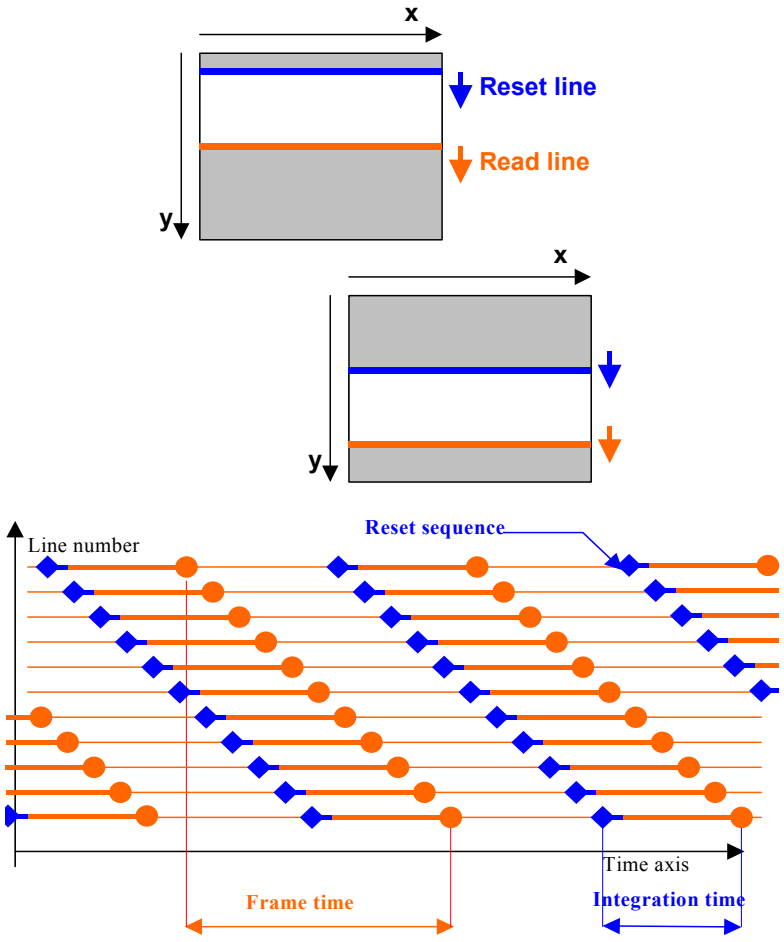


Figure 15: Rolling shutter operation

In Figure 15, we schematically indicate the relative shift of the integration times of different lines during the rolling shutter operation. Each line is read and reset in a sequential way. The integration time is the same for all lines, but is shifted in time. The integration time can be varied through the INT_TIME register (in number of lines).
This indicates us that all pixels are light sensitive at another period of time, which can cause some blurring if a fast moving object is captured.

When the sensor is set to rolling shutter mode, the input SS_START and SS_STOP should best be held low.

3.9.2 Snapshot (synchronous) shutter

A synchronous (global, snapshot) shutter solves that inconvenience. Light integration takes place on all pixels in parallel, although subsequent readout is sequential.

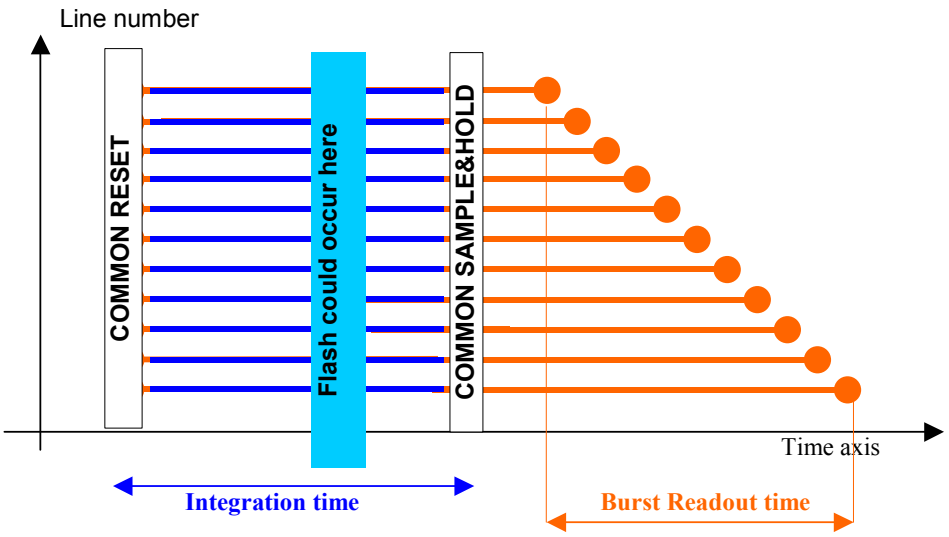


Figure 16: Synchronous shutter operation

Figure 16 shows the integration and read out sequence for the synchronous shutter. All pixels are light sensitive at the same period of time. The whole pixel core is reset simultaneously and after the integration time all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. Note that the integration and read out cycle is carry out in serial, which causes that no integration is possible during read out.

During synchronous shutter the input pins SS_START and SS_STOP are used to start and

stop the synchronous shutter.

3.10 Sequencer

Figure 7 showed a number of control signals that are needed to operate the sensor in a particular sub-sampling mode, with a certain integration time, output amplifier gain, etc. Most of these signals are generated on chip by the sequencer that uses only a few control signals. These control signals should be generated by the external system:

- SYS_CLOCK (X-clock), which will define the pixel rate,
- Y_START pulse, which will indicate the start of a new frame,
- Y_CLOCK, which will select a new row and will start the row blanking sequence, including the synchronization and loading of the X-register.
- SS_START and SS_STOP to control the integration period in snapshot shutter mode.

The relative position of the pulses will be determined by a number of data bits that are uploaded in internal registers through the serial or parallel interface.

3.10.1 Internal registers

Table 18 shows a list of the internal registers with a short description. In the next section, the registers are explained in more detail.

Table 18: Internal registers

Register	Bit	Name	Description
0 (0000)	11:0	SEQUENCER register	*Default value <11:0>:"000011000100"*
	0	SHUTTER_TYPE	1 = rolling shutter 0 = synchronous shutter
	1	FRAME_CAL_MODE	0 = fast 1 = slow
	2	LINE_CAL_MODE	0 = fast 1 = slow
	3	CONT_CHARGE	1 = "Continuous" precharge enabled.
	4	GRAN_X_SEQ_LSB	Granularity of the X sequencer clock
	5	GRAN_X_SEQ_MSB	
	6	GRAN_SS_SEQ_LSB	Granularity of the SS sequencer clock
	7	GRAN_SS_SEQ_MSB	
	8	KNEEPOINT_LSB	Sets reset voltage for multiple slope operation.
	9	KNEEPOINT_MSB	
	10	KNEEPOINT_ENABLE	1 = Enables multiple slope operation in synchronous shutter mode
	11	VDDR_RIGHT_EXT	1 = Disables circuit that generates VDDR_RIGHT voltage so external voltage can be applied.
1 (0001)	11:0	NROF_PIXELS	Number of pixels to count (maximum 1280/2).

Register	Bit	Name	Description
			Default value <11:0>:"001001111111"
2 (0010)	11:0	NROF_LINES	Number of lines to count. *Default value <11:0>:"001111111111"*
3 (0011)	11:0	INT_TIME	Integration time. *Default value <11:0>:"111111111111"*
4 (0100)	10:0	X_REG	X start position (maximum 1280/2). *Default value <10:0>:"00000000000"*
5 (0101)	10:0	YL_REG	Y-left start position. *Default value <10:0>:"00000000000"*
6 (0110)	10:0	YR_REG	Y-right start position. *Default value <10:0>:"00000000000"*
7 (0111)	7:0	IMAGE CORE register	*Default value <7:0>:"00000000"*
	0	TEST_EVEN	Test even columns.
	1	TEST_ODD	Test odd columns.
	2	X_SUBSAMPLE	Enable sub-sampling in X-direction.
	3	X_SWAP12	Swap columns 1-2, 5-6, …
	4	X_SWAP30	Swap columns 3-4, 7-8, …
	5	Y_SUBSAMPLE	Enable sub-sampling in Y-direction.
	6	Y_SWAP12	Swap rows 1-2, 5-6, …
	7	Y_SWAP30	Swap rows 3-4, 7-8, …
8 (1000)	6:0	AMPLIFIER register	*Default value <6:0>:"1010000"*
	0	GAIN<0>	Output amplifier gain setting.
	1	GAIN<1>	
	2	GAIN<2>	
	3	GAIN<3>	
	4	UNITY	1 = Amplifier in unity gain mode.
	5	DUAL_OUT	1 = Activates second output.
	6	STANDBY	0 = Amplifier in standby mode.
9 (1001)	6:0	DACRAW_REG	Amplifier DAC raw offset. *Default value <6:0>:"1000000"*
10 (1010)	6:0	DACFINE_REG	Amplifier DAC fine offset. *Default value <6:0>:"1000000"*
11 (1011)	2:0	ADC register	*Default value <2:0>:"011"*
	0	TRISTATE_OUT	0 = output bus in tri-state.
	1	GAMMA	0 = Gamma-correction on.
	2	BIT_INV	1 = Bit inversion on output bus.
12 (1100)		Reserved.	
13 (1101)		Reserved.	
14 (1110)		Reserved.	
15 (1111)		Reserved.	

3.10.2 Detailed description of the internal registers

3.10.2.1 Sequencer register (7:0)

3.10.2.1.1 Shutter type (bit 0)

The IBIS5-A-1300 image sensor has 2 shutter types:

0 = synchronous shutter.
1 = rolling shutter.

3.10.2.1.2 Output amplifier calibration (bits 1 and 2)

Bits FRAME_CAL_MODE and LINE_CAL_MODE define the calibration mode of the output amplifier.

During every row-blanking period, a calibration is done of the output amplifier. There are 2 calibration modes. The FAST mode (= 0) can force a calibration in one cycle but is not so accurate and suffers from KTC noise, while the SLOW mode (= 1) can only make incremental adjustments and is noise free.
Approximately 200 or more "slow" calibrations will have the same effect as 1 "fast" calibration.

Different calibration modes can be set at the beginning of the frame (FRAME_CAL_MODE bit) and for every subsequent line that is read (LINE_CAL_MODE bit). The beginning of a frame is defined by the Y_START input (see lower), Y_CLOCK defines the beginning of a new row.

3.10.2.1.3 Continuous charge (bit 3)

For some applications it might be necessary to use continuous charging of the pixel columns instead of a pre-charge on every line sample operation.
Setting bit CONT_CHARGE to "1" will activate this function. The resistor connected to pin PC_CMD is used to control the current level on every pixel column.

3.10.2.1.4 Internal clock granularities (bits 4, 5, 6 and 7)

The system clock is divided several times on chip.

The X-shift-register that controls the column/pixel readout, is clocked by half the system clock rate. Odd and even pixel columns are switched to 2 separate buses. In the output amplifier the pixel signals on the 2 buses are combined into one pixel stream at the same frequency as SYS_CLOCK.

The clock, that drives the "snapshot" or synchronous shutter sequencer, can be programmed using the bits GRAN_SS_SEQ_MSB (bit 7) and GRAN_SS_SEQ_LSB (bit 6).
This way the integration time in synchronous shutter mode can be a multiple of 32, 64, 128 or 256 times the system clock period. To overcome global reset issues it is advised

that the longest SS granularity is used (bits 6&7 set to '1').

Table 19: SS sequencer clock granularities

GRAN_SS_SEQ_MSB/LSB	SS-sequencer clock	Integration time step*
00	*32 x SYS_CLOCK*	*800 ns*
01	*64 x SYS_CLOCK*	*1.6 us*
10	*128 x SYS_CLOCK*	*3.2 us*
11	*256 x SYS_CLOCK*	*6.4 us*

* using a SYS_CLOCK of 40 MHz (25 ns period)

The clock that drives the X-sequencer can be a multiple of 4, 8, 16 or 32 times the system clock. Clocking the X-sequencer at a slower rate (longer row blanking time; pixel read out speed is always equal to the SYSTEM_CLOCK) can result in more signal swing for the same light conditions.

Table 20: X sequencer clock granularities

GRAN_X_SEQ_MSB/LSB	X-sequencer clock	Row Blanking Time*
00	*4 x SYS_CLOCK*	*3.5 us*
01	*8 x SYS_CLOCK*	*7 us*
10	*16 x SYS_CLOCK*	*14 us*
11	*32 x SYS_CLOCK*	*28 us*

* using a SYS_CLOCK of 40 MHz (25 ns period)

3.10.2.1.5 Pixel reset knee-point for multiple slope operation (bits 8, 9 and 10)

In normal (single slope) mode the pixel reset is controlled from the left side of the image core using the voltage applied on pin VDDR_LEFT as pixel reset voltage.
In multiple slope operation one or more variable pixel reset voltages have to be applied.
Bits KNEE_POINT_MSB and KNEE_POINT_LSB select the on chip-generated pixel reset voltage.
Bit KNEE_POINT_ENABLE set to "1" switches control to the right side of the image core so the pixel reset voltage (VDDR_RIGHT), selected by bits KNEE_POINT_MSB/LSB, is used.
Bit KNEE_POINT_ENABLE should only be used for multiple slope operation in synchronous shutter mode. In rolling shutter mode, only the bits KNEE_POINT_MSB/LSB must be used to select the second knee-point in dual slope operation.

Table 21: Multiple slope register settings

KNEE_POINT		Pixel reset voltage (V) VDDR_RIGHT	Knee-point (V)
MSB/LSB	ENABLE (1)		
00	*0 or 1*	*VDDR_LEFT*	*0*
01	*1*	*VDDR_LEFT – 0.76*	*+ 0.76*
10	*1*	*VDDR_LEFT – 1.52*	*+ 1.52*
11	*1*	*VDDR_LEFT – 2.28*	*+ 2.28*

The actual knee-point depends on VDDH, VDDR_LEFT and VDDC applied to the sensor.

3.10.2.1.6 External pixel reset voltage for multiple slope (bit 11)

When bit VDDR_RIGHT_EXT is set to "1", the circuit that generates the variable pixel reset voltage is disabled and the voltage externally applied to pin VDDR_RIGHT is used as the double/multiple slope reset voltage.
When bit VDDR_RIGHT_EXT is set to "0" the variable pixel reset voltage (used for multiple slope operation) can be monitored on pin VDDR_RIGHT.

3.10.2.2 NROF_PIXELS register (11:0)

After the internal x_sync is generated (start of the pixel readout of a particular row), the PIXEL_VALID signal goes high. The PIXEL_VALID signal goes low when the pixel counter reaches the value loaded in the NROF_PIXEL register. Due to the fact that 2 pixels are read at the same clock cycle this number have to be divided by 2 (NROF_PIXELS = (width of ROI / 2) - 1).

3.10.2.3 NROF_LINES register (11:0)

After the internal yl_sync is generated (start of the frame readout with Y_START), the line counter increases with each Y_CLOCK pulse until it reaches the value loaded in the NROF_LINES register and an LAST_LINE pulse is generated.

3.10.2.4 INT_TIME register (11:0)

The INT_TIME register is used to set the integration time of the electronic shutter. The interpretation of the INT_TIME depends on the chosen shutter type (rolling or synchronous).

Synchronous shutter

After the SS_START pulse is applied an internal counter counts the number of SS granulated clock cycles until it reaches the value loaded in the INT_TIME register and a TIME_OUT pulse is generated. This TIME_OUT pulse can be used to generate the SS_STOP pulse to stop the integration. When the INT_TIME register is used the maximum integration time is:

$$T_{INT\_MAX} = 2^{12} * 256 \text{ (maximum granularity)} * (40 \text{ MHZ})^{-1} = 26.2 \text{ ms.}$$

This maximum time can be increased if an external counter is used to trigger SS_STOP. The minimal value that should be loaded into the INT_TIME register is 10 (see also 3.10.2.1.4).

Rolling shutter

When the Y_START pulse is applied (start of the frame readout), the sequencer will generate the yl_sync pulse for the left Y-shift register (read out Y-shift register). This loads the left Y-shift register with the pointer loaded in YL_REG register. At each Y_CLOCK pulse, the pointer shifts to the next row and the integration time counter increases until it reaches the value loaded in the INT_TIME register. At that moment, the

yr_sync pulse for the right Y-shift register is generated which loads the right Y-shift register (reset Y-shift register) with the pointer loaded in YR_REG register (*Figure 17*). The integration time counter is reset when the sync for the left Y-shift register is asserted. Both shift registers keep moving until the next sync is asserted (Y_START for the left Y-shift register and the sync for the right Y-shift register is generated when the integration time counter reaches the INT_TIME value).

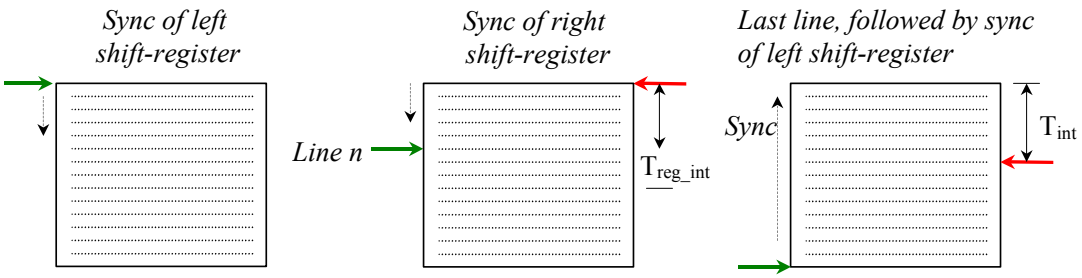


Figure 17: Synchronization of the shift registers in rolling shutter mode.

T_{reg_int} Difference between left and right pointer = value set in the INT_TIME register (number of lines).

The actual integration time is given by:

T_{int} Integration time [# lines] = NROF_LINES register - INT_TIME register

3.10.2.5 X_REG register (10:0)

The X_REG register determines the start position of the window in the X-direction. In this direction, there are 640 possible starting positions (2 pixels are addressed at the same time in one clock cycle). If sub sampling is enabled only the even pixels can be set as starting position (for instance: 0, 2, 4, 6, 8… 638).

3.10.2.6 YL_REG (10:0) and YR_REG (10:0)

The YL_REG and YR_REG registers determine the start position of the window in the Y-direction. In this direction, there are 1024 possible starting positions. In rolling shutter mode the YL_REG register sets the start position of the read (left) pointer and the YR_REG sets the start position of the reset (right) pointer. For both shutter types YL_REG should always be equal to YR_REG.

3.10.2.7 Image core register (7:0)

Bits 1:0 of the IMAGE_CORE register define the test mode of the image core. Setting 00 is the default and normal operation mode. In case the bit is set to 1, the odd (bit 1) or even (bit 0) columns are tight to the reset level. If the internal ADC is used bits 0 and 1 can be used to create test pattern to test the sample moment of the ADC. If the ADC sample moment is not chosen correctly the created test pattern will not be black-white-black-etc.

(IMAGE_CORE register set at 1 or 2) or black-black-white-white-black-black (IMAGE_CORE register set at 9) but grey shadings if the sensor is saturated. See also paragraph 3.8.10 for detailed ADC timing.
Bits 7:2 of the IMAGE_CORE register define the sub-sampling mode in the X-direction (bits 4:2) and in the Y-direction (bits 7:5). The sub-sampling modes and corresponding bit setting are given in Table 12 (section 3.5) and Table 13 (section 3.6).

3.10.2.8 Amplifier register (6:0)

3.10.2.8.1 GAIN (bits 3:0)

The gain bits determine the gain setting of the output amplifier. They are only effective if UNITY = 0. The gains and corresponding bit setting are given in Table 14 section 3.7.2).

3.10.2.8.2 UNITY (bit 4)

In case UNITY = 1, the gain setting of GAIN is bypassed and the gain amplifier is put in unity feedback.

3.10.2.8.3 DUAL_OUT (bit 5)

If DUAL_OUT = 1, the two output amplifiers are active. If DUAL_OUT = 0, the signals from the two busses are multiplexed to output PXL_OUT1 which should be connected to ADC_IN. The gain amplifier and output driver of the second path are put in standby.

3.10.2.8.4 STANDBY

If STANDBY = 0, the complete output amplifier is put in standby. For normal use STANDBY should be set to 1.

3.10.2.9 DAC_RAW register (6:0) and DAC_FINE (6:0) register

These registers determine the black reference level at the output of the output amplifier. Bit setting 1111111 for DAC_RAW register gives the highest offset voltage, bit setting 0000000 for DAC_RAW register gives the lowest offset voltage. Ideally, if the two output paths have no offset mismatch, the DAC_FINE register must be set to 1000000. Deviation from this value can be used to compensate the internal mismatch (see 3.7).

3.10.2.10 ADC register (2:0)

3.10.2.10.1 TRISTATE_OUT (bit 0)

In case TRISTATE = 0, the ADC_D<9:0> outputs are in tri-state mode. TRISTATE = 1 for normal operation mode.

3.10.2.10.2 GAMMA (bit 1)

If GAMMA is set to 1, the ADC input to output conversion is linear; otherwise the

conversion follows a ‘gamma’ law (more contrast in dark parts of the window, lower contrast in the bright parts). See section 3.8.3 for more details.

3.10.2.10.3 BIT_INV (bit 2)

If BIT_INV = 1, 0000000000 is the conversion of the lowest possible input voltage, otherwise the bits are inverted.

3.10.3 Data interfaces

2 different data interfaces are implemented. They can be selected using pins IF_MODE (pin 12) and SER_MODE (pin 6).

Table 22: Serial and parallel interface selection

IF_MODE	SER_MODE	Selected interface
1	X	*Parallel*
0	1	*Serial 3 Wire*
0	0	*No mode selected.*

3.10.3.1 Parallel interface

The parallel interface uses a 16-bit parallel input (P_DATA <15:0>) to upload new register values. Asserting P_WRITE will load the parallel data into the internal register of the IBIS5-A-1300 where it is decoded.

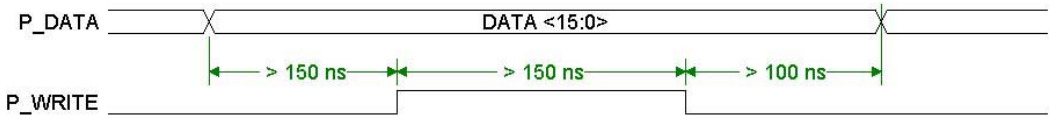


Figure 18: Parallel interface timing

P_DATA (15:12)	Address bits	REG_ADDR (3:0)
P_DATA (11:0)	Data bits	REG_DATA (11:0)

3.10.3.2 Serial-3-wire interface

The serial-3-wire interface (or Serial-to-Parallel Interface) uses a serial input to shift the data in the register buffer. When the complete data word is shifted into the register buffer the data word is loaded into the internal register where it is decoded.

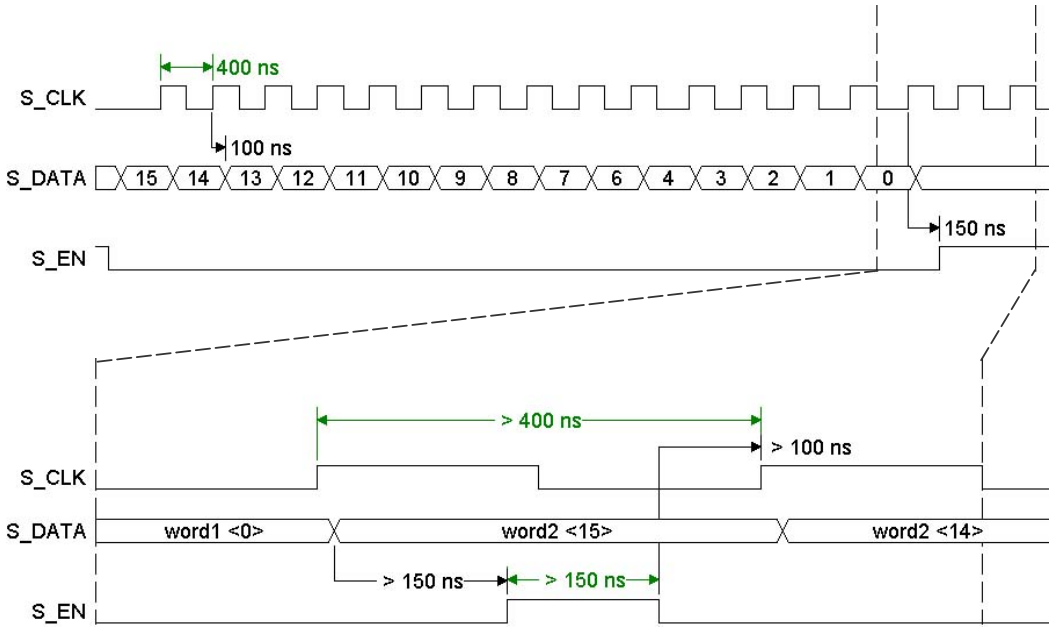


Figure 19: Serial-3 –wire interface timing

S_DATA (15:12) Address bits REG_ADDR (3:0)
S_DATA (11:0) Data bits REG_DATA (11:0)
When S_EN is asserted the parallel data is loaded into the internal registers of the IBIS5-A-1300. The maximum tested frequency of S_DATA is 2.5 MHz.

3.10.3.3 Pins involved in the interface circuitry

Table 23: Pins involved in the interface circuitry

Name	No.	Function
Digital controls		
P_DATA<0>…<7>	*38-45*	*Data parallel interface. <0> : LSB*
P_DATA<15>…<9>	*78-84*	*Data parallel interface. <15> : MSB*
P_DATA<8>	*1*	*Date parallel interface.*
SI2_ADDR<0>…<4>	*46-50*	*2 wire serial address bits (7 bits).* *<0>:LSB <4>:MSB* *Bits 4,5 and 6 are tied together.*
P_WR	*2*	*Parallel write.*
S_CLK	*3*	*Clock serial interface.*
S_DATA	*4*	*Data serial interface.*
S_EN	*5*	*Enable serial interface.*
SER_MODE	*6*	*Serial mode: 0 = Disable; 1 = Serial-3-wire enabled.*

4 Timing diagrams

4.1 Timing requirements

There are 6 control signals that operate the image sensor:

- SS_START
- SS_STOP
- Y_CLOCK
- Y_START
- X_LOAD
- SYS_CLOCK

These control signals should be generated by the external system with following time constraints to SYS_CLOCK (rising edge = active edge):

- T_{SETUP} >7.5 ns.
- T_{HOLD} > 7.5 ns.

It is important that these signals are free of any glitches.

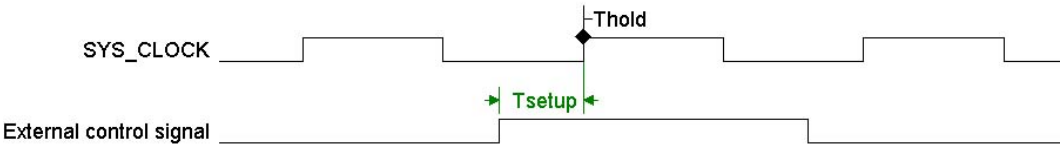


Figure 20: Relative timing of the 5 sequencer control signals

Figure 22 shows a recommended schematic for generating the basic signals and to avoid any timing problems.

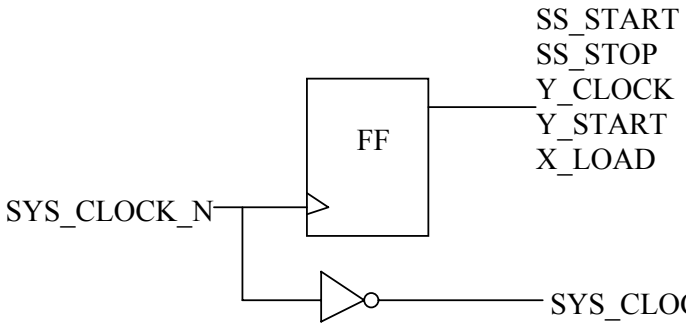


Figure 21: Recommended schematic for generating basic signals

4.2 Synchronous shutter: single slope integration

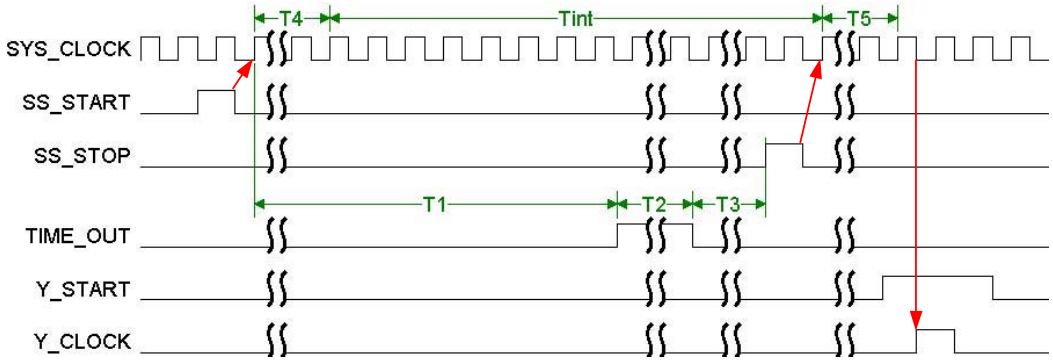


Figure 22: Synchronous shutter: single slope integration

SS_START and SS_STOP should change on the falling edge of the SYS_CLOCK (Tsetup and Thold > 7.5 ns). The pulse width of both signals should be minimum 1 SYS_CLOCK cycle. As long as SS_START or SS_STOP are asserted, the sequencer stays in a suspended state.

T_1 Time counted by the integration timer until the value of INT_TIME register is reached. The integration timer is clocked by the granulated SS-sequencer clock.

T_2 TIME_OUT signal stays high for 1 granulated SS-sequencer clock period.

T_3 There are no constraints for this time. The user can use the TIME_OUT signal to trigger the SS_STOP pin (or use an external counter to trigger SS_STOP) although that both signal can't be tied together.

T_4 During this time, the SS-sequencer applies the control signals to reset the image core and start integration. This takes 4 granulated SS-sequencer clock periods. The integration time counter starts counting at the first rising edge after the falling edge of SS_START.

T_5 The SS-sequencer puts the image core in a readable state. It takes 2 granulated SS-sequencer clock periods.

T_{int} The "real" integration or exposure time.

4.3 Synchronous shutter: pixel readout

4.3.1 Basic operation

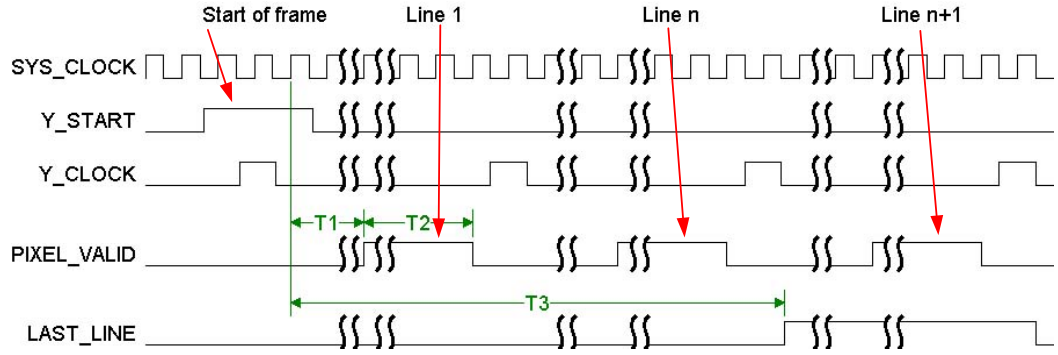


Figure 23: Synchronous shutter: pixel read out

Y_START and Y_CLOCK should change on the falling edge of the SYS_CLOCK (Tsetup and Thold > 7.5 ns). The pulse width should be minimum 1 clock cycle for Y_CLOCK and 3 clock cycles for Y_START. As long as Y_CLOCK is applied, the sequencer stays in a suspended state.

T_1 Row blanking time: During this period, the X-sequencer generates the control signals to sample the pixel signal and pixel reset levels (double sampling fpn-correction), and start the readout of one line. The row blanking time depends on the granularity of the X-sequencer clock (see below).

Table 24: Row blanking time as function of X-sequencer granularity

Granularity N_{GRAN}	T_1 (µs) = 35 x N_{GRAN} x $T_{SYS\ CLOCK}$	GRAN_X_SEQ MSB/LSB
x 4	*140 x $T_{SYS\ CLOCK}$ = 3.5*	00
x 8	*280 x $T_{SYS\ CLOCK}$ = 7.0*	01
x 16	*560 x $T_{SYS\ CLOCK}$ = 14.0*	10
x 32	*1120 x $T_{SYS\ CLOCK}$ = 28.0*	11

T_2 Pixels counted by pixel counter until the value of NROF_PIXELS register is reached. PIXEL_VALID goes high when the internal X_SYNC signal is generated, in other words when the readout of the pixels is started. PIXEL_VALID goes low when the pixel counter reaches the value loaded in the NROF_PIXELS register (after a complete row read out).

T_3 LAST_LINE goes high when the line counter reaches the value loaded in the NROF_LINES register and stays high for 1 line period (until the next falling edge of Y-CLOCK).

On Y_START the left Y-shift-register of the image core is loaded with the YL-pointer that

is loaded in to register YL_REG.

4.3.2 Pixel output

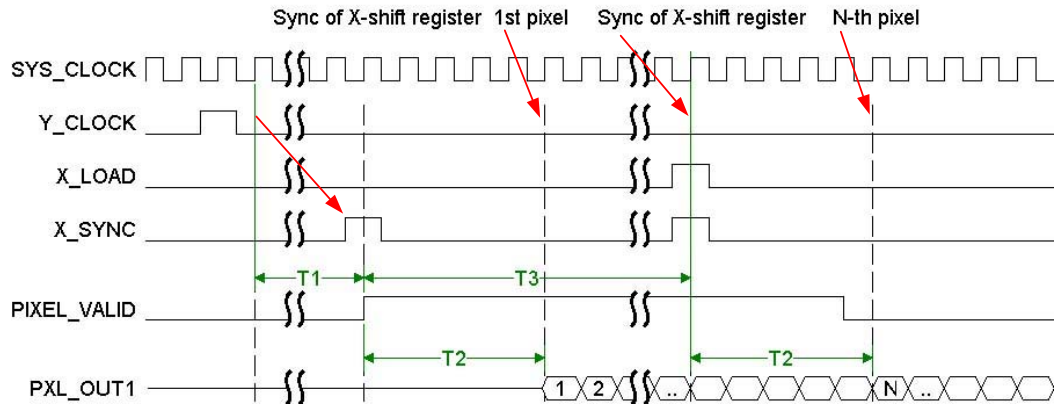


Figure 24: Pixel output

The pixel signal at the PXL_OUT1 output becomes valid after 5 SYS_CLOCK cycles when the internal X_SYNC (= start of PIXEL_VALID output or external X_LOAD pulse) pulse is asserted.

T_1 Row blanking time (see Table 24).
T_2 5 SYS_CLOCK cycles.
T_3 Time for new X-pointer position upload in X_REG register (see 4.6 for more details).

4.4 Synchronous shutter: multiple slope integration

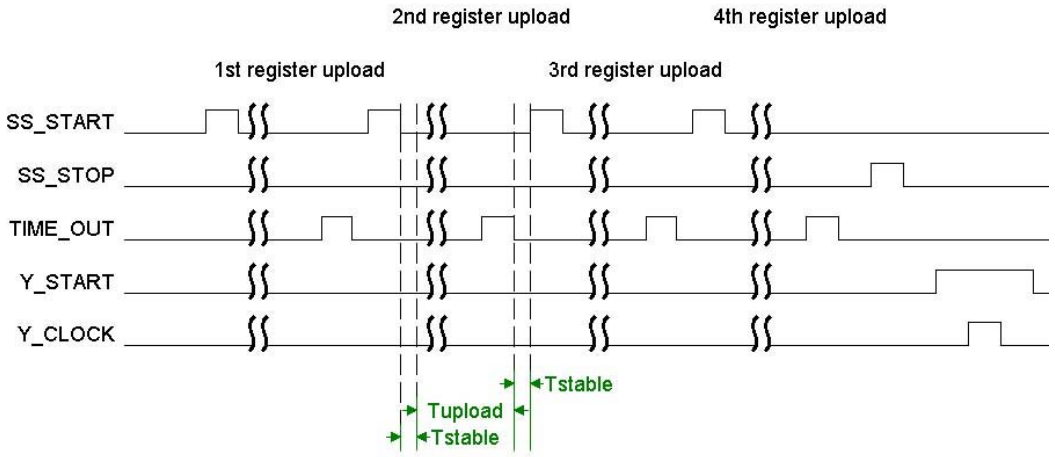


Figure 25: Multiple slope integration

Up to 4 different pixel reset voltages can be used during multiple slope operation in synchronous shutter mode. This is done by uploading new values to register bits KNEEPOINT_MSB/LSB/ENABLE before a new SS_START pulse is applied.
Bit KNEEPOINT_ENABLE should be set high to do a pixel reset with a lower voltage.
Bits KNEEPOINT_MSB/LSB/ENABLE should be set back to "0" before the SS_STOP pulse is applied. Every time an SS_START pulse is applied, the integration time counter is reset.

Table 25: Multiple slope register settings

	KNEEPOINT	
	MSB/LSB	**ENABLE**
Initial setup	*00*	*0*
1st register upload	*01*	*1*
2nd register upload	*10*	*1*
3th register upload	*11*	*1*
4th register upload	*00*	*0*

The register upload should be uploaded after time T_{stable}, otherwise the change will affect the SS-sequencer resulting in a bad pixel reset. T_{stable} depends on the granularity of the SS-sequencer clock (see Table 26).

Table 26: T_{stable} for different granularity settings

Granularity N_{GRAN}	**T_{stable} (µs) = 5 x N_{GRAN} x $T_{SYS\ CLOCK}$**	**GRAN_SS_SEQ MSB/LSB**
x 32	*160 x $T_{SYS\ CLOCK}$ = 4*	00
x 64	*320 x $T_{SYS\ CLOCK}$ = 8*	01
x 128	*640 x $T_{SYS\ CLOCK}$ = 16*	10

Granularity N_{GRAN}	T_{stable} (µs) = 5 x N_{GRAN} x $T_{SYS\ CLOCK}$	GRAN_SS_SEQ MSB/LSB
x 256	*1280 x $T_{SYS\ CLOCK}$ = 32*	11

T_{upload} depends on the interface mode used to upload the registers

Table 27: T_{upload} for different interface modes

Interface mode	T_{upload} (µs)
Parallel	*1*
Serial 3 Wire	*8 (2.5 MHz clock rate)*

4.5 Rolling shutter operation

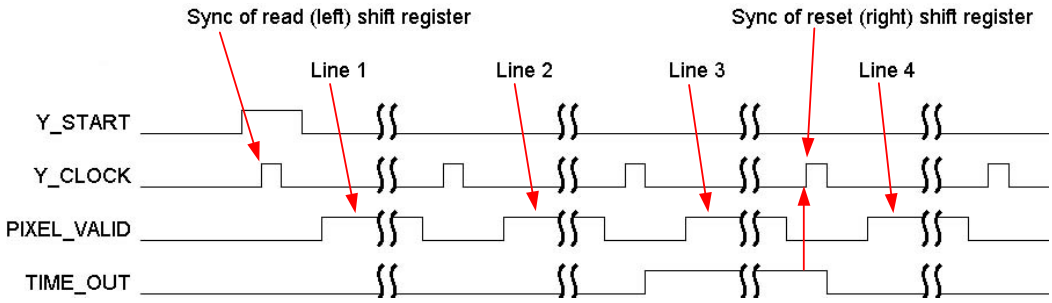


Figure 26: Rolling shutter operation

The integration of the light in the image sensor is done during readout of the other lines. The only difference with synchronous shutter is that the TIME_OUT pin is used to indicate when the Y_SYNC pulse for the right Y-shift-register (reset Y-shift register) is generated. This loads the right Y-shift-register with the pointer loaded in register YR_REG. The Y_SYNC pulse for the left Y-shift register (read Y-shift register) is generated with Y_START.
The INT_TIME register defines how many lines have to be counted before the Y_SYNC of the right Y-shift-register is generated, hence defining the integration time. See also chapter's 3.10.2 and 3.10.2.4 for a detailed description of the rolling shutter operation.

T_{int} Integration time [# lines] = register(NROF_LINES) - register(INT_TIME)

Note: For normal operation the values of the YL_REG and YR_REG registers are equal.

4.6 Windowing in X-direction

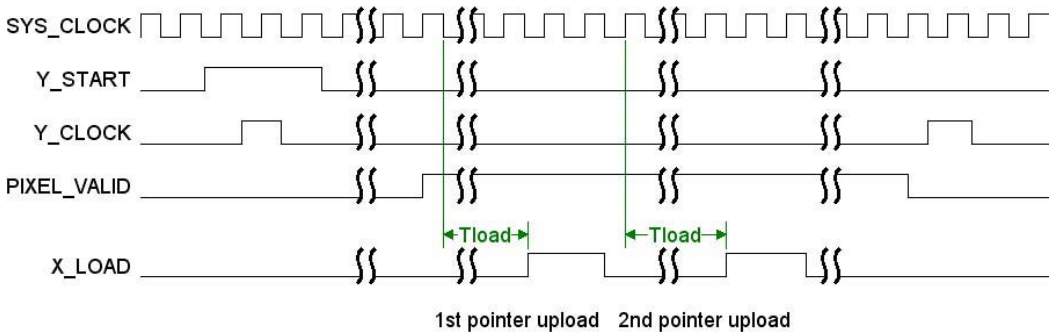


Figure 27: Windowing in the X-direction

An X_LOAD pulse overrides the internal X_SYNC signal, loading a new X-pointer (stored in the X_REG register) into the X-shift-register.

The X_LOAD pulse has to appear on the falling edge of SYS_CLOCK and has to remain 2 SYS_CLOCK cycles high overlapping 2 rising edges of SYS_CLOCK. On one of the 2 rising edges of SYS_CLOCK the new X-pointer is loaded.

T_{load} is the available time to upload the register and is defined from the previous register load to the rising edge of X_LOAD. It depends on the settling time of the register and the X-decoder.

The actual time to load the register is self depends on the interface mode that is used. The parallel interface is the fastest.

Table 28: T_{load} for different interfaces

Interface mode	T_{load} (µs)
Parallel interface	*1 (about 40 SYS_CLOCK cycles)*
Serial 3 Wire	*16 (at 2.5 MHz data rate)*

4.7 Windowing in Y-direction

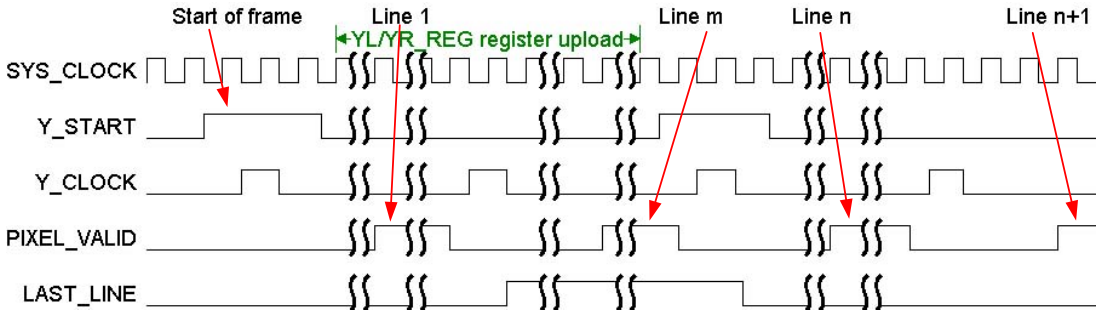


Figure 28: Windowing in the Y-direction

A new Y-pointer can be loaded into the Y-shift-register, by reapplying the Y_START pulse after loading a new Y-pointer value into the YL_REG and YR_REG registers.

Every time a Y_START pulse appears, a frame calibration of the output amplifier is done.

4.8 Initialization (start up behaviour)

To avoid any high current consumption at start up it is recommended to apply the SYS_CLOCK signal as soon as possible after or even before power on of the image sensor.

After power on of the image sensor it is recommended to apply SYS_RESET for minimal 5 SYS_CLOCK periods to assure a proper reset of the on-chip sequencer and timing circuitry. All internal register will be set to 0 after SYS_RESET is applied.

As all the IBIS5-A-1300 control signal are active high it is also recommended to apply a low level (before SYS_RESET occurs) to these pins at start up to avoid latch up.

5 Pin list

The IBIS5-A-1300 image sensor is packaged in a leadless ceramic carrier (LCC package). Table 29 is a list of all the pins and their function. In total, there are 84 pins.

Table 29: Pin list

Pin	Pin name	Pin type	Pin description
1	**P_DATA<8>**	Input	Digital input. Data parallel interface.
2	**P_WR**	Input	Digital input (active high). Parallel write.
3	**S_CLK**	Input	Digital input. Clock signal of serial interface.
4	**S_DATA**	Input	Digital input/output. Data of serial interface.
5	**S_EN**	Input	Digital input (active low). Enable of Serial-3-wire interface.
6	**SER_MODE**	Input	Digital input. Serial mode enable (1=Enable serial-3-wire, 0=disable).
7	**VDDC**	Supply	Analog supply voltage. Supply voltage of the pixel core [3.3V].
8	**VDDA**	Supply	Analog supply voltage. Analog supply voltage of the image sensor [3.3V].
9	**GNDA**	Ground	Analog ground. Analog ground of the image sensor.
10	**GNDD**	Ground	Digital ground. Digital ground of the image sensor.
11	**VDDD**	Supply	Digital supply voltage. Digital supply voltage of the image sensor [3.3V].
12	**IF_MODE**	Input	Digital input. Interface mode (1=parallel; 0=serial).
13	**DEC_CMD**	Input	Analog input. Biasing of decoder stage. Connect to VDDA with R = 50 kΩ and decouple with C=100nF to GNDA.
14	**Y_START**	Input	Digital input (active high). Start frame read out.
15	**Y_CLOCK**	Input	Digital input (active high). Line clock.
16	**LAST_LINE**	Output	Digital output. Generates a high level when the last line is read out.
17	**X_LOAD**	Input	Digital input (active high). Loads new X-position during read out.
18	**SYS_CLOCK**	Input	Digital input. System (pixel) clock (40 MHz).
19	**PXL_VALID**	Output	Digital output. Generates high level during pixel read out.
20	**SS_START**	Input	Digital input (active high). Start synchronous shutter operation.
21	**SS_STOP**	Input	Digital input (active high). Stop synchronous shutter operation.
22	**TIME_OUT**	Output	Digital output. Synchronous shutter: pulse when time-out reached. Can be used to trigger SS_STOP although both signals can't be tied together. Rolling shutter: pulse when second Y-sync appears.
23	**SYS_RESET**	Input	Digital input (active high). Global system reset.
24	**EL_BLACK**	Input	Digital input (active high). Enables electrical black in output amplifier.
25	**EOSX**	Output	Digital output. Diagnostic end-of-scan of X-register.

Pin	Pin name	Pin type	Pin description
26	**DAC_VHIGH**	Input	Analog reference input. Biasing of DAC for output dark level. Can be used to set output range of DAC. Default: Connect to VDDA with R = 0 Ω.
27	**DAC_VLOW**	Input	Analog reference input. Biasing of DAC for output dark level. Can be used to set output range of DAC. Default: Connect to GND A with R = 0 Ω.
28	**PXL_OUT1**	Output	Analog output. Analog pixel output 1.
29	**PXL_OUT2**	Output	Analog output. Analog pixel output 2. Leave not connected if not used.
30	**AMP_CMD**	Input	Analog input. Biasing of the output amplifier. Connect to VDDA with R = 50 kΩ and decouple with C=100nF to GNDA.
31	**COL_CMD**	Input	Analog input. Biasing of the column amplifiers. Connect to VDDA with R = 50 kΩ and decouple with C=100nF to GNDA.
32	**PC_CMD**	Input	Analog input. Pre-charge bias. Connect to VDDA with R = 25 kΩ and decouple with C=100nF to GNDA.
33	**VDDD**	Supply	Digital supply. Digital supply voltage of the image sensor [3.3V].
34	**GNDD**	Ground	Digital ground. Digital ground of the image sensor.
35	**GNDA**	Ground	Analog ground. Analog ground of the image sensor.
36	**VDDA**	Supply	Analog supply voltage. Analog supply voltage of the image sensor [3.3V].
37	**VDDC**	Supply	Analog supply voltage. Supply voltage of the pixel core [3.3V].
38	**P_DATA<0>**	Input	Digital input. Data parallel interface (LSB).
39	**P_DATA<1>**	Input	Digital input. Data parallel interface.
40	**P_DATA<2>**	Input	Digital input. Data parallel interface.
41	**P_DATA<3>**	Input	Digital input. Data parallel interface.
42	**P_DATA<4>**	Input	Digital input. Data parallel interface.
43	**P_DATA<5>**	Input	Digital input. Data parallel interface.
44	**P_DATA<6>**	Input	Digital input. Data parallel interface.
45	**P_DATA<7>**	Input	Digital input. Data parallel interface.
46	**SI2_ADDR<0>**	Input	Unused interface inputs. Tie to GNDD.
47	**SI2_ADDR<1>**	Input	
48	**SI2_ADDR<2>**	Input	
49	**SI2_ADDR<3>**	Input	
50	**SI2_ADDR<4>**	Input	
51	**GNDAB**	Supply	Analog supply voltage. Anti-blooming ground.
52	**VDDR_RIGHT**	Supply	Analog supply voltage. Variable reset voltage (multiple slope operation). Decouple with 1uF to GNDA.
53	**ADC_VLOW**	Input	Analog reference input. ADC low reference voltage. Default: Connect to GNDA with R = 360 Ω and decouple with C=100nF to GNDA.
54	**ADC_GNDA**	Ground	Analog ground. ADC analog ground.
55	**ADC_VDDA**	Supply	Analog supply voltage. ADC analog supply voltage [3.3V].
56	**ADC_GNDD**	Ground	Digital ground. ADC digital ground.
57	**ADC_VDDD**	Supply	Digital supply voltage. ADC digital supply voltage [3.3V].

Pin	Pin name	Pin type	Pin description
58	**ADC_CLOCK**	Input	Digital input. ADC clock (40 MHz).
59	**ADC_OUT<9>**	Output	Digital output. ADC data output (MSB).
60	**ADC_OUT<8>**	Output	Digital output. ADC data output.
61	**ADC_OUT<7>**	Output	Digital output. ADC data output.
62	**ADC_OUT<6>**	Output	Digital output. ADC data output.
63	**ADC_OUT<5>**	Output	Digital output. ADC data output.
64	**ADC_OUT<4>**	Output	Digital output. ADC data output.
65	**ADC_OUT<3>**	Output	Digital output. ADC data output.
66	**ADC_OUT<2>**	Output	Digital output. ADC data output.
67	**ADC_OUT<1>**	Output	Digital output. ADC data output.
68	**ADC_OUT<0>**	Output	Digital output. ADC data output (LSB).
69	**ADC_IN**	Input	Analog input. ADC analog input.
70	**ADC_CMD**	Input	Analog input. Biasing of the input stage of the ADC. Connect to ADC_VDDA with R = 50 kΩ and decouple with C=100nF to ADC_GNDA.
71	**ADC_VDDD**	Supply	Digital supply voltage. ADC digital supply voltage [3.3V].
72	**ADC_GNDA**	Ground	Analog ground. ADC analog ground.
73	**ADC_GNDD**	Ground	Digital ground. ADC digital ground.
74	**ADC_VDDA**	Supply	Analog supply voltage. ADC analog supply voltage [3.3V].
75	**ADC_VHIGH**	Input	Analog reference input. ADC high reference voltage. Default: Connect to VDDA with R = 90 Ω and decouple with C=100nF to GNDA.
76	**VDDR_LEFT**	Supply	Analog supply voltage. High reset level [4.5V].
77	**VDDH**	Supply	Analog supply voltage. High supply voltage for HOLD switches in the image core [4.5V]
78	**P_DATA<15>**	Input	Digital input. Data parallel interface (MSB).
79	**P_DATA<14>**	Input	Digital input. Data parallel interface.
80	**P_DATA<13>**	Input	Digital input. Data parallel interface.
81	**P_DATA<12>**	Input	Digital input. Data parallel interface.
82	**P_DATA<11>**	Input	Digital input. Data parallel interface.
83	**P_DATA<10>**	Input	Digital input. Data parallel interface.
84	**P_DATA<9>**	Input	Digital input. Data parallel interface.

REMARKS:

1. All pins with the same name can be connected together.
2. All digital input are active high (unless mentioned otherwise).
3. Digital inputs that are not used should be tied to GND.

6 Pad position and Packaging

6.1 Bare die

The IBIS5-A-1300 image sensor has 84 pins, 21 pins on every edge. The die size from pad-edge to pad-edge (without scribe-line) is:

10048.55 µm (x) by 9240.30 µm (y)

Scribe lines will take about 100 to 150 µm extra on each side.

Pin 1 is located in the middle of the left side, indicated by a "1" on the layout. A logo and some identification tags can be found on the top right of the die.

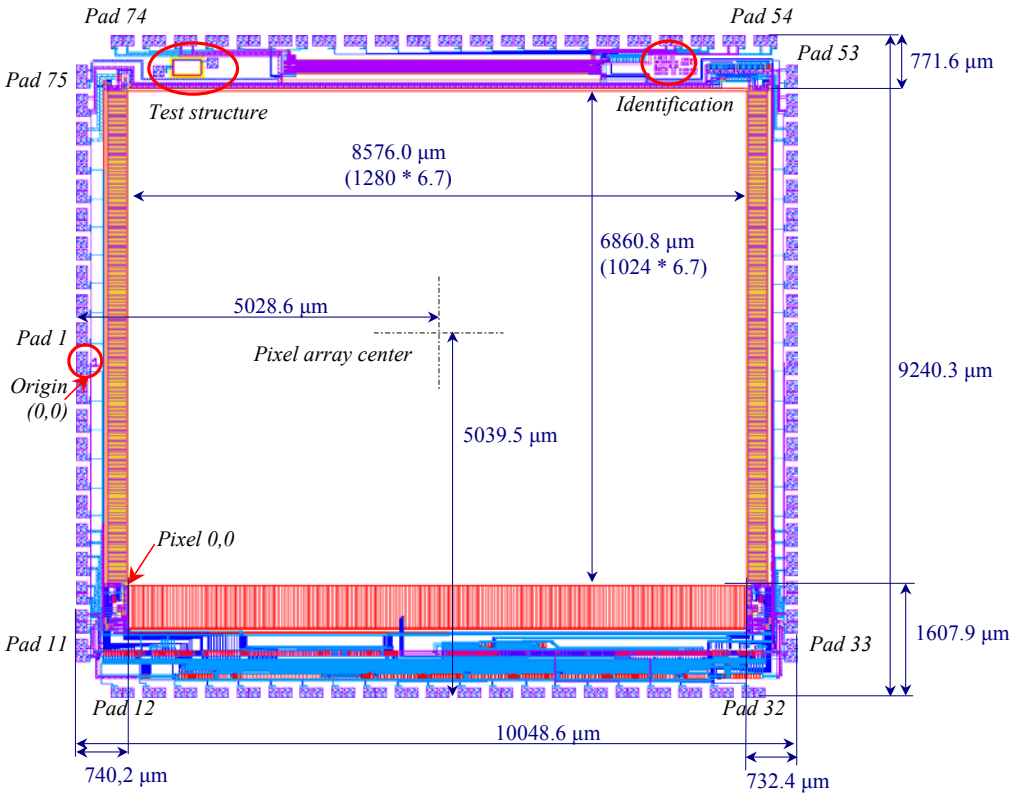


Figure 29: IBIS5-A-1300 bare die dimensions

6.2 IBIS5-A-1300 in 84-pins LCC package

6.2.1 Technical drawing of the 84-pins LCC package

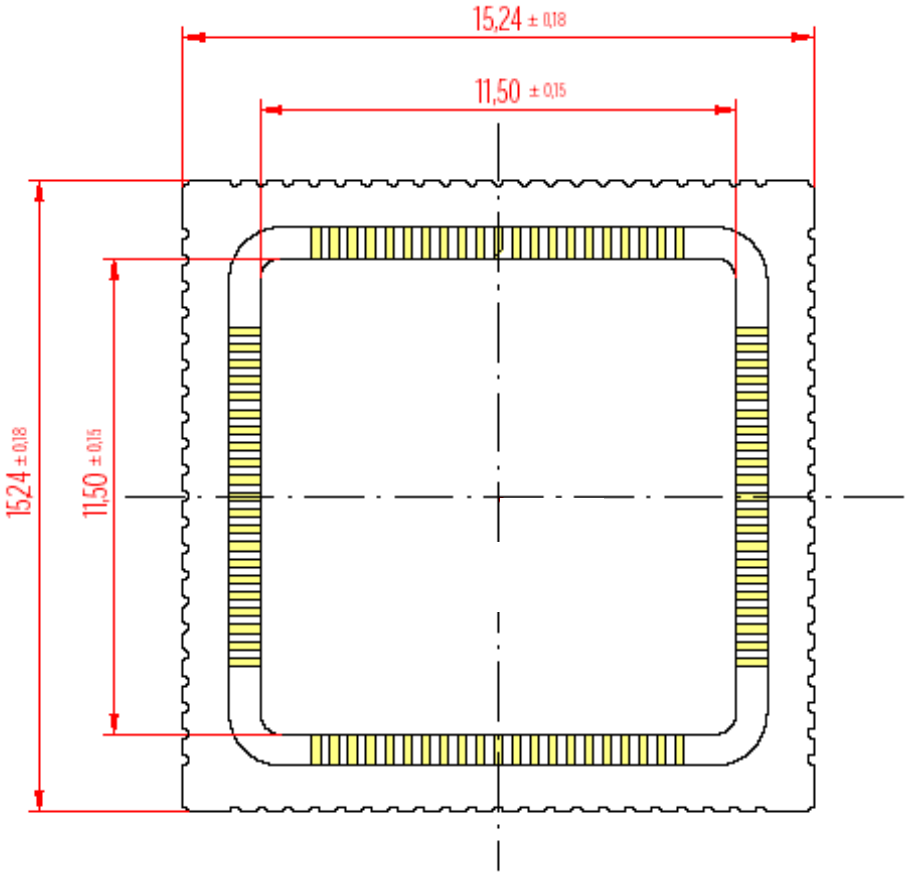


Figure 30: Top view of the 84-pins LCC package (all dimensions in mm).

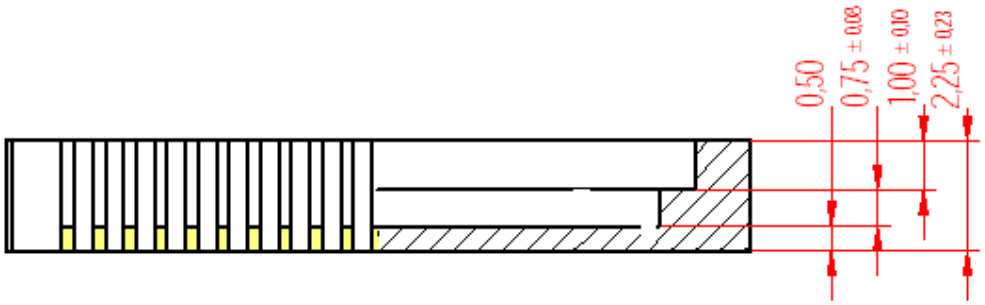


Figure 31: Side view of the 84-pins LCC package (all dimensions in mm).

Table 30: Side view dimensions.

Dimension	Description	(inch)			(mm)		
		Min	Typ	Max	Min	Typ	Max
A	Glass (thickness) – mono	0.020	0.022	0.024	0.500	0.550	0.600
B	Cavity (depth)	0.060	0.069	0.078	1.520	1.750	1.980
C	Die – Si (thickness) – mono		0.029			0.740	
D	Bottom layer (thickness)		0.020			0.500	
E	Die attach-bondline (thickness)	0.001	0.002	0.004	0.030	0.060	0.090
F	Glass attach-bondline (thickness)	0.001	0.003	0.004	0.030	0.070	0.110
G	Imager to lid-outer surface		0.062			1.570	
H	Imager to lid-inner surface		0.037			0.950	
J	Imager to seating plane of package	0.050	0.051	0.052	1.270	1.300	1.330

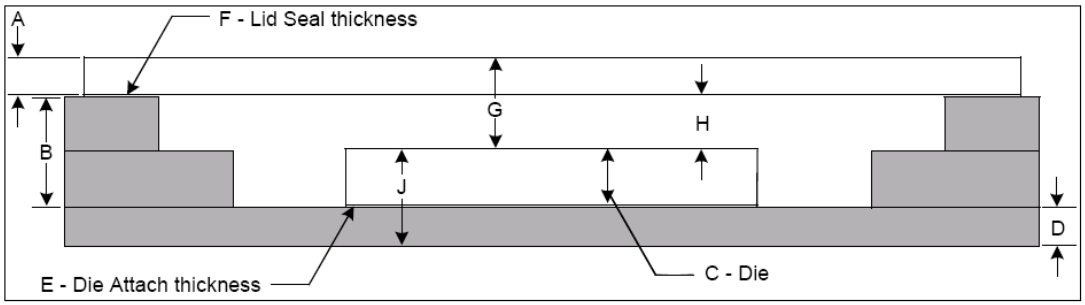


Figure 32: Side view dimensions.

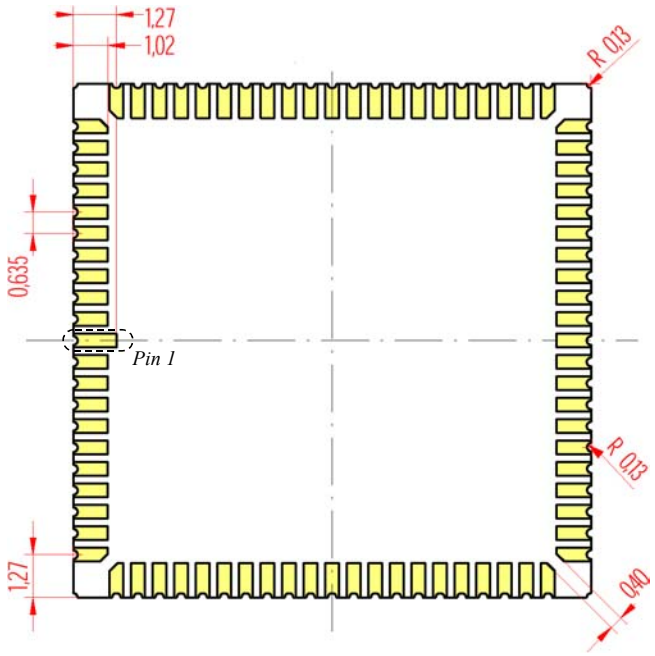


Figure 33: Bottom view of the 84-pins LCC package (all dimensions in mm).

6.2.2 Bonding of the IBIS5-A-1300 sensor in the 84-pins LCC package

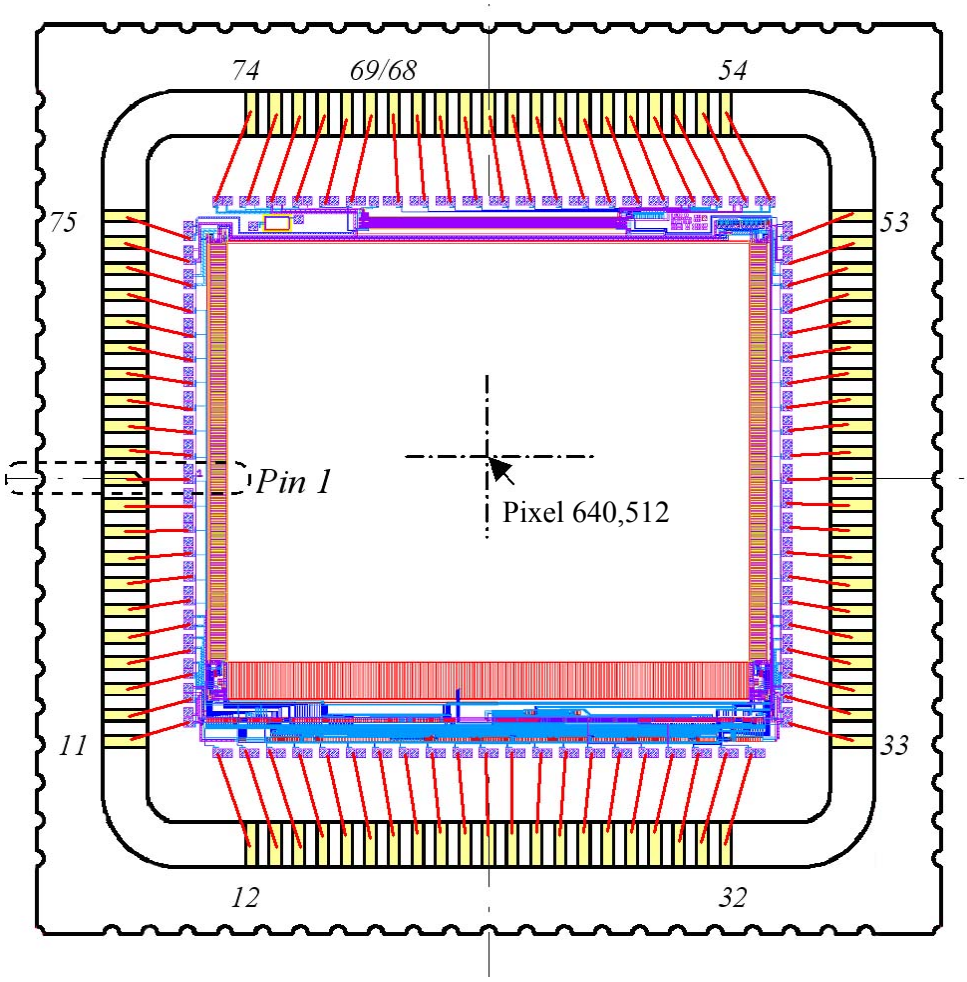


Figure 34: Bonding of the IBIS5-A-1300 in the 84-pins LCC package.

6.2.3 Die placement of the IBIS5-A-1300 in the 84-pins LCC package

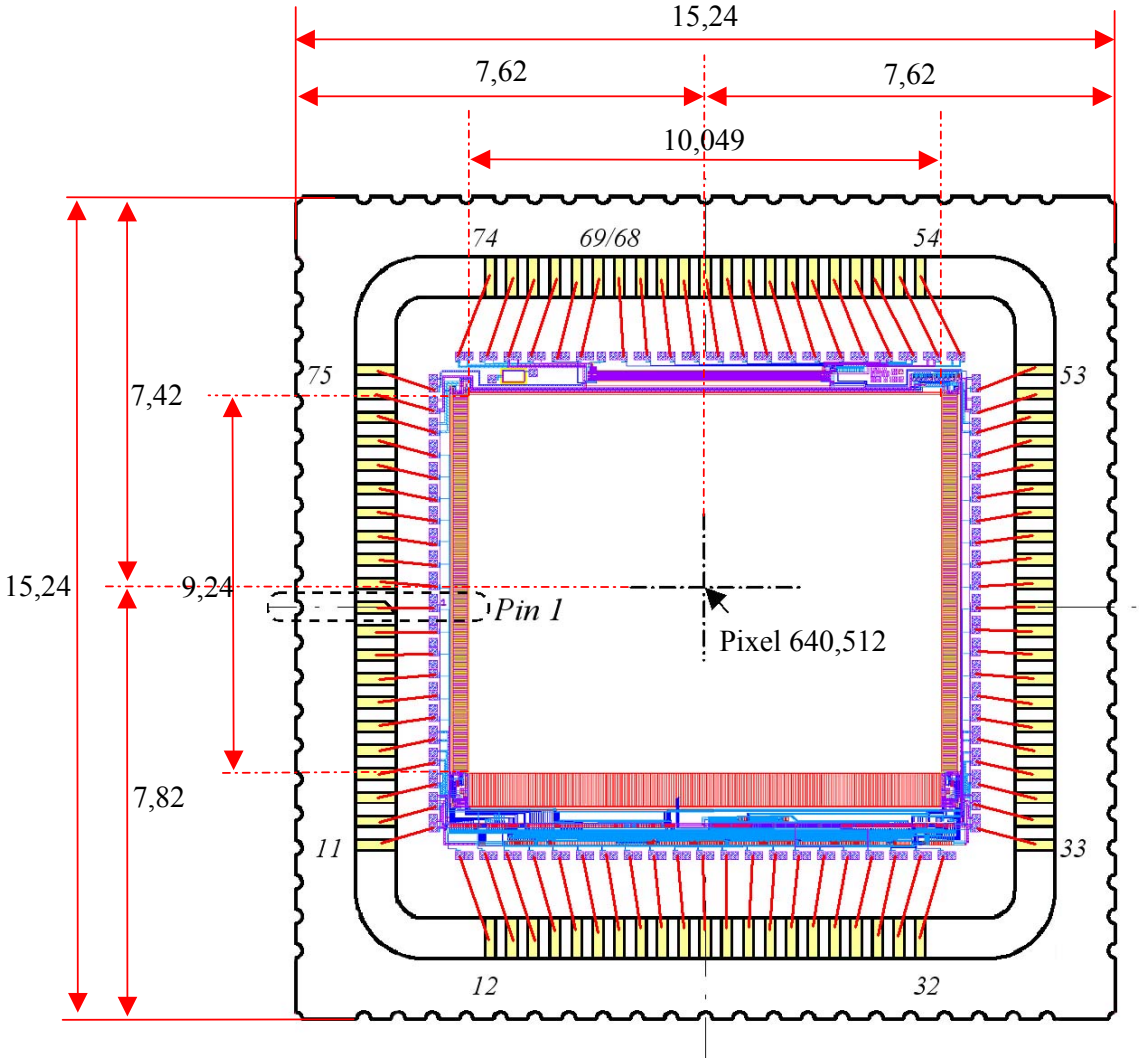


Figure 35: Die placement of the IBIS5-A-1300 in the 84-pins LCC package (all dimensions in mm).

Tolerance on the die placement in X- and Y-directions is maximal +/- 50 um.

6.3 Cover glass

6.3.1 Monochrome sensor

A D263 glass lid (which has a refraction index of 1.52) will be used as protection glass lid on top of the IBIS5-A-1300 monochrome sensors. Figure 36 shows the transmission characteristics of the D263 glass.

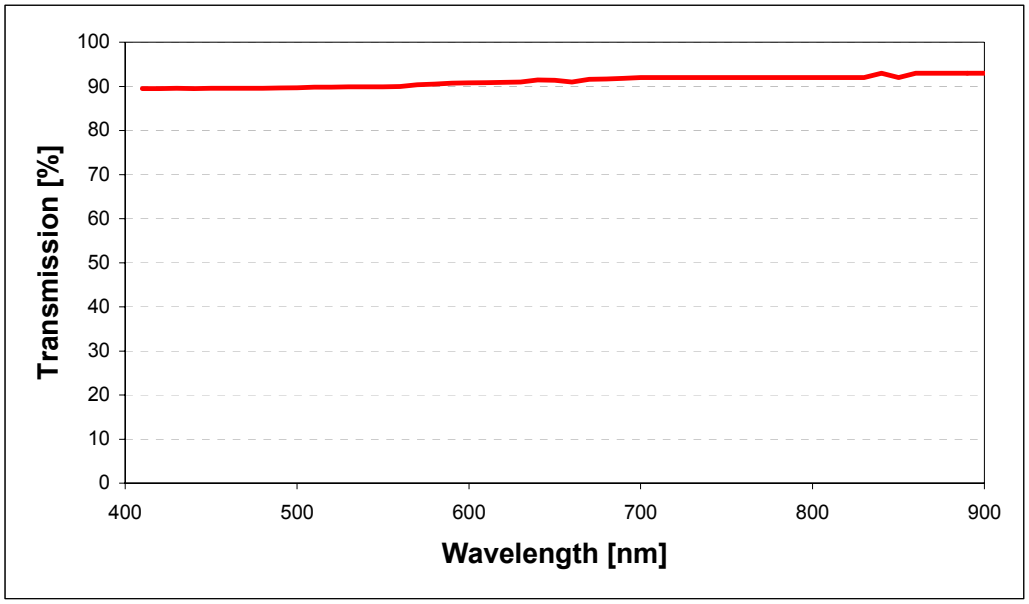


Figure 36: Transmission characteristics of the D263 glass used as protective cover for the IBIS5-A-1300 sensors.

6.3.2 Color sensor

A S8612 glass lid (which has a refraction index of 1.55) will be used as NIR cut-off filter on top of the IBIS5-A-1300-C color image sensor. Figure 37 shows the transmission characteristics of the S8612 glass.

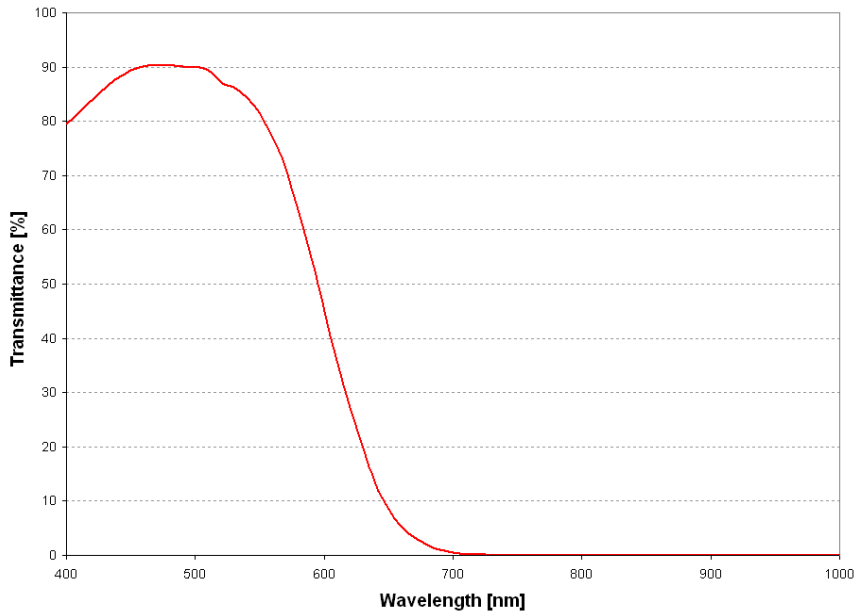


Figure 37: Transmission characteristics of the S8612 glass used as protective cover for the IBIS5-A-1300 sensors

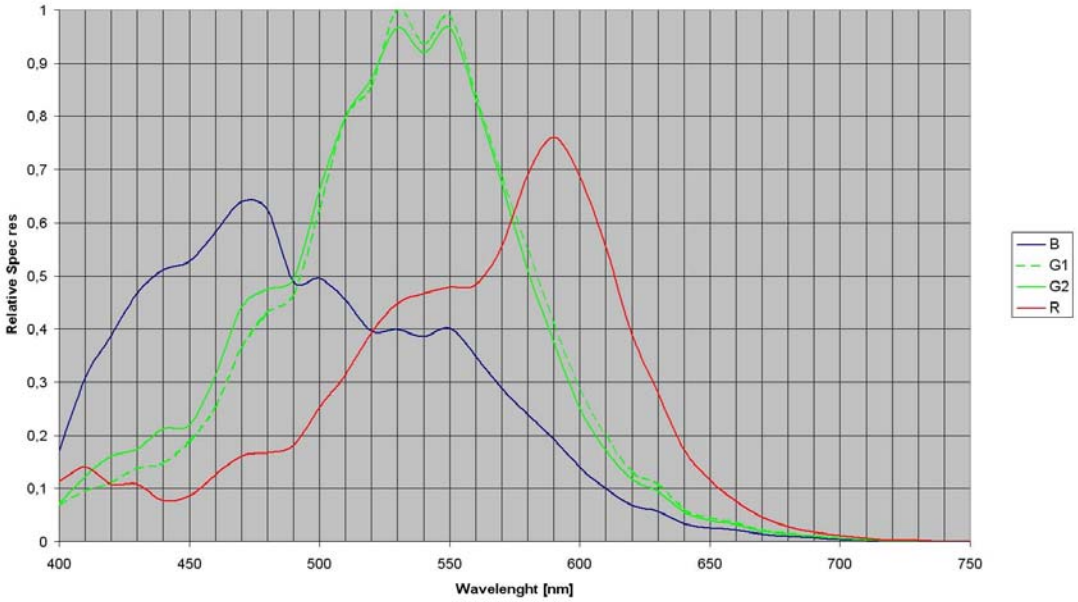


Figure 38: Color response of the IBIS5-A-1300-C in combination with the S8612 NIR filter

7 Storage and handling

7.1 Storage conditions

Table 31: Storage conditions.

Description	Minimum	Maximum	Units	Conditions
Temperature	-10	66	°C	@ 15% RH
Temperature	-10	38	°C	@ 86% RH

Note: RH = Relative Humidity

7.2 Handling and solder precautions

Special care should be given when soldering image sensors with color filter arrays (RGB color filters), onto a circuit board, since color filters are sensitive to high temperatures. Prolonged heating at elevated temperatures may result in deterioration of the performance of the sensor. The following recommendations are made to ensure that sensor performance is not compromised during end-user's assembly processes.

Board Assembly:
Device placement onto boards should be done in accordance with strict ESD controls for Class 0, JESD22 Human Body Model, and Class A, JESD22 Machine Model devices. Assembly operators should always wear all designated and approved grounding equipment; grounded wrist straps at ESD protected workstations are recommended including the use of ionized blowers. All tools should be ESD protected.

Manual Soldering:
When a soldering iron is used the following conditions should be observed:

- Use a soldering iron with temperature control at the tip.
- The soldering iron tip temperature should not exceed 350°C.
- The soldering period for each pin should be less than 5 seconds.

Reflow Soldering:
Figure 39 shows the maximum recommended thermal profile for a reflow soldering system. If the temperature/time profile exceeds these recommendations damage to the image sensor may occur.

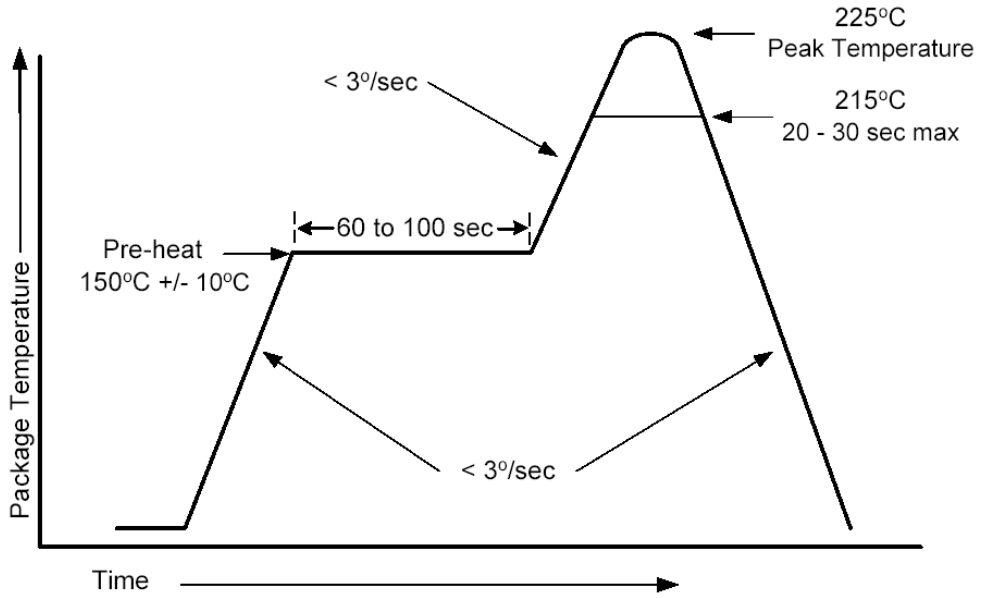


Figure 39: Reflow soldering temperature / time profile

Precautions and cleaning:

Avoid spilling solder flux on the cover glass; bare glass and particularly glass with antireflection filters may be adversely affected by the flux. Avoid mechanical or particulate damage to the cover glass.

It is recommended that isopropyl alcohol (IPA) is used as a solvent for cleaning the image sensor glass lid. When using other solvents, it should be confirmed beforehand whether the solvent will dissolve the package and/or the glass lid or not.

8 Ordering Information

Table 32: FillFactory and Cypress part numbers

FillFactory Part Number	Cypress Semiconductor Part Number
IBIS5-A-1300-M-1	CYII5SM1300AA-HBC (Preliminary)
IBIS5-A-1300-M-2	CYII5SM1300AA-QBC (Preliminary)
IBIS5-A-1300-C-1	CYII5SC1300AA-HAC (Preliminary)
IBIS5-A-1300-C-2	CYII5SC1300AA-QAC (Preliminary)

Disclaimer

FillFactory image sensors are only warranted to meet the specifications as described in the production data sheet. FillFactory reserves the right to change any information contained herein without notice.

Please contact info@FillFactory.com for more information.

Revision changes

No.	Date	Description of revision
1.0	22-Jun-04	Origination.
1.1	16-Sep-04	3.10.2.g. Additional explanation about the test pattern use. 5 Pin list. Recommended values of pins 30, 31, 76 and 77 corrected. 6.3 Refraction index of both color and mono glass lid added.
1.2	24-Sep-04	3.8.4 Table 17. ADC reference voltages updated.
1.3	04-Jan-2005	Added Cypress equivalent part numbers, part ordering table Added Cypress Document # 38-05710 Rev ** in the document footer.

APPENDIX A: IBIS5 evaluation system

For evaluating purposes an IBIS5 evaluation kit is available.

The IBIS5 evaluation kit consists of a multifunctional digital board (memory, sequencer and IEEE 1394 Fire Wire interface) and an analog image sensor board.

Visual Basic software (under Win 2000 or XP) allows the grabbing and display of images and movies from the sensor. All acquired images and movies can be stored in different file formats (8 or 16-bit). All setting can be adjusted on the fly to evaluate the sensors specs. Default register values can be loaded to start the software in a desired state.

Figure 40: Content of the IBIS5 evaluation kit

Please contact FillFactory (info@Fillfactory.com) for more information on the evaluation kit.

APPENDIX B: Frequently Asked Questions

Q: ***How does the dual (multiple) slope extended dynamic range mode works?***

A: Dual slope is a method to extend the dynamic range of a normally linear-transfer imager, by combining the images taken with a long integration time (dark areas of a scene) and a short integration time (bright areas of a scene) into one image. The resulting electro-optical transfer curve is bi-linear. Multiple slope is an extension of it, resulting in a multi-linear transfer curve with multiple knee points.

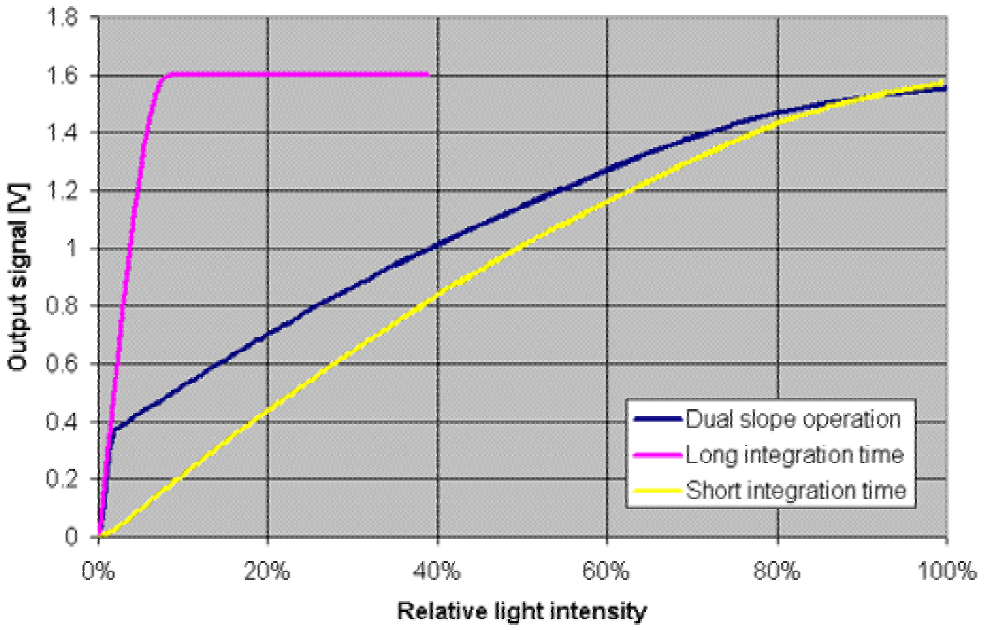


Figure 41: Double slope response

Please look at our website to find some pictures taken with the IBIS4-1300 in double slope mode on: http://www.fillfactory.be/htm/technology/htm/dual-slope.htm. Please contact support@fillfactory.com for additional application notes to use the multiple slope extended dynamic range mode with the IBIS5-A-1300 sensor.

Document History Page

Document Title: IBIS5A-1300 1.3M Pixel DualShutter Mode CMOS Image Sensor

Document Number: 38-05710

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	310213	See ECN	SIL	Initial Cypress release

(EOD)