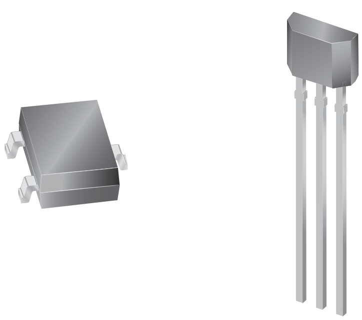
Chopper-Stabilized Unipolar Hall-Effect Switches

Features and Benefits

- Chopper stabilization
  - Superior temperature stability
  - Extremely low switchpoint drift
  - Insensitive to physical stress
- Reverse battery protection
- Output short circuit protection
- Solid state reliability
- Small size
- Robust EMC capability
- High ESD ratings (HBM)

Packages: 3 pin SOT23W (suffix LH), and 3 pin SIP (suffix UA)



Not to scale

Description

The A3241 and A3242 integrated circuits are unipolar Hall-effect switches with digital outputs. These devices are suited for operation over extended temperature ranges, up to +150°C. Superior high-temperature performance is made possible through an Allegro® patented dynamic offset cancellation, which reduces the residual offset voltage normally caused by device overmolding, temperature excursions, and thermal stress.

The A3241 and A3242 Hall-effect switches include the following on a single silicon chip: voltage regulator, Hall-voltage generator, small-signal amplifier, chopper stabilization, Schmitt trigger, and a short circuit protected open-drain output. Advanced BiCMOS wafer fabrication processing is used to take advantage of low-voltage requirements, component matching, very low input-offset errors, and small component geometries.

The integrated voltage regulator permits operation from 3.6 to 24 V. The unipolar family members operate with a sufficient south polarity field only, turning off in the absence of such a south polarity field.

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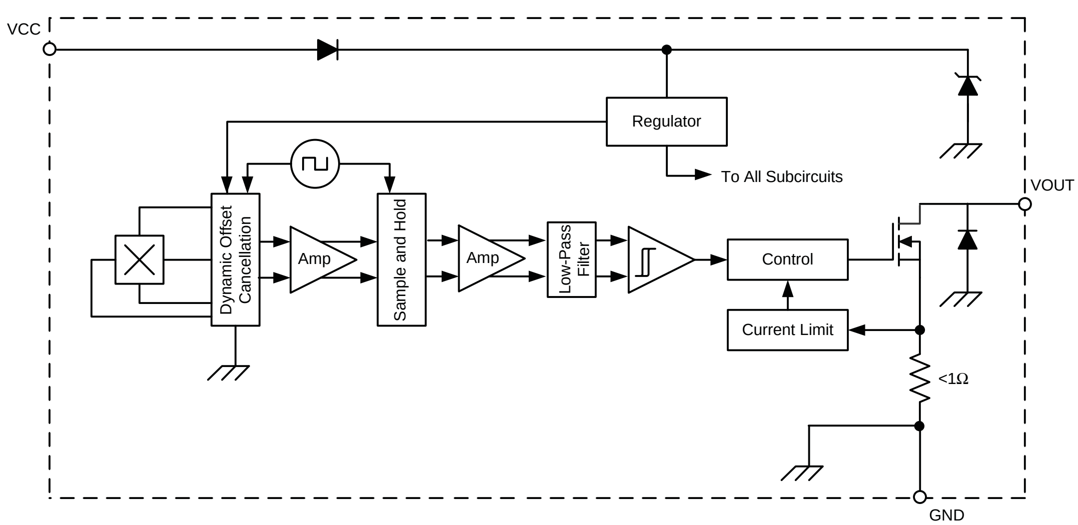
Functional Block Diagram



Description (continued)

The A3241 and A3242 are rated for operation between the ambient temperatures –40°C and 85°C for the E temperature range, and –40°C to 150°C for the L temperature range. The small geometries of the BiCMOS process allow these devices to be provided in ultrasmall packages. The package styles available provide magnetically optimized solutions for most applications. Package LH is an SOT23W, a miniature low-profile surface-mount package, while package UA is a three-lead ultramini SIP for through-hole mounting. Each package is lead (Pb) free, with 100% matte tin plated leadframes.

Selection Guide

Part Number	Packing[1]	Mounting	Ambient, T_A (°C)	$B_{RP(MIN)}$ (G)	$B_{OP(MAX)}$ (G)
~~A3241ELHLT-T~~[3]	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	–40 to 85	40	135
~~A3241EUA-T~~[3]	Bulk, 500 pieces/bag	3-pin SIP through hole			
~~A3241LLHLT-T~~[3]	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	–40 to 150		
~~A3241LUA-T~~[3]	Bulk, 500 pieces/bag	3-pin SIP through hole			
~~A3242ELHLT-T~~[2]	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	–40 to 85	110	200
~~A3242EUA-T~~[3]	Bulk, 500 pieces/bag	3-pin SIP through hole			
A3242LLHLT-T	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	–40 to 150		
~~A3242LUA-T~~[2]	Bulk, 500 pieces/bag	3-pin SIP through hole			

[1]Contact Allegro for additional packing options.

[2]Variant is in production but has been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: May 4, 2009.

[3]Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change May 4, 2009. Deadline for receipt of LAST TIME BUY orders is November 4, 2009.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		28	V
Reverse-Supply Voltage	V_{RCC}		–18	V
Reverse-Supply Current	I_{RCC}		–2	mA
Output Off Voltage	V_{OUT}		28	V
Output Current	$I_{OUTSINK}$		Internally Limited	–
Magnetic Flux Density	B		Unlimited	G
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
		Range L	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

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OPERATING CHARACTERISTICS valid over full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Electrical Characteristics							
Supply Voltage[1]	V_{CC}	Operating, T_J < 165°C		3.6	–	24	V
Output Leakage Current	I_{OUTOFF}	V_{OUT} = 24 V, B < B_{RP}		–	–	10	µA
Output On Voltage	$V_{OUT(SAT)}$	I_{OUT} = 20 mA, B > B_{OP}		–	–	500	mV
Output Current Limit	I_{OM}	B > B_{OP}		30	–	60	mA
Power-On Time	t_{PO}	V_{CC} > $V_{CC(MIN)}$		–	–	50	µs
Chopping Frequency	f_c			–	200	–	kHz
Output Rise Time[2]	t_r	R_{LOAD} = 820 Ω, C_S = 20 pF		–	–	1	µs
Output Fall Time[2]	t_f	R_{LOAD} = 820 Ω, C_S = 20 pF		–	–	1	µs
Supply Current	I_{CCON}	B > B_{OP}		–	1.5	3.5	mA
	I_{CCOFF}	B < B_{RP}		–	1.5	3.5	mA
Reverse Battery Current	I_{RCC}	V_{RCC} = –18 V		–	–	–2	mA
Supply Zener Clamp Voltage	$V_{ZSupply}$	I_{CC} = 6.5 mA; T_A = 25°C		28	–	–	V
Supply Zener Current[3]	$I_{ZSupply}$	V_S = 28 V		–	–	6.5	mA
Magnetic Characteristics[4]							
Operate Point	B_{OP}	A3241		50	95	135	G
		A3242		120	150	200	G
Release Point	B_{RP}	A3241		40	70	110	G
		A3242		110	125	190	G
Hysteresis	B_{HYS}	A3241	$B_{OP} – B_{RP}$	10	25	42	G
		A3242		10	25	40	G

[1] Maximum voltage must be adjusted for power dissipation and junction temperature, see *Power Derating* section.
[2] C_S = oscilloscope probe capacitance.
[3] Maximum current limit is equal to the maximum $I_{CC(MAX)}$ + 3 mA.
[4] Magnetic flux density, B, is indicated as a negative value for north-polarity magnetic fields, and as a positive value for south-polarity magnetic fields. This so-called algebraic convention supports arithmetic comparison of north and south polarity values, where the relative strength of the field is indicated by the absolute value of B, and the sign indicates the polarity of the field (for example, a –100 G field and a 100 G field have equivalent strength, but opposite polarity).

DEVICE QUALIFICATION PROGRAM

Contact Allegro for information.

EMC (Electromagnetic Compatibility) REQUIREMENTS

Contact Allegro for information.

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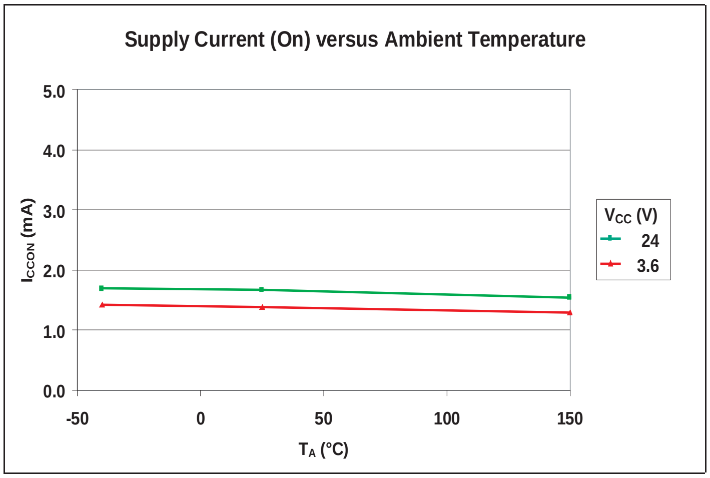
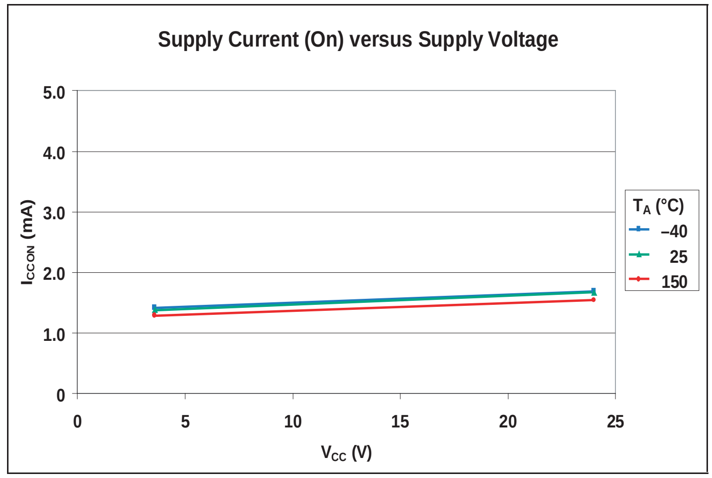
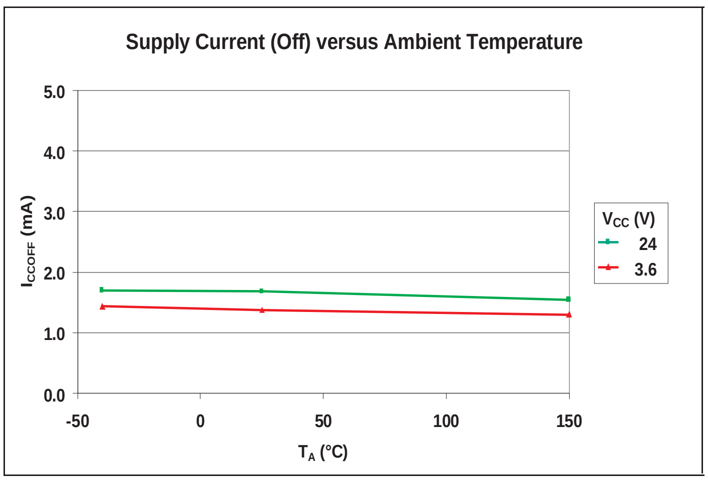
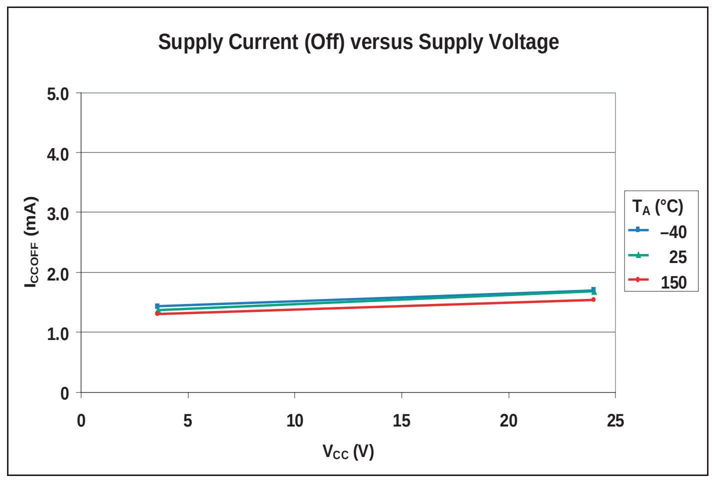
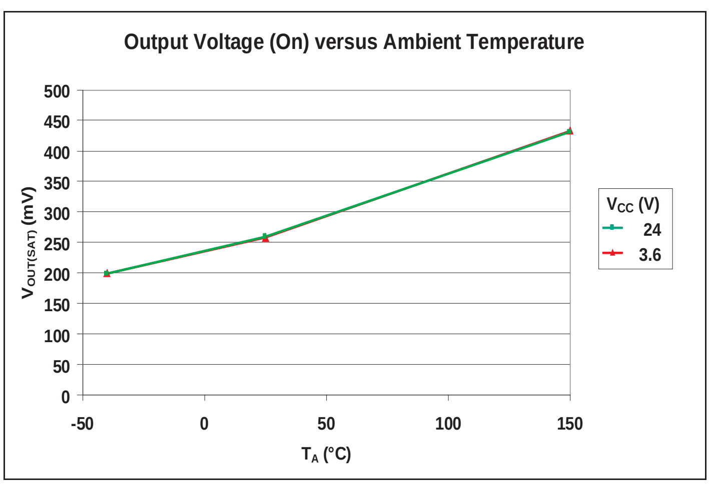
Characteristic Data

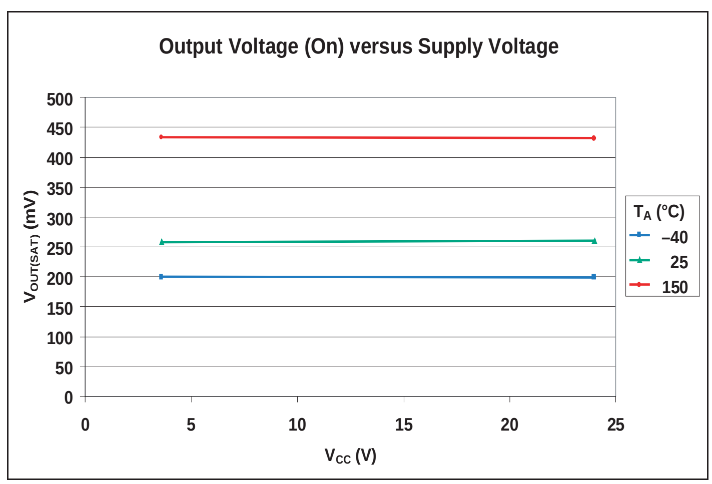












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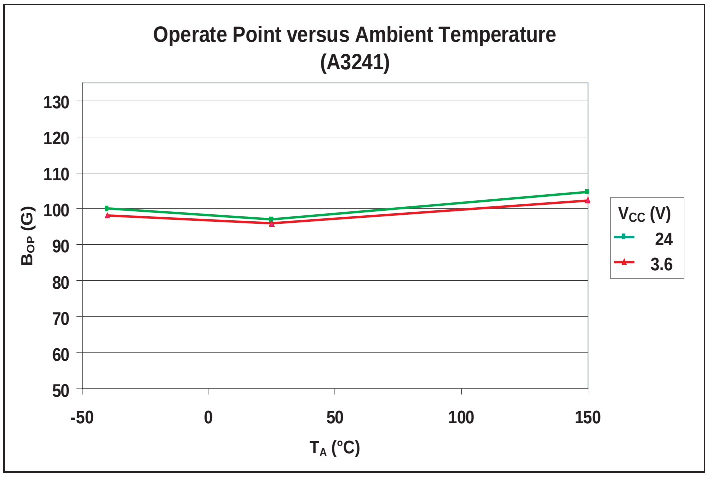

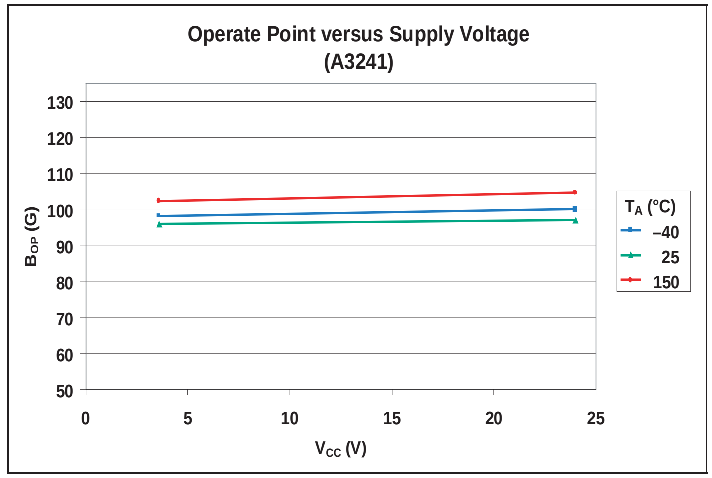

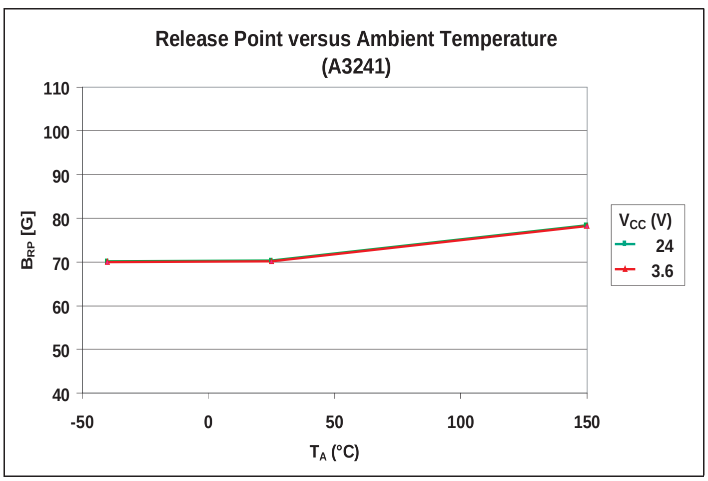

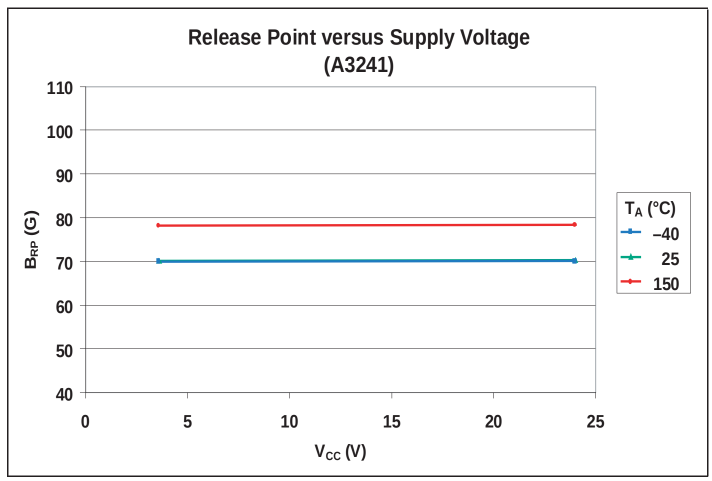

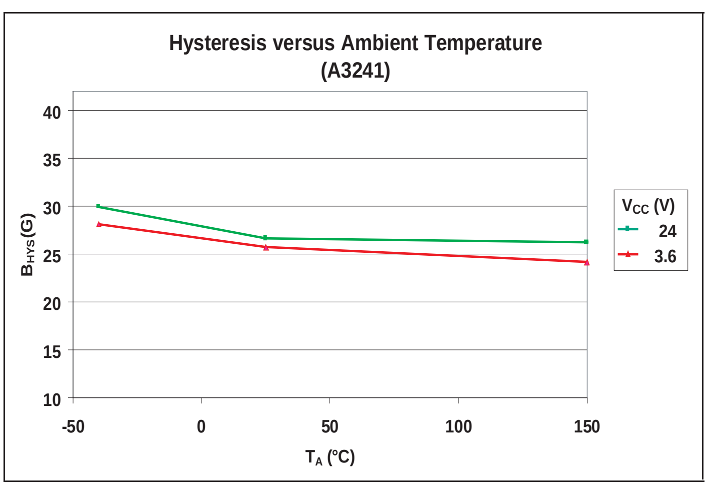

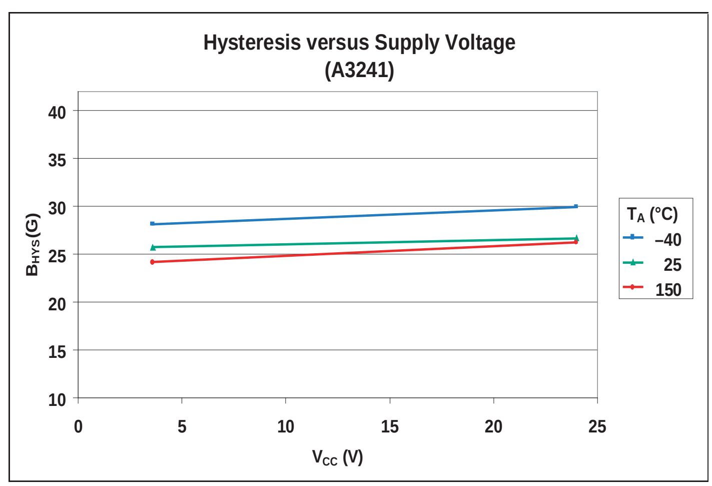

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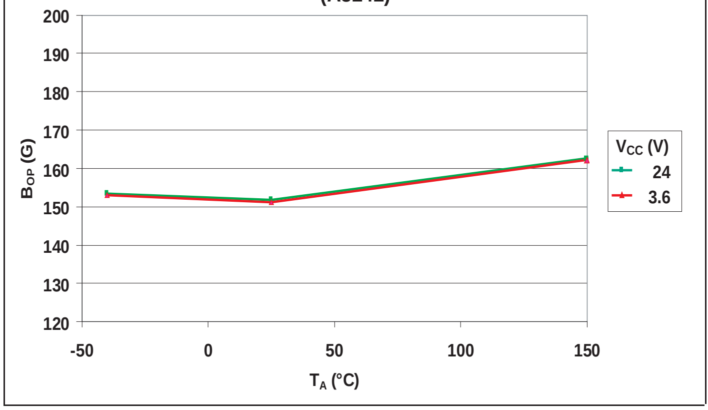
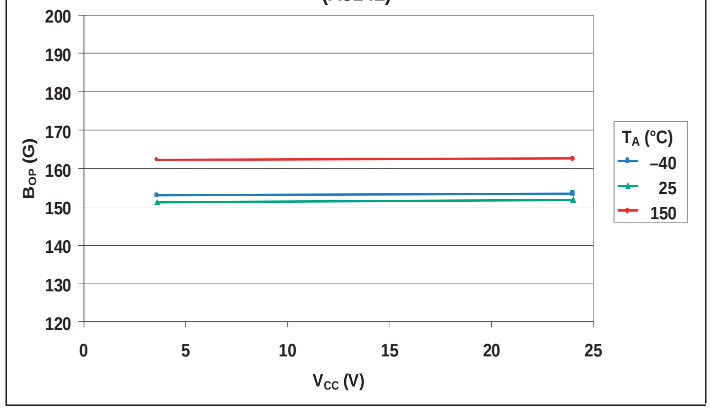
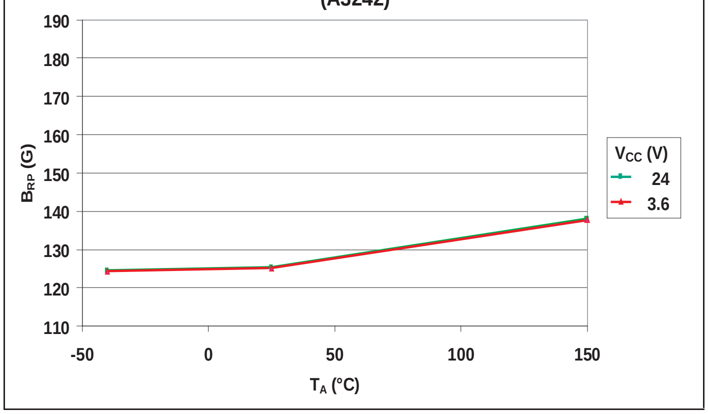
Operate Point versus Ambient Temperature (A3242)



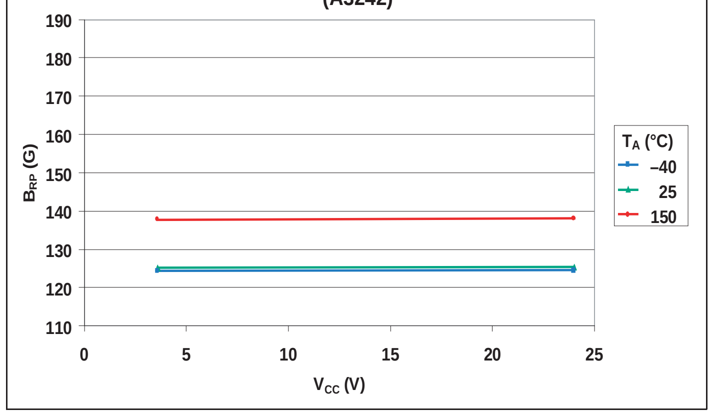
Operate Point versus Supply Voltage (A3242)



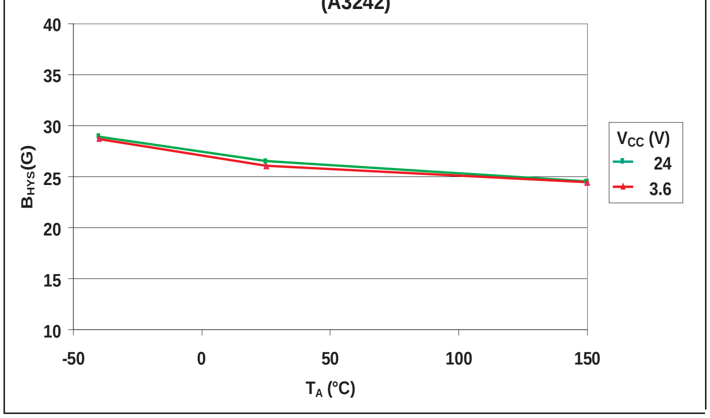
Release Point versus Ambient Temperature (A3242)



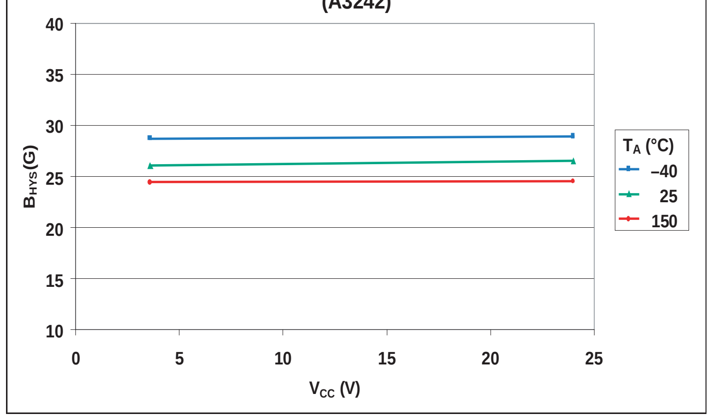
Release Point versus Supply Voltage (A3242)



Hysteresis versus Ambient Temperature (A3242)



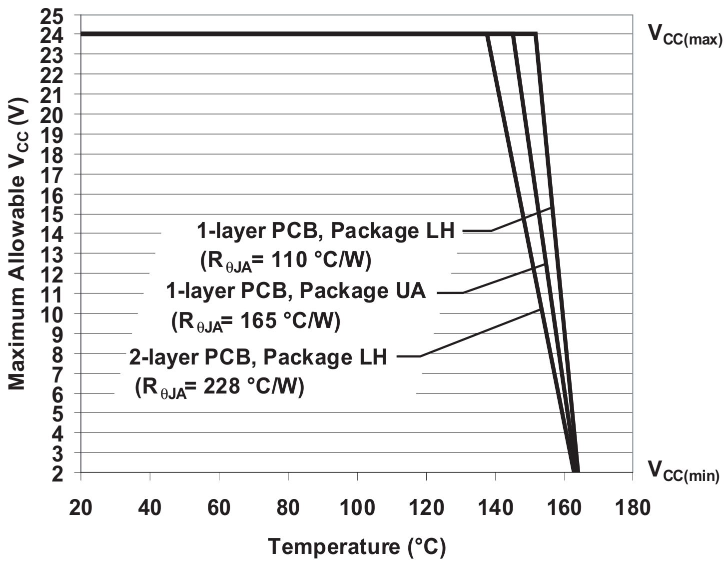
Hysteresis versus Supply Voltage (A3242)



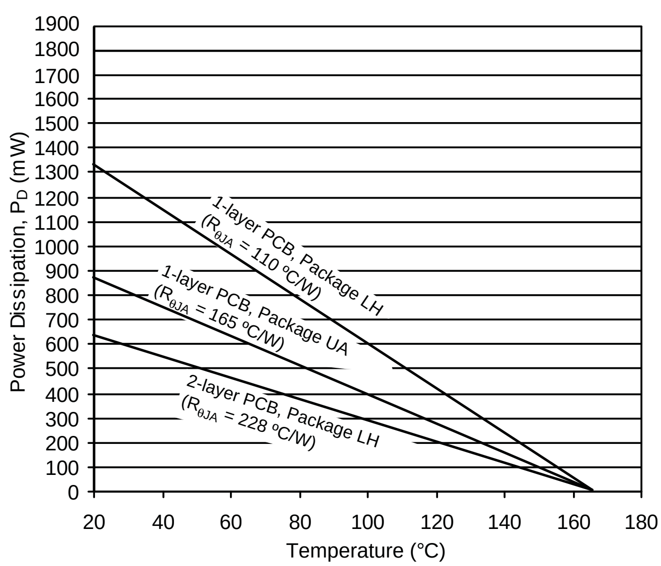
THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH-3, 1-layer PCB with copper limited to solder pads	110	ºC/W
		Package LH-3, 2-layer PCB with 0.926 in^2 on each side, connected by thermal vias	228	ºC/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	ºC/W

Power Derating Curve



Power Dissipation versus Ambient Temperature



Functional Description

Operation

The output of these devices switches low (turns on) when a magnetic field (south polarity) perpendicular to the Hall element exceeds the operate point threshold, B_{OP}. After turn-on, the output voltage is $V_{OUT(SAT)}$. The output transistor is capable of sinking current up to the short circuit current limit, I_{OM}, which is a minimum of 30 mA. When the magnetic field is reduced below the release point, B_{RP}, the device output goes high (turns off). The difference in the magnetic operate and release points is the hysteresis, B_{hys}, of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

Powering-on the device in the hysteresis region, less than B_{OP} and higher than B_{RP}, allows an indeterminate output state. The correct state is attained after the first excursion beyond B_{OP} or B_{RP}.

Applications

It is strongly recommended that an external bypass capacitor be connected (in close proximity to the Hall element) between the supply and ground of the device to reduce both external noise and noise generated by the chopper stabilization technique. As is shown in Panel B of figure 1, a 0.1µF capacitor is typical.

Extensive applications information on magnets and Hall-effect devices is available in:

- *Hall-Effect IC Applications Guide*, AN27701,
- *Hall-Effect Devices: Gluing, Potting, Encapsulating, Lead Welding and Lead Forming*, AN27703.1
- *Soldering Methods for Allegro's Products – SMT and Through-Hole*, AN26009

All are provided in *Allegro Electronic Data Book*, AMS-702 and the Allegro Web site: www.allegromicro.com

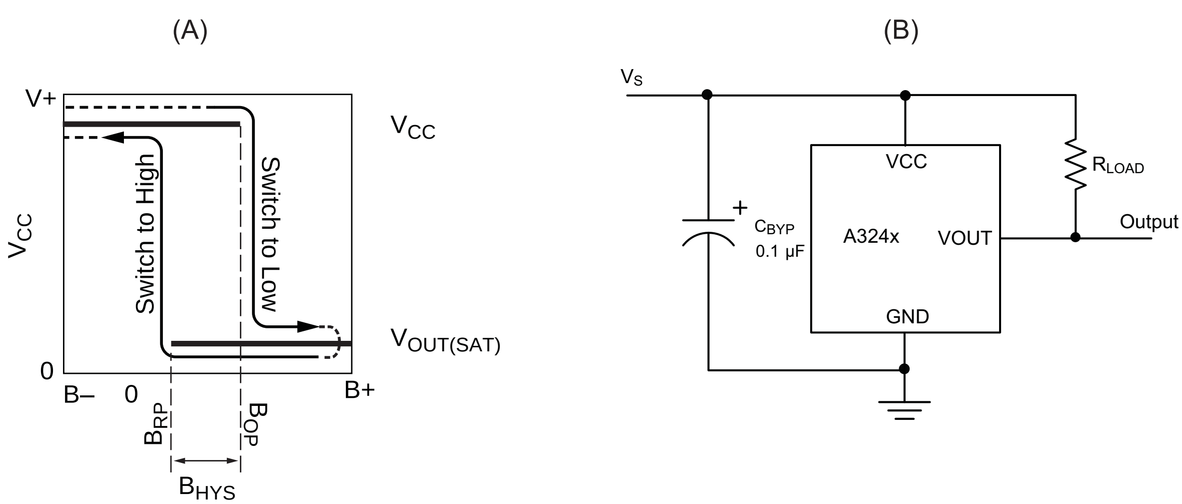


Figure 1: Switching Behavior of Unipolar Switches. In Panel A, *on the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength, and the B– direction indicates decreasing south polarity field strength (including the case of increasing north polarity). This behavior can be exhibited when using a circuit such as that shown in panel B.*

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Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall element. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges.

Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The patented Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic-field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic-field-induced signal to recover its original spectrum at baseband, while the DC offset becomes a high-frequency signal. The magnetic-field-induced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. This configuration is illustrated in figure 2.

The chopper stabilization technique uses a 200 kHz high-frequency clock. For demodulation process, a sample and hold technique is used, where the sampling is performed at twice the chopper frequency (400 kHz). This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

The repeatability of magnetic-field-induced switching is affected slightly by a chopper technique. However, the Allegro high-frequency chopping approach minimizes the affect of jitter and makes it imperceptible in most applications. Applications that are more likely to be sensitive to such degradation are those requiring precise sensing of alternating magnetic fields; for example, speed sensing of ring-magnet targets. For such applications, Allegro recommends its digital device families with lower sensitivity to jitter. For more information on those devices, contact your Allegro sales representative.

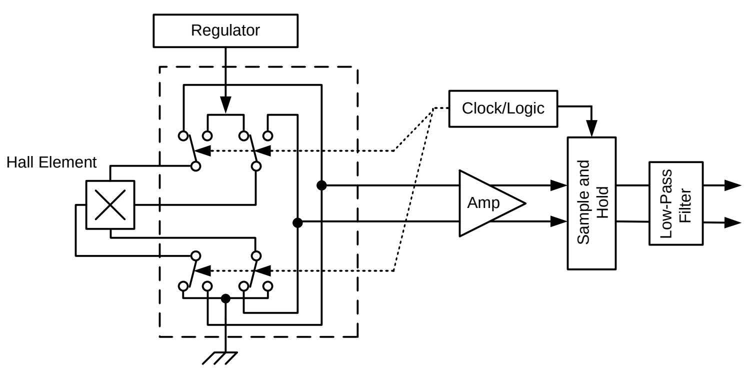

Figure 2. Chopper Stabilization Circuit (Dynamic Quadrature Offset Cancellation)

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Power Derating

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 1.5 mA, and $R_{\theta JA}$ = 165 °C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\text{ V} \times 1.5\text{ mA} = 18\text{ mW}$$

$$\Delta T = P_D \times R_{\theta JA} = 18\text{ mW} \times 165\text{ °C/W} = 3\text{°C}$$

$$T_J = T_A + \Delta T = 25\text{°C} + 3\text{°C} = 28\text{°C}$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package LH, using a low-K PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=228 °C/W, $T_{J(max)}$ = 165°C, $V_{CC(max)}$ = 24 V, and $I_{CC(max)}$ = 5 mA.

Calculate the maximum allowable power level, $P_{D(max)}$. First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165\text{°C} - 150\text{°C} = 15\text{°C}$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15\text{°C} \div 228\text{ °C/W} = 65.8\text{ mW}$$

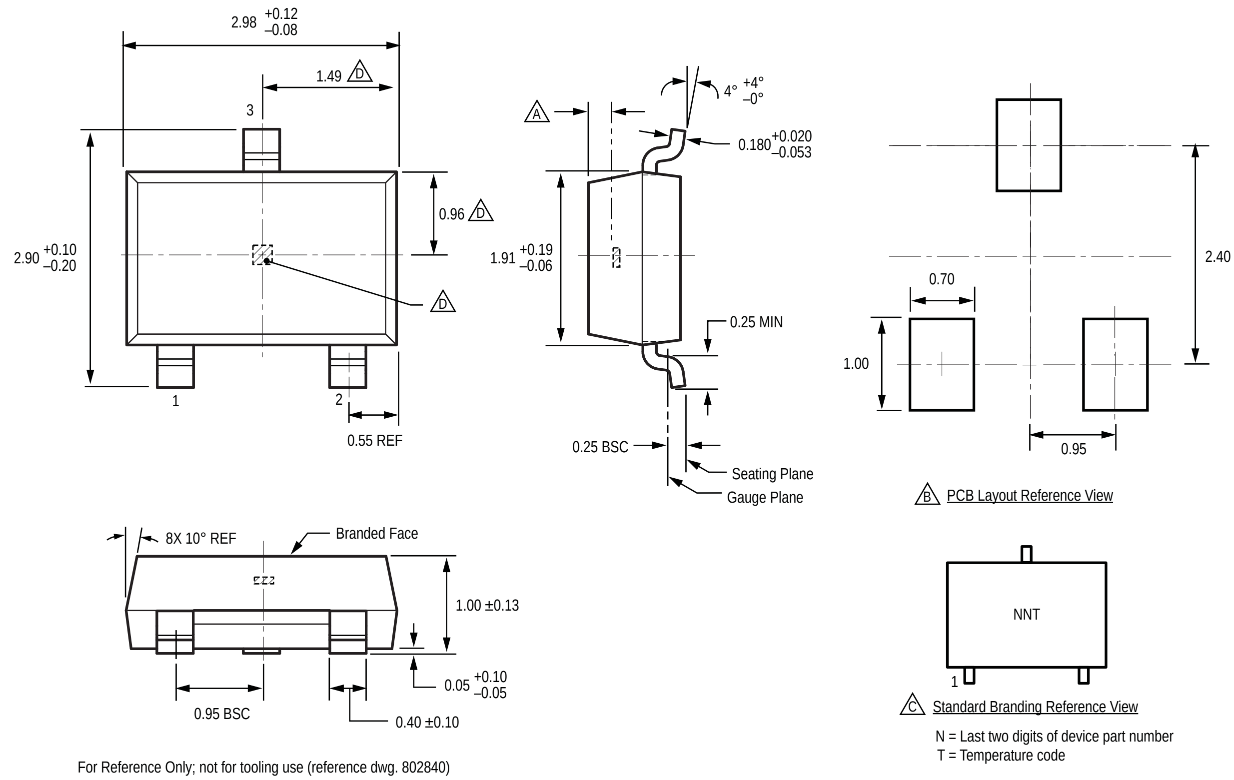
Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 65.8\text{ mW} \div 5\text{ mA} = 13.2\text{ V}$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages $\leq V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.

Package LH, 3-Pin (SOT-23W)



For Reference Only; not for tooling use (reference dwg. 802840)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

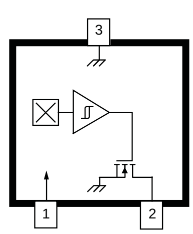
A Active Area Depth, 0.28 mm REF

B Reference land pattern layout
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

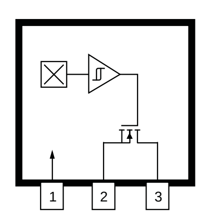
C Branding scale and appearance at supplier discretion

D Hall element, not to scale

Package LH



Package UA



Terminal List

Name	Description	Number	
		Package LH	Package UA
VCC	Connects power supply to chip	1	1
VOUT	Output from circuit	2	3
GND	Ground	3	2

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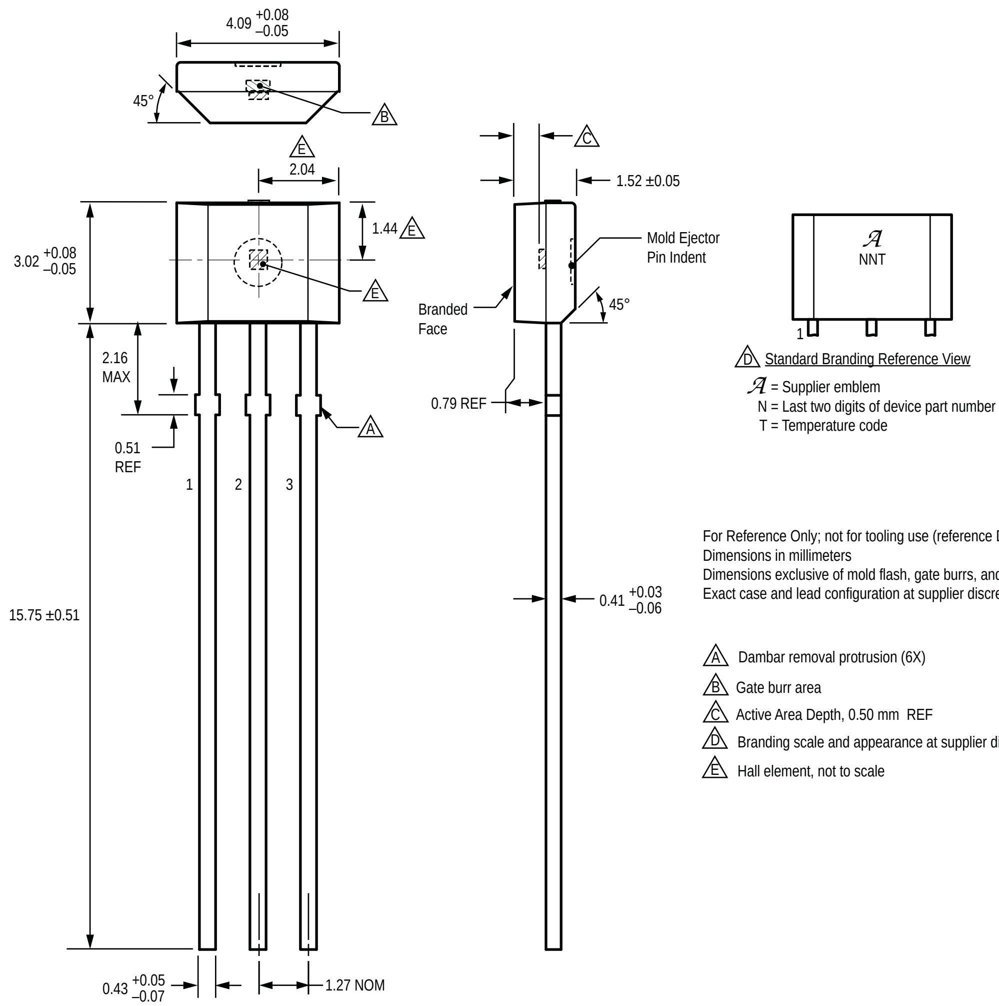
Package UA, 3-Pin SIP



For Reference Only; not for tooling use (reference DWG-9049)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

- A Dambar removal protrusion (6X)
- B Gate burr area
- C Active Area Depth, 0.50 mm REF
- D Branding scale and appearance at supplier discretion
- E Hall element, not to scale

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