PLDC20RA10

Reprogrammable Asynchronous CMOS Logic Device

Features

- **Advanced-user programmable macrocell**
- **CMOS EPROM technology for reprogrammability**
- **Up to 20 input terms**
- **10 programmable I/O macrocells**
- **Output macrocell programmable as combinatorial or asynchronous D-type registered output**
- **Product-term control of register clock, reset and set and output enable**
- **Register preload and power-up reset**
- **Four data product terms per output macrocell**
- **Fast**
  - **—Commercial**
    t_{PD} = 15 ns
    t_{CO} = 15 ns
    t_{SU} = 7 ns
  - **—Military**
    t_{PD} = 20 ns
    t_{CO} = 20 ns
    t_{SU} = 10 ns
- **Low power**
  - **—I_{CC} max - 80 mA (Commercial)**
  - **—I_{CC} max = 85 mA (Military)**
- **High reliability**
  - **—Proven EPROM technology**
  - **—>2001V input protection**
  - **—100% programming and functional testing**
- **Windowed DIP, windowed LCC, DIP, LCC, PLCC available**

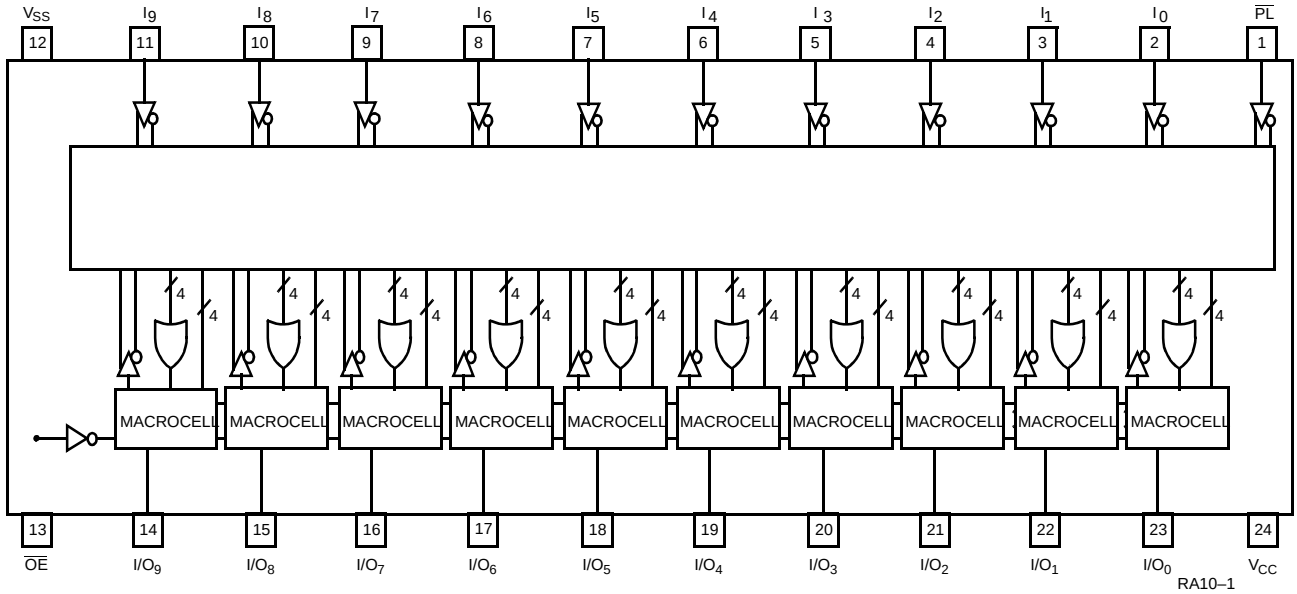
Functional Description

The Cypress PLDC20RA10 is a high-performance, second-generation programmable logic device employing a flexible macrocell structure that allows any individual output to be configured independently as a combinatorial output or as a fully asynchronous D-type registered output.

The Cypress PLDC20RA10 provides lower-power operation with superior speed performance than functionally equivalent bipolar devices through the use of high-performance 0.8-micron CMOS manufacturing technology.

The PLDC20RA10 is packaged in a 24 pin 300-mil molded DIP, a 300-mil windowed cerDIP, and a 28-lead square leadless chip carrier, providing up to 20 inputs and 10 outputs. When the windowed device is exposed to UV light, the 20RA10 is erased and can then be reprogrammed.

Logic Block Diagram

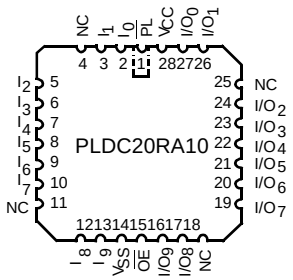


Selection Guide

Generic Part Number	t_{PD} ns		t_{SU} ns		t_{CO} ns		t_{CC} ns	
	Com'l	Mil	Com'l	Mil	Com'l	Mil	Com'l	Mil
20RA10-15	15		7		15		80	
20RA10-20	20	20	10	10	20	20	80	85
20RA10-25		25		15		25		85
20RA10-35		35		20		35		85

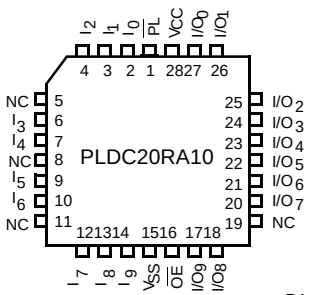
Pin Configurations

LCC
Top View



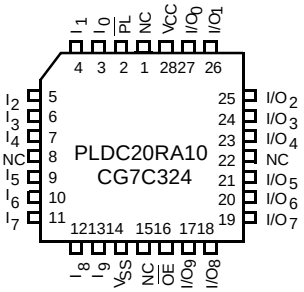
RA10–2

STD PLCC/HLCC
Top View



RA10–3

JEDEC PLCC/HLCC [1]
Top View



RA10–4

Macrocell Architecture

Figure 1 illustrates the architecture of the 20RA10 macrocell. The cell dedicates three product terms for fully asynchronous control of the register set, reset, and clock functions, as well as, one term for control of the output enable function.

The output enable product term output is ANDed with the input from pin 13 to allow either product term or hardwired external control of the output or a combination of control from both sources. If product-term-only control is selected, it is automatically chosen for all outputs since, for this case, the external output enable pin must be tied LOW. The active polarity of each output may be programmed independently for each output cell and is subsequently fixed. *Figure 2* illustrates the output enable options available.

When an I/O cell is configured as an output, combinatorial-only capability may be selected by forcing the set and reset product term outputs to be HIGH under all input conditions. This is achieved by programming all input term programming cells for these two product terms. *Figure 3* illustrates the available output configuration options.

An additional four uncommitted product terms are provided in each output macrocell as resources for creation of user-defined logic functions.

Programmable I/O

Because any of the ten I/O pins may be selected as an input, the device input configuration programmed by the user may vary from a total of nine programmable plus ten dedicated inputs (a total of nineteen inputs) and one output down to a ten-input, ten-output configuration with all ten programmable I/O cells configured as outputs. Each input pin available in a given configuration is available as an input to the four control product terms and four uncommitted product terms of each programmable I/O macrocell that has been configured as an output.

An I/O cell is programmed as an input by tying the output enable pin (pin 13) HIGH or by programming the output enable product term to provide a LOW, thereby disabling the output buffer, for all possible input combinations.

When utilizing the I/O macrocell as an output, the input path functions as a feedback path allowing the output signal to be fed back as an input to the product term array. When the output cell is configured as a registered output, this feedback path may be used to feed back the current output state to the device inputs to provide current state control of the next output state as required for state machine implementation.

Preload and Power-Up Reset

Functional testability of programmed devices is enhanced by inclusion of register preload capability, which allows the state of each register to be set by loading each register from an external source prior to exercising the device. Testing of complex state machine designs is simplified by the ability to load an arbitrary state without cycling through long test vector sequences to reach the desired state. Recovery from illegal states can be verified by loading illegal states and observing recovery. Preload of a particular register is accomplished by impressing the desired state on the register output pin and lowering the signal level on the preload control pin (pin1) to a logic LOW level. If the specified preload set-up, hold and pulse width minimums have been observed, the desired state is loaded into the register. To insure predictable system initialization, all registers are preset to a logic LOW state upon power-up, thereby setting the active LOW outputs to a logic HIGH.

Note:

1. The CG7C324 is the PLDC20RA10 packaged in the JEDEC-compatible 28-pin PLCC pinout. Pin function and pin order is identical for both PLCC pinouts. The principal difference is in the location of the "no connect" (NC) pins

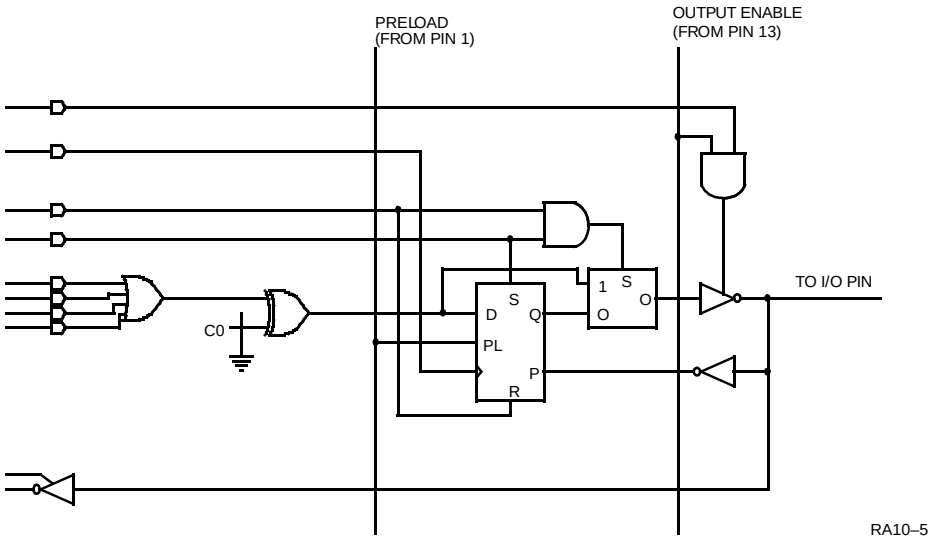


Figure 1. PLDC20RA10 Macrocell

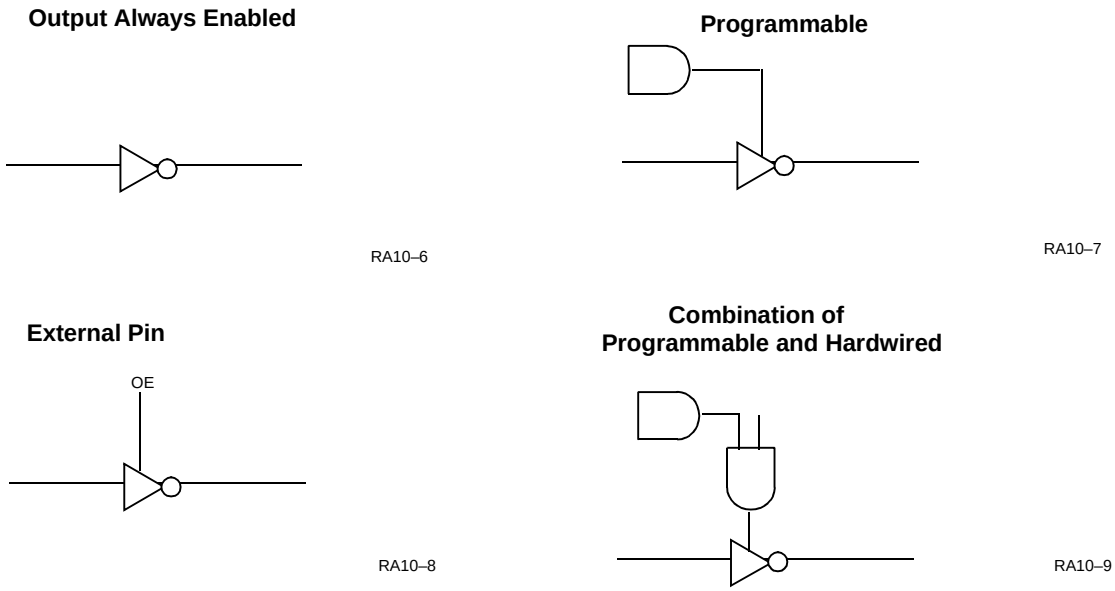
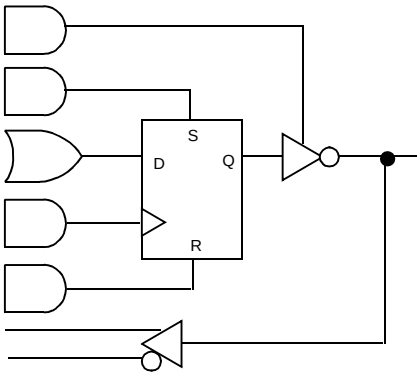


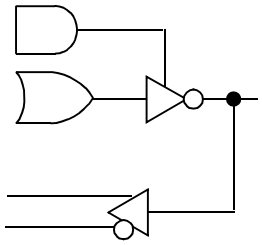
Figure 2. Four Possible Output Enable Alternatives for the PLDC20RA10

Registered/Active LOW



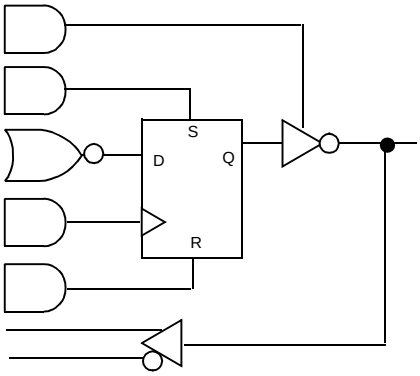
RA10–10

Combinatorial/Active LOW



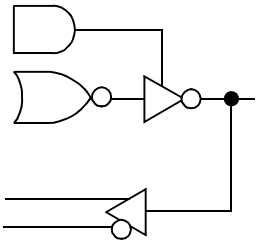
RA10–11

Registered/Active HIGH



RA10–12

Combinatorial/Active HIGH



RA10–13

Figure 3. Four Possible Macrocell Configurations for the PLDC20RA10

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage..... –3.0 V to + 7.0 V

Output Current into Outputs (LOW) .....16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

DC Program Voltage 13.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ± 10%
Military[2]	–55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3.2 mA	Com'l	2.4		V
			I_{OH} = –2 mA	Mil			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8 mA			0.5	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[4]			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[4]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max			–10	+10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			–40	+40	µA
I_{SC}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = 0.5V[6]			–30	–90	mA
I_{CC1}	Standby Power Supply Current	V_{CC}= Max., V_{IN} = GND Outputs Open		Com'l		75	mA
				Mil		80	mA
I_{CC2}	Power Supply Current at Frequency[5]	V_{CC} = Max., Outputs Disabled (In High Z State) Device Operating at f_{MAX}		Com'l		80	mA
				Mil		85	mA

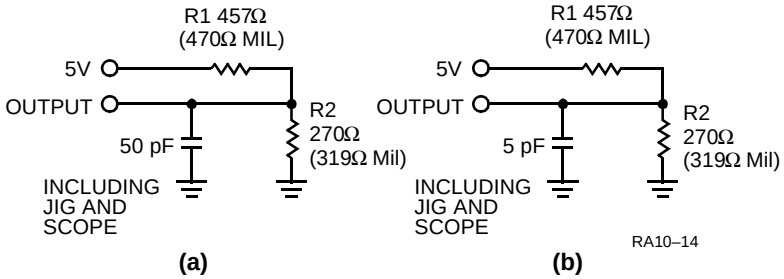
Capacitance[5]

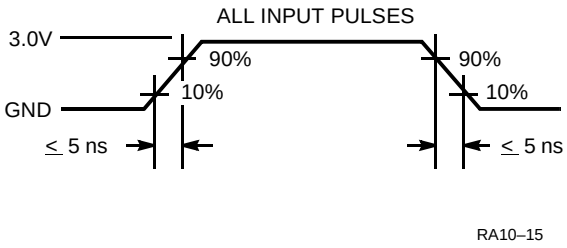
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz	10	pF

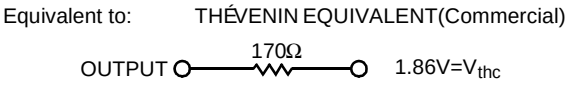
Notes:

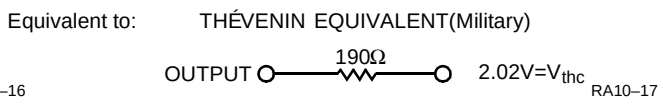
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
5. Tested initially and after any design or process changes that may affect these parameters.
6. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

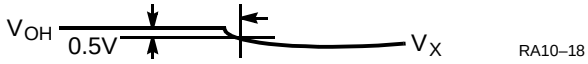
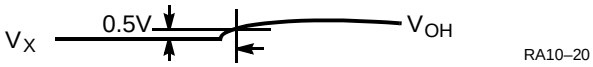
AC Test Loads and Waveforms (Commercial)









Parameter	V_{th}	Output Waveform Measurement Level
$t_{PXZ(-)}$	1.5V	 RA10–18
$t_{PXZ(+)}$	2.6V	 RA10–19
$t_{PZX(+)}$	V_{thc}	 RA10–20
$t_{PZX(-)}$	V_{thc}	 RA10–21
$t_{ER(-)}$	1.5V	 RA10–22
$t_{ER(+)}$	2.6V	 RA10–23
$t_{EA(+)}$	V_{thc}	 RA10–24
$t_{EA(-)}$	V_{thc}	 RA10–25

(c)

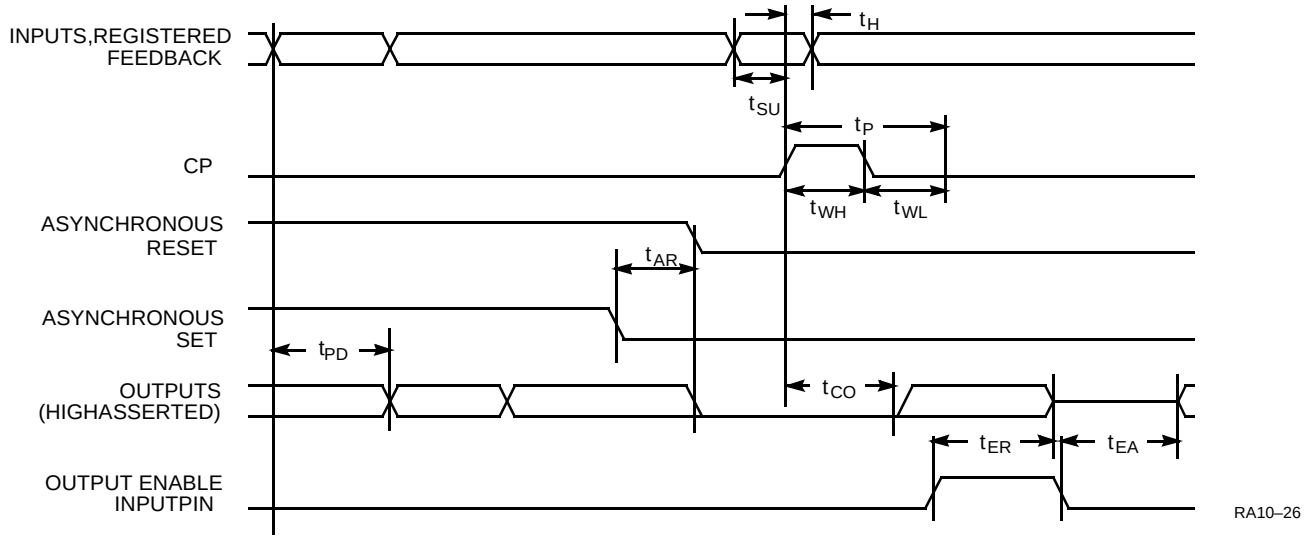
Switching Characteristics Over the Operating Range[3, 7, 8]

Parameter	Description	Commercial				Military						Unit
		–15		–20		–20		–25		–35		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output		15		20		20		25		35	ns
t_{EA}	Input to Output Enable		15		20		20		30		35	ns
t_{ER}	Input to Output Disable		15		20		20		30		35	ns
t_{PZX}	Pin 13 to Output Enable		12		15		15		20		25	ns
t_{PXZ}	Pin 13 to Output Disable		12		15		15		20		25	ns
t_{CO}	Clock to Output		15		20		20		25		35	ns
t_{SU}	Input or Feedback Set-Up Time	7		10		10		15		20		ns
t_H	Hold Time	3		5		3		5		5		ns
t_P	Clock Period ($t_{SU} + t_{CO}$)	22		30		30		40		55		ns
t_{WH}	Clock Width HIGH[5]	10		13		12		18		25		ns
t_{WL}	Clock Width LOW[5]	10		13		12		18		25		ns
f_{MAX}	Maximum Frequency ($1/t_P$)[5]	45.5		33.3		33.3		25.0		18.1		MHz
t_S	Input of Asynchronous Set to Registered Output		15		20		20		25		40	ns
t_R	Input of Asynchronous Reset to Registered Output		15		20		20		25		40	ns
t_{ARW}	Asynchronous Reset Width[5]	15		20		20		25		25		ns
t_{ASW}	Asynchronous S-Width[5]	15		20		20		25		25		ns
t_{AR}	Asynchronous Set/ Reset Recovery Time	10		12		12		15		20		ns
t_{WP}	Preload Pulse Width	15		15		15		15		15		ns
t_{SUP}	Preload Set-Up Time	15		15		15		15		15		ns
t_{HP}	Preload Hold Time	15		15		15		15		15		ns

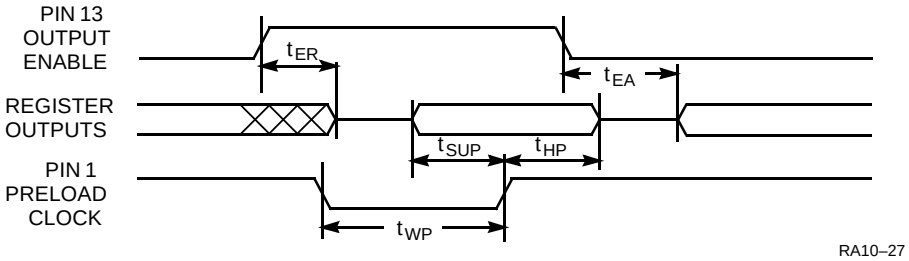
Notes:

7. Part (a) of AC Test Loads was used for all parameters except t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}, which use part (b).
8. The parameters t_{ER} and t_{PXZ} are measured as the delay from the input disable logic threshold transition to V_{OH} - 0.5 V for an enabled HIGH output or V_{OL} +0.5V for an enabled LOW output. Please see part (c) of AC Test Loads and Waveforms for waveforms and measurement reference levels.

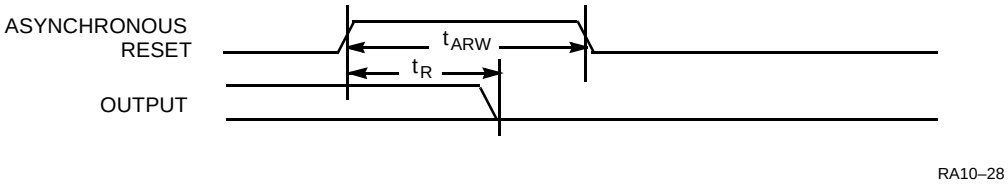
Switching Waveform



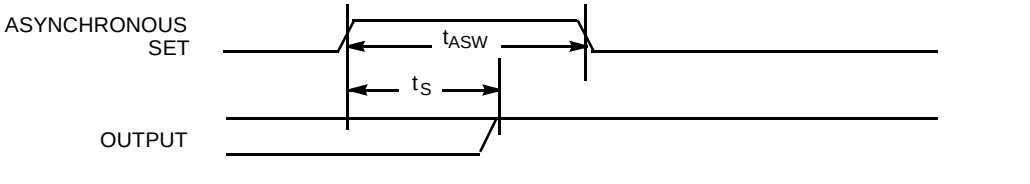
Preload Switching Waveform



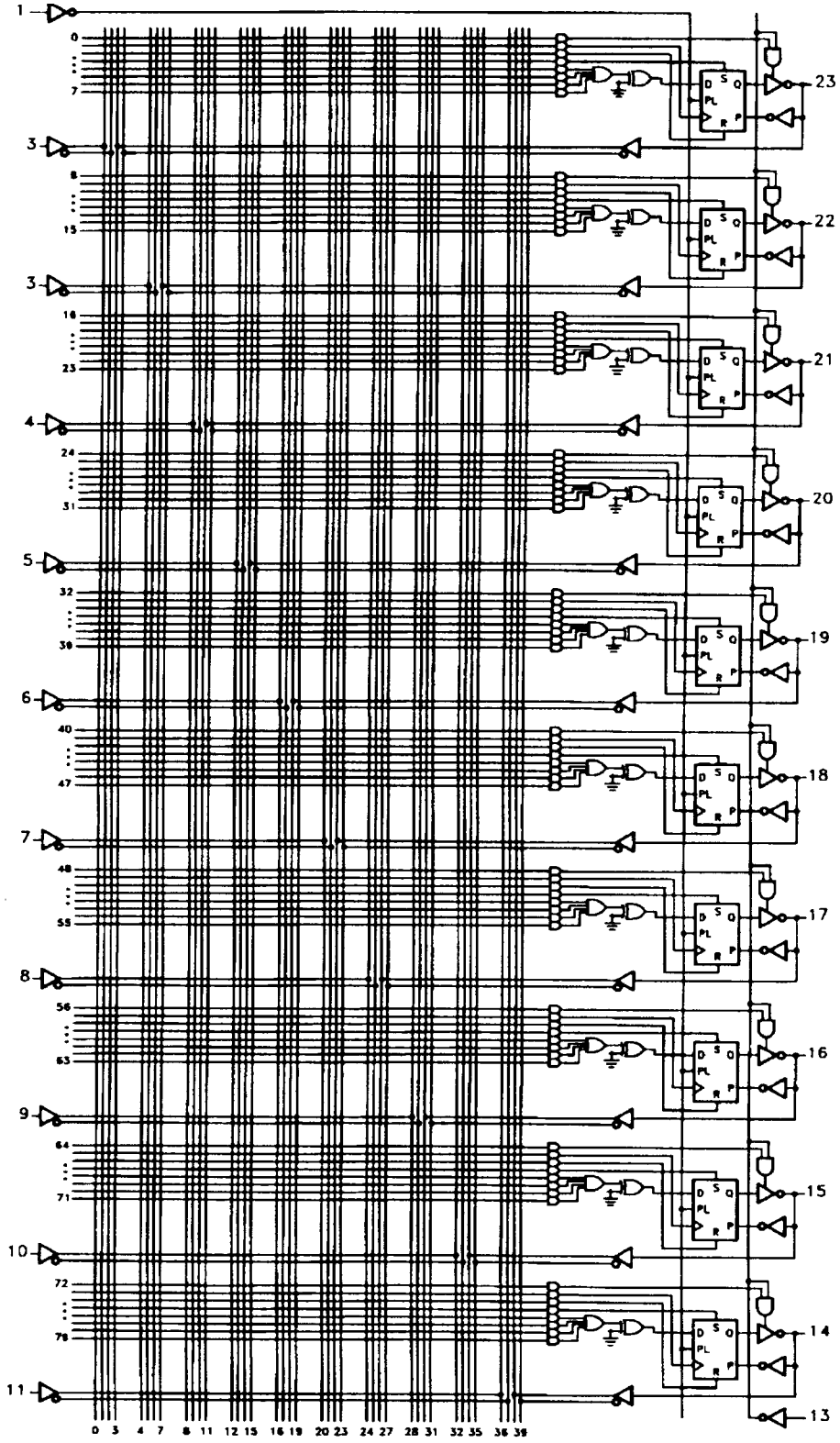
Asynchronous Reset



Asynchronous Set



Functional Logic Diagram



Ordering Information

I_{CC2}	t_{PD} (ns)	t_{SU} (ns)	t_{CO} (ns)	Ordering Code	Package Name	Package Type	Operating Range
80	15	7	15	PLDC20RA10-15JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
				PLDC20RA10-15PC	P13	24-Lead (300-Mil) Molded DIP	
				CG7C324-A15JC	J64	28-Lead Plastic Leaded Chip Carrier	
	20	10	20	PLDC20RA10-20PC	P13	24-Lead (300-Mil) Molded DIP	
				CG7C324-A20JC	J64	28-Lead Plastic Leaded Chip Carrier	
85	20	10	20	PLDC20RA10-20DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PLDC20RA10-20WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
	25	15	25	PLDC20RA10-25DMB	D14	24-Lead (300-Mil) CerDIP	
				PLDC20RA10-25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
	35	20	35	PLDC20RA10-35DMB	D14	24-Lead (300-Mil) CerDIP	
				PLDC20RA10-35WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3

DC Characteristics

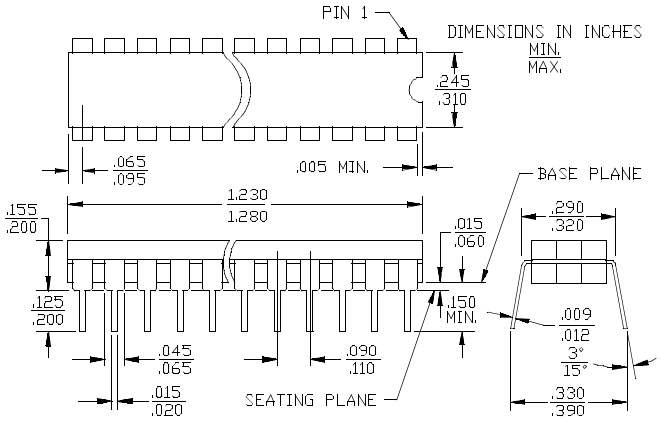
Parameter	Subgroups
I_{CC}	1, 2, 3

Switching Characteristics

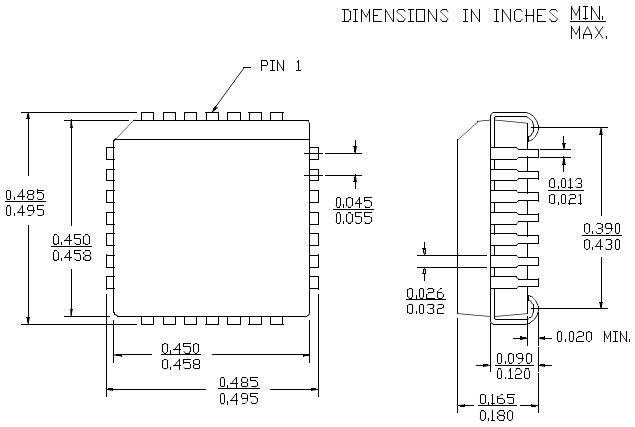
Parameter	Subgroups
t_{PD}	9, 10, 11
t_{PZX}	9, 10, 11
t_{CO}	9, 10, 11
t_{SU}	9, 10, 11
t_{H}	9, 10, 11

Package Diagrams

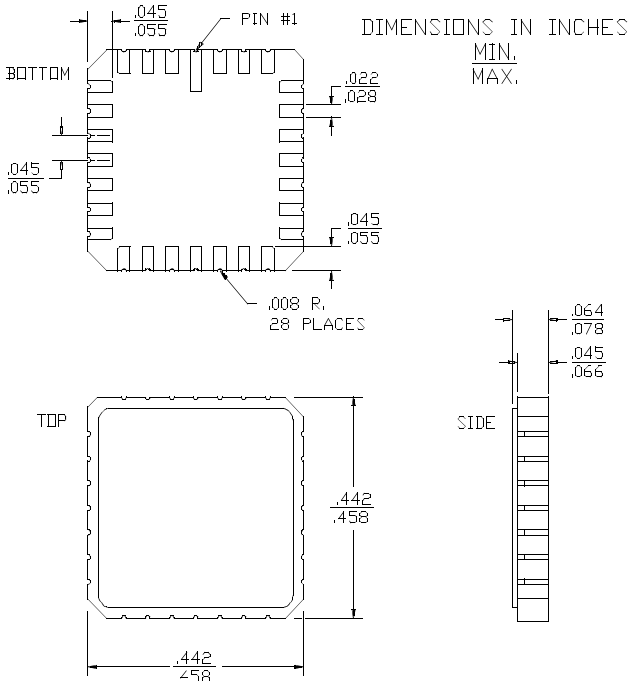
24-Lead (300-Mil) CerDIP D14
MIL-STD-1835 D- 9Config.A



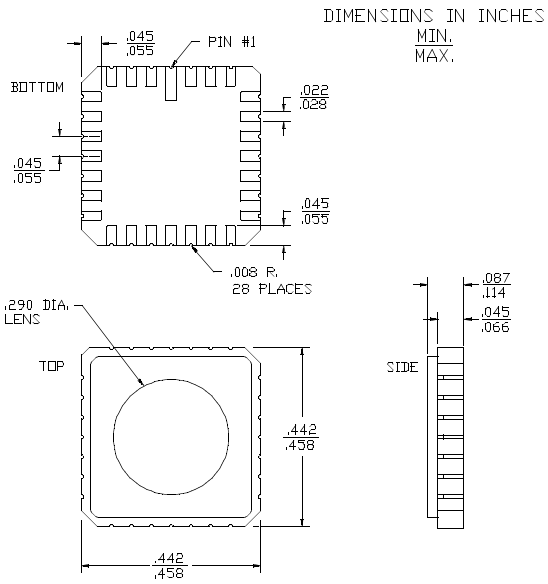
28-Lead Plastic Leaded Chip Carrier J64



28-Square L64 Carrier Chip Leadless
MIL-STD-1835 C-4

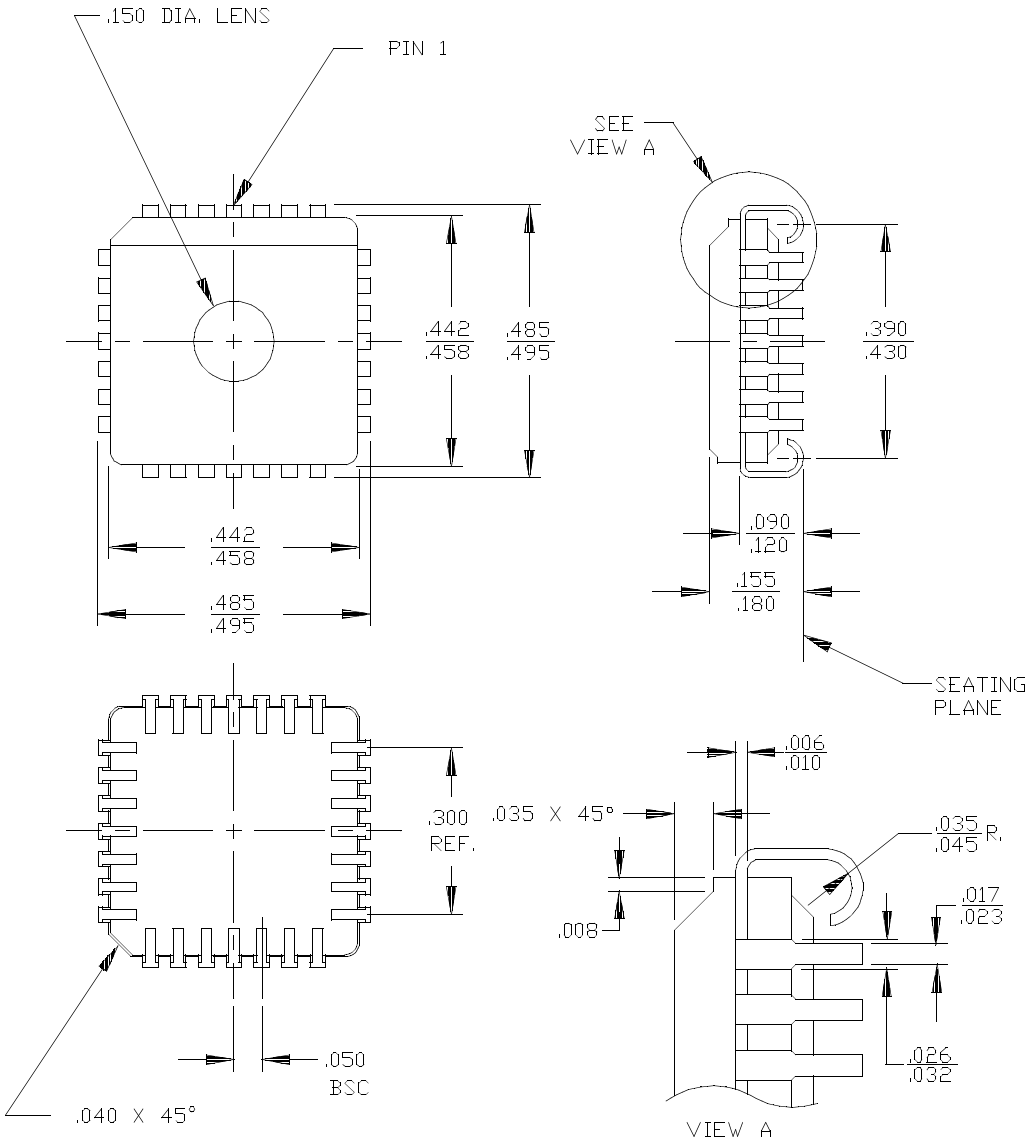


28-Pin Windowed Leadless Chip Carrier Q64
MIL-STD-1835 C-4



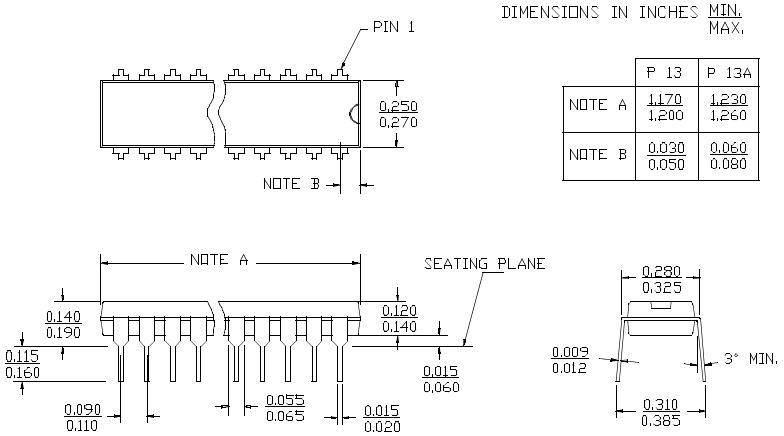
Package Diagrams (continued)

28-Pin Windowed Leaded Chip Carrier H64



Package Diagrams (continued)

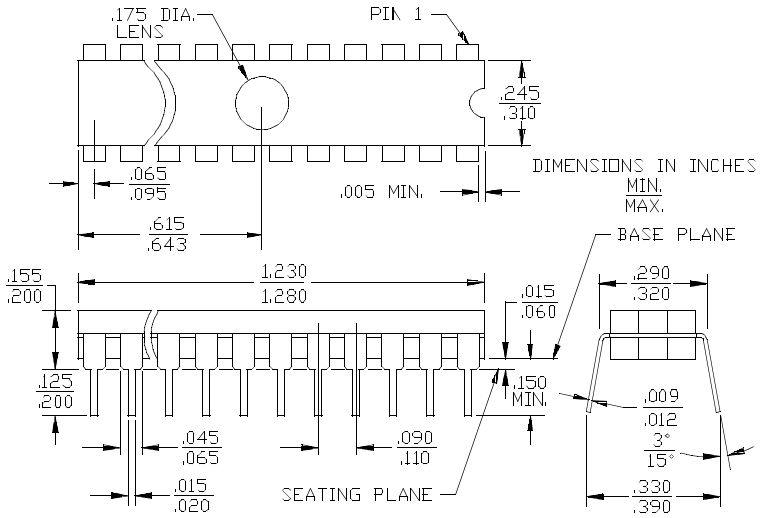
24-Lead (300-Mil) Molded DIP P13/P13A



	P 13	P 13A
NOTE A	1.170 1.200	1.230 1.260
NOTE B	0.030 0.050	0.060 0.080

24-Lead (300-Mil) Windowed CerDIP W14

MIL-STD-1835 D-9 Config.A



Document Title: PLDC20RA10 Reprogrammable Asynchronous CMOS Logic Device Document Number: 38-03012				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106294	04/24/01	SZV	Change from Spec number: 38-00073 to 38-03012