



**USE ULTRA37000™ FOR
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PALCE20V8

Flash-Erasable Reprogrammable CMOS PAL® Device

Features

- Active pull-up on data input pins
- Low power version (20V8L)
 - 55 mA max. commercial (15, 25 ns)
 - 65 mA max. military/industrial (15, 25 ns)
- Standard version has low power
 - 90 mA max. commercial (15, 25 ns)
 - 115 mA max. commercial (10 ns)
 - 130 mA max. military/industrial (15, 25 ns)
- CMOS Flash technology for electrical erasability and reprogrammability
- User-programmable macrocell
 - Output polarity control
 - Individually selectable for registered or combinatorial operation

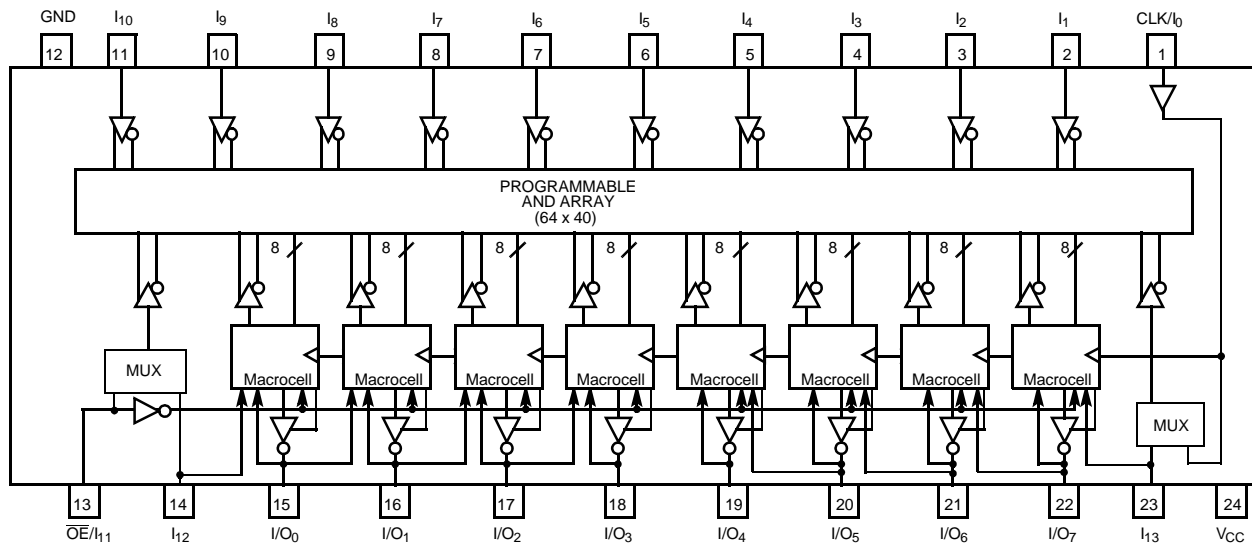
- QSOP package available
 - 10, 15, and 25 ns com'l version
 - 15, and 25 ns military/industrial versions
- High reliability
 - Proven Flash technology
 - 100% programming and functional testing

Functional Description

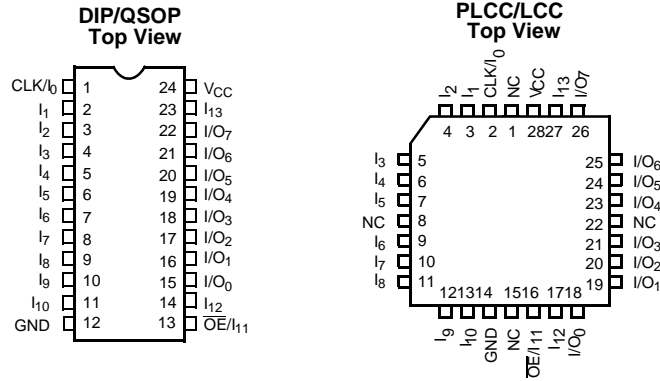
The Cypress PALCE20V8 is a CMOS Flash Erasable second-generation programmable array logic device. It is implemented with the familiar sum-of-product (AND-OR) logic structure and the programmable macrocell.

The PALCE20V8 is executed in a 24-pin 300-mil molded DIP, a 300-mil cerdip, a 28-lead square ceramic leadless chip carrier, a 28-lead square plastic leaded chip carrier, and a 24-lead quarter size outline. The device provides up to 20 inputs and 8 outputs. The PALCE20V8 can be electrically erased and reprogrammed. The programmable macrocell enables the device to function as a superset to the familiar 24-pin PLDs such as 20L8, 20R8, 20R6, 20R4.

Logic Block Diagram (PDIP/CDIP/QSOP)



Pin Configuration



Selection Guide

| Generic Part Number | t _{PD} ns | | t _S ns | | t _{CO} ns | | I _{CC} mA | |
|---------------------|--------------------|-----|-------------------|-----|--------------------|-----|--------------------|---------|
| | Com'I/Ind | Mil | Com'I/Ind | Mil | Com'I/Ind | Mil | Com'I | Mil/Ind |
| PALCE20V8-5 | 5 | | 3 | | 4 | | 115 | |
| PALCE20V8-7 | 7.5 | | 7 | | 5 | | 115 | |
| PALCE20V8-10 | 10 | 10 | 10 | 10 | 7 | 10 | 115 | 130 |
| PALCE20V8-15 | 15 | 15 | 12 | 12 | 10 | 12 | 90 | 130 |
| PALCE20V8-25 | 25 | 25 | 15 | 20 | 12 | 20 | 90 | 130 |
| PALCE20V8L-15 | 15 | 15 | 12 | 12 | 10 | 12 | 55 | 65 |
| PALCE20V8L-25 | 25 | 25 | 15 | 20 | 12 | 20 | 55 | 65 |

Shaded areas contain preliminary information.

Functional Description

The PALCE20V8 features 8 product terms per output and 40 input terms into the AND array. The first product term in a macrocell can be used either as an internal output enable control or as a data product term.

There are a total of 18 architecture bits in the PALCE20V8 macrocell; two are global bits that apply to all macrocells and 16 that apply locally, two bits per macrocell. The architecture bits determine whether the macrocell functions as a register or combinatorial with inverting or noninverting output. The output enable control can come from an external pin or internally from a product term. The output can also be permanently enabled, functioning as a dedicated output or permanently disabled, functioning as a dedicated input. Feedback paths are selectable from either the input/output pin associated with the macrocell, the input/output pin associated with an adjacent pin, or from the macrocell register itself.

Power-Up Reset

All registers in the PALCE20V8 power-up to a logic LOW for predictable system initialization. For each register, the associated output pin will be HIGH due to active-LOW outputs.

Electronic Signature

An electronic signature word is provided in the PALCE20V8 that consists of 64 bits of programmable memory that can contain user-defined data.

Security Bit

A security bit is provided that defeats the readback of the internal programmed pattern when the bit is programmed.

Low Power

The Cypress PALCE20V8 provides low-power operation through the use of CMOS technology, and increased testability with Flash reprogrammability.

Product Term Disable

Product Term Disable (PTD) fuses are included for each product term. The PTD fuses allow each product term to be individually disabled.

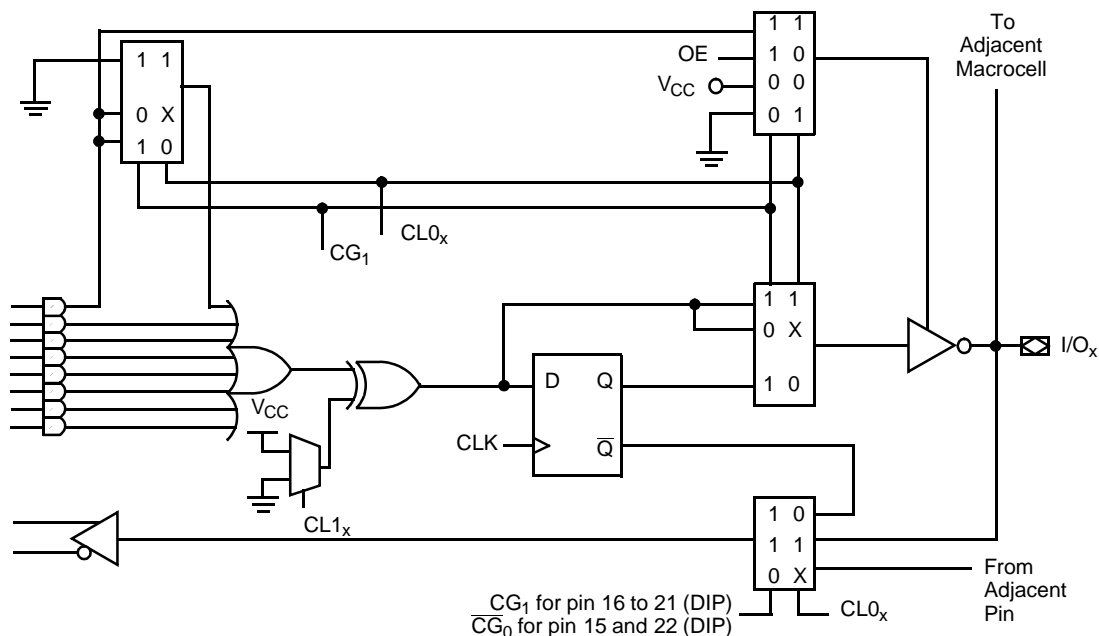
Input and I/O Pin Pull-Ups

The PALCE20V8 input and I/O pins have built-in active pull-ups that will float unused inputs and I/Os to an active HIGH state (logical 1). All unused inputs and three-stated I/O pins should be connected to another active input, V_{CC} , or Ground to improve noise immunity and reduce I_{CC} .

Configuration Table

| CG_0 | CG_1 | $CL0_x$ | Cell Configuration | Devices Emulated |
|--------|--------|---------|----------------------|---------------------|
| 0 | 1 | 0 | Registered Output | Registered Med PALs |
| 0 | 1 | 1 | Combinatorial I/O | Registered Med PALs |
| 1 | 0 | 0 | Combinatorial Output | Small PALs |
| 1 | 0 | 1 | Input | Small PALs |
| 1 | 1 | 1 | Combinatorial I/O | 20L8 only |

Macrocell





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PALCE20V8

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature -65°C to +150°C
- Ambient Temperature with Power Applied..... -55°C to +125°C
- Supply Voltage to Ground Potential (Pin 24 to Pin 12)..... -0.5V to +7.0V
- DC Voltage Applied to Outputs in High-Z State -0.5V to +7.0V

- DC Input Voltage -0.5V to +7.0V
- Output Current into Outputs (LOW)..... 24 mA
- DC Programming Voltage..... 12.5V
- Latch-up Current..... >200 mA

Operating Range^[1]

| Range | Ambient Temperature | V _{CC} |
|-------------------------|---------------------|-----------------|
| Commercial | 0°C to +75°C | 5V ±5% |
| Industrial | -40°C to +85°C | 5V ±10% |
| Military ^[2] | -55°C to +125°C | 5V ±10% |

Electrical Characteristics Over the Operating Range^[3]

| Parameter | Description | Test Conditions | | | Min. | Max. | Unit |
|--------------------------------|-----------------------------------|---|---------------------------|---------|------|------|------|
| | | | | | | | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} | I _{OH} = -3.2 mA | Com'l | 2.4 | | V |
| | | | I _{OH} = -2 mA | Mil/Ind | | | |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} | I _{OL} = 24 mA | Com'l | | 0.5 | V |
| | | | I _{OL} = 12 mA | Mil/Ind | | | |
| V _{IH} | Input HIGH Level | Guaranteed Input Logical HIGH Voltage for All Inputs ^[4] | | | 2.0 | | V |
| V _{IL} ^[5] | Input LOW Level | Guaranteed Input Logical LOW Voltage for All Inputs ^[4] | | | -0.5 | 0.8 | V |
| I _{IH} | Input or I/O HIGH Leakage Current | 3.5V ≤ V _{IN} ≤ V _{CC} | | | | 10 | μA |
| I _{IL} ^[6] | Input or I/O LOW Leakage Current | 0V ≤ V _{IN} ≤ V _{IN} (Max.) | | | | -100 | μA |
| I _{SC} | Output Short Circuit Current | V _{CC} = Max., V _{OUT} = 0.5V ^[7,8] | | | -30 | -150 | mA |
| I _{CC} | Operating Power Supply Current | V _{CC} = Max., V _{IL} = 0V, V _{IH} = 3V, Output Open, f = 15 MHz (counter) | 5, 7, 10 ns | Com'l | | 115 | mA |
| | | | 15, 25 ns | | | 90 | mA |
| | | | 15L, 25L ns | | | 55 | mA |
| | | | 10, 15, 25 ns | Mil/Ind | | 130 | mA |
| | | | 15L, 25L ns | Mil/Ind | | 65 | mA |

Capacitance^[8]

| Parameter | Description | Test Conditions | Typ. | Unit |
|------------------|--------------------|-------------------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 2.0V @ f = 1 MHz | 5 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 2.0V @ f = 1 MHz | 5 | pF |

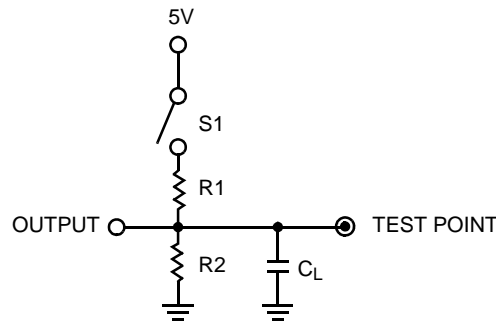
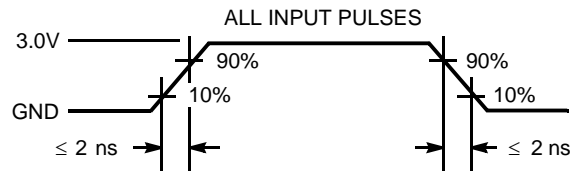
Endurance Characteristics^[8]

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|-----------|------------------------------|-------------------------------|------|------|--------|
| N | Minimum Reprogramming Cycles | Normal Programming Conditions | 100 | | Cycles |

Notes:

1. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
5. V_{IL} (Min.) is equal to -3.0V for pulse durations less than 20 ns.
6. The leakage current is due to the internal pull-up resistor on all pins.
7. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
8. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



| Specification | S ₁ | C _L | Commercial | | Military | | Measured Output Value |
|------------------------------------|------------------------------|----------------|----------------|----------------|----------------|----------------|--|
| | | | R ₁ | R ₂ | R ₁ | R ₂ | |
| t _{PD} , t _{CO} | Closed | 50 pF | 200Ω | 390Ω | 390Ω | 750Ω | 1.5V |
| t _{PZX} , t _{EA} | Z H: Open Z L: Closed | | | | | | 1.5V |
| t _{PXZ} , t _{ER} | H Z: Open L Z: Closed | 5 pF | | | | | H Z: V _{OH} - 0.5V L Z: V _{OL} + 0.5V |

Commercial and Industrial Switching Characteristics ^[3]

| Parameter | Description | 20V8-5 | | 20V8-7 | | 20V8-10 | | 20V8-15 | | 20V8-25 | | Unit |
|------------------|---|--------|------|--------|------|---------|------|---------|------|---------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{PD} | Input to Output Propagation Delay ^[9] | 1 | 5 | 1 | 7.5 | 1 | 10 | 1 | 15 | 1 | 25 | ns |
| t _{PZX} | OE to Output Enable | | 5 | | 6 | | 10 | | 15 | | 20 | ns |
| t _{PXZ} | OE to Output Disable | | 5 | | 6 | | 10 | | 15 | | 20 | ns |
| t _{EA} | Input to Output Enable Delay ^[8] | | 6 | | 9 | | 10 | | 15 | | 25 | ns |
| t _{ER} | Input to Output Disable Delay ^[8,10] | | 6 | | 9 | | 10 | | 15 | | 25 | ns |
| t _{CO} | Clock to Output Delay ^[9] | 1 | 4 | 1 | 5 | 1 | 7 | 1 | 10 | 1 | 12 | ns |
| t _S | Input or Feedback Set-up Time | 3 | | 7 | | 10 | | 12 | | 15 | | ns |
| t _H | Input Hold Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t _P | External Clock Period (t _{CO} + t _S) | 7 | | 12 | | 17 | | 22 | | 27 | | ns |

Shaded areas contain preliminary information.

Notes:

9. Min. times are tested initially and after any design or process changes that may affect these parameters.
10. This parameter is measured as the time after OE pin or internal disable input disables or enables the output pin. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max.
11. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
12. This specification indicates the guaranteed maximum frequency at which the device can operate in data path mode.
13. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate.
14. This parameter is calculated from the clock period at f_{MAX} internal (1/f_{MAX3}) as measured (see Note 7 above) minus t_S.

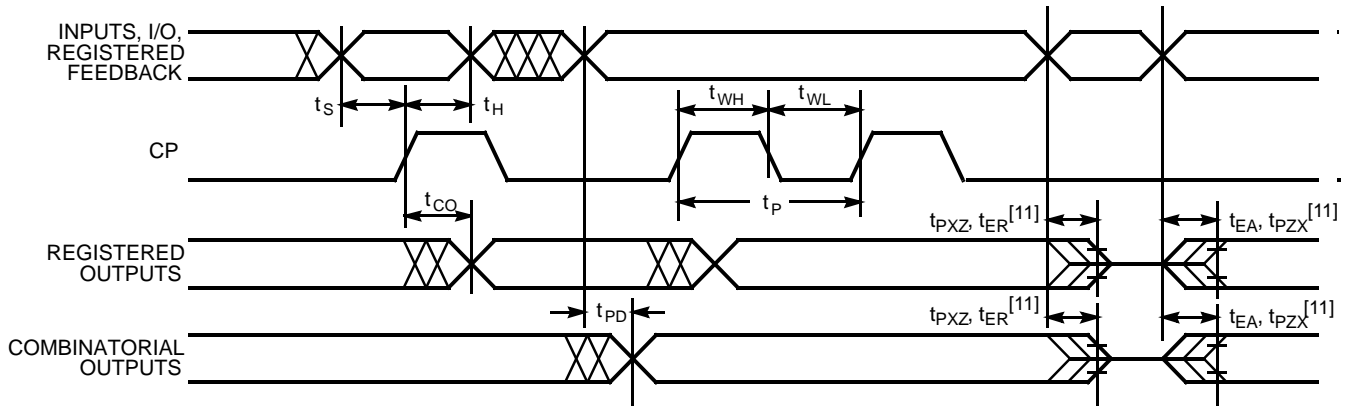
Commercial and Industrial Switching Characteristics (continued)^[3]

| Parameter | Description | 20V8-5 | | 20V8-7 | | 20V8-10 | | 20V8-15 | | 20V8-25 | | Unit |
|-------------------|---|--------|------|--------|------|---------|------|---------|------|---------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{WH} | Clock Width HIGH ^[8] | 3 | | 5 | | 8 | | 8 | | 12 | | ns |
| t _{WL} | Clock Width LOW ^[8] | 3 | | 5 | | 8 | | 8 | | 12 | | ns |
| f _{MAX1} | External Maximum Frequency (1/(t _{CO} + t _S)) ^[8,11] | 143 | | 83 | | 58 | | 45.5 | | 37 | | MHz |
| f _{MAX2} | Data Path Maximum Frequency (1/(t _{WH} + t _{WL})) ^[8, 12] | 166.6 | | 100 | | 62.5 | | 62.5 | | 41.6 | | MHz |
| f _{MAX3} | Internal Feedback Maximum Frequency (1/(t _{CF} + t _S)) ^[8,13] | 166.6 | | 100 | | 62.5 | | 50 | | 40 | | MHz |
| t _{CF} | Register Clock to Feedback Input ^[8, 14] | | 3 | | 3 | | 6 | | 8 | | 10 | ns |
| t _{PR} | Power-Up Reset Time ^[8] | 1 | | 1 | | 1 | | 1 | | 1 | | μs |

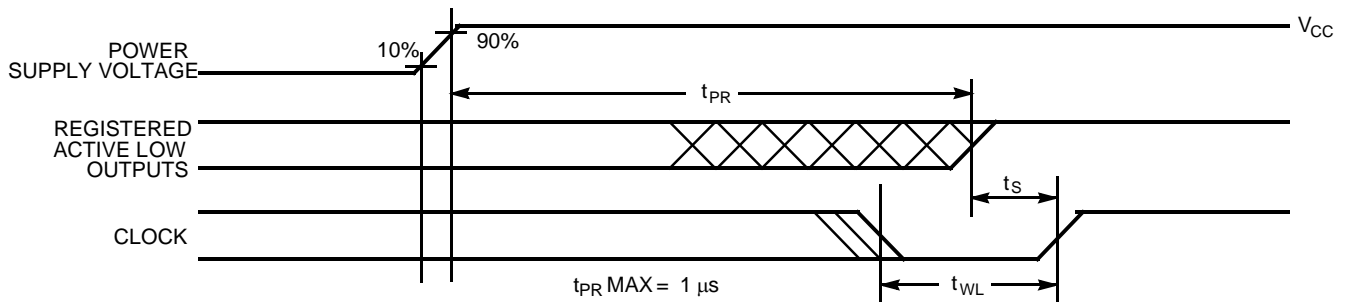
Military Switching Characteristics^[3]

| Parameter | Description | 20V8-10 | | 20V8-15 | | 20V8-25 | | Unit |
|-------------------|---|---------|------|---------|------|---------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{PD} | Input to Output Propagation Delay ^[9] | 1 | 10 | 1 | 15 | 1 | 25 | ns |
| t _{PZX} | OE to Output Enable | | 10 | | 15 | | 20 | ns |
| t _{PXZ} | OE to Output Disable | | 10 | | 15 | | 20 | ns |
| t _{EA} | Input to Output Enable Delay ^[8] | | 10 | | 15 | | 25 | ns |
| t _{ER} | Input to Output Disable Delay ^[8,10] | | 10 | | 15 | | 25 | ns |
| t _{CO} | Clock to Output Delay ^[9] | 1 | 10 | 1 | 12 | 1 | 20 | ns |
| t _S | Input or Feedback Set-Up Time | 10 | | 12 | | 20 | | ns |
| t _H | Input Hold Time | 0 | | 0 | | 0 | | ns |
| t _P | External Clock Period (t _{CO} + t _S) | 20 | | 24 | | 40 | | ns |
| t _{WH} | Clock Width HIGH ^[8] | 8 | | 10 | | 15 | | ns |
| t _{WL} | Clock Width LOW ^[8] | 8 | | 10 | | 15 | | ns |
| f _{MAX1} | External Maximum Frequency (1/(t _{CO} + t _S)) ^[8,11] | 50 | | 41.7 | | 25 | | MHz |
| f _{MAX2} | Data Path Maximum Frequency (1/(t _{WH} + t _{WL})) ^[8, 12] | 62.5 | | 50 | | 33.3 | | MHz |
| f _{MAX3} | Internal Feedback Maximum Frequency (1/(t _{CF} + t _S)) ^[8,13] | 62.5 | | 50 | | 33.3 | | MHz |
| t _{CF} | Register Clock to Feedback Input ^[8, 14] | | 6 | | 8 | | 10 | ns |
| t _{PR} | Power-Up Reset Time ^[8] | 1 | | 1 | | 1 | | μs |

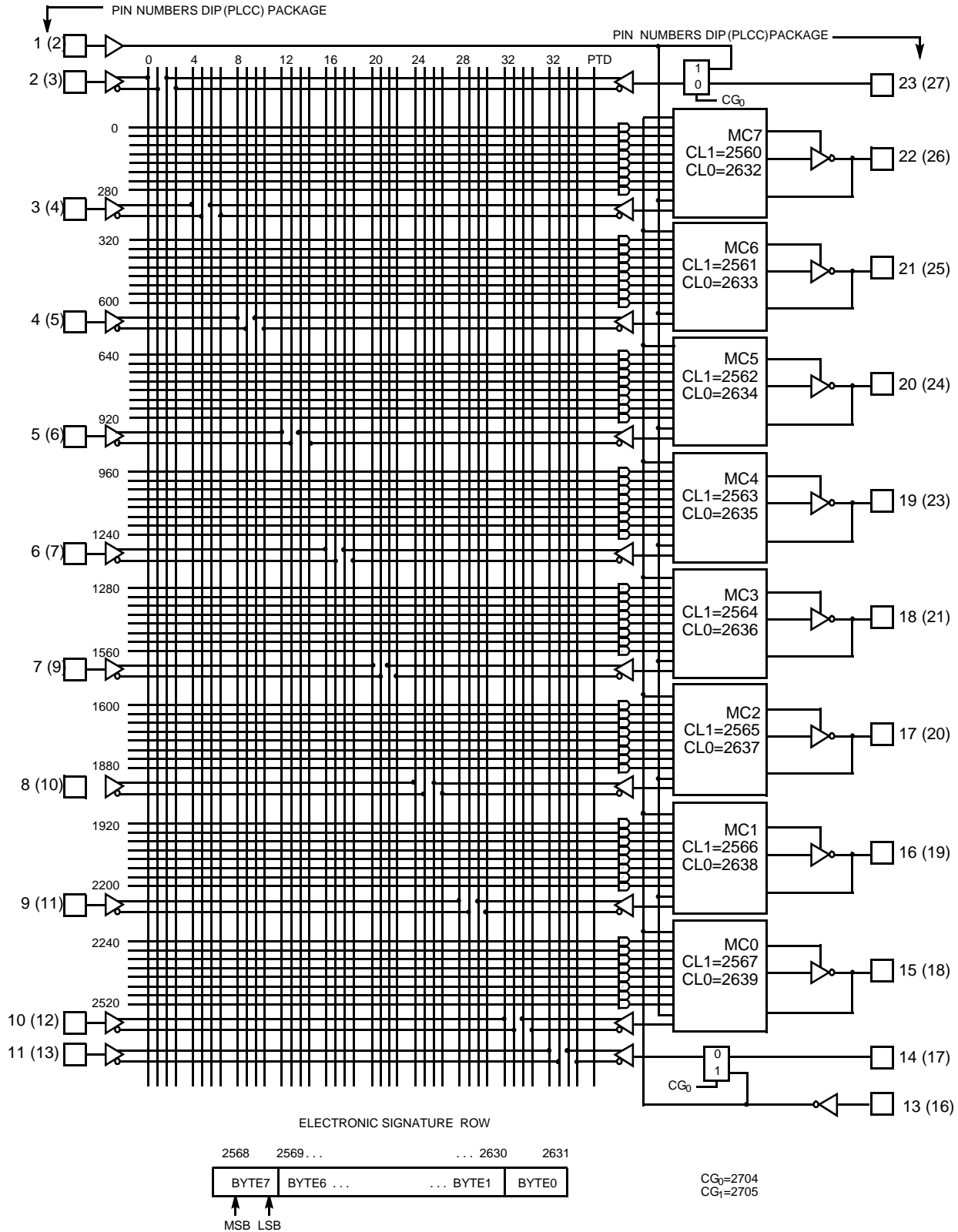
Switching Waveform



Power-Up Reset Waveform



Functional Logic Diagram for PALCE20V8



Ordering Information for PALCE20V8

| I_{CC} (mA) | t_{PD} (ns) | t_S (ns) | t_{CO} (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------------|------------------|---------------|------------------|-----------------|--------------|-------------------------------------|-----------------|
| 115 | 5 | 3 | 4 | PALCE20V8-5JC | J64 | 28-Lead Plastic Leaded Chip Carrier | Commercial |
| 115 | 7.5 | 7 | 5 | PALCE20V8-7JC | J64 | 28-Lead Plastic Leaded Chip Carrier | Commercial |
| | | | | PALCE20V8-7PC | P13 | 24-Lead (300-Mil) Molded DIP | |
| 115 | 10 | 10 | 7 | PALCE20V8-10JC | J64 | 28-Lead Plastic Leaded Chip Carrier | |
| | | | | PALCE20V8-10PC | P13 | 24-Lead (300-Mil) Molded DIP | |
| | | | | PALCE20V8-10QC | Q13 | 24-Lead Quarter-Size Outline | |
| 130 | 10 | 10 | 10 | PALCE20V8-10JI | J64 | 28-Lead Plastic Leaded Chip Carrier | Industrial |
| | | | | PALCE20V8-10PI | P13 | 24-Lead (300-Mil) Molded DIP | |
| | | | | PALCE20V8-10DMB | D14 | 24-Lead (300-Mil) CerDIP | Military |
| | | | | PALCE20V8-10LMB | L64 | 28-Pin Square Leadless Chip Carrier | |
| 90 | 15 | 12 | 10 | PALCE20V8-15JC | J64 | 28-Lead Plastic Leaded Chip Carrier | Commercial |
| | | | | PALCE20V8-15PC | P13 | 24-Lead (300-Mil) Molded DIP | |
| | | | | PALCE20V8-15QC | Q13 | 24-Lead Quarter-Size Outline | |
| 130 | 15 | 12 | 12 | PALCE20V8-15JI | J64 | 28-Lead Plastic Leaded Chip Carrier | Industrial |
| | | | | PALCE20V8-15PI | P13 | 24-Lead (300-Mil) Molded DIP | |
| | | | | PALCE20V8-15QI | Q13 | 24-Lead Quarter-Size Outline | |
| | | | | PALCE20V8-15DMB | D14 | 24-Lead (300-Mil) CerDIP | Military |
| | | | | PALCE20V8-15LMB | L64 | 28-Pin Square Leadless Chip Carrier | |
| 90 | 25 | 15 | 12 | PALCE20V8-25JC | J64 | 28-Lead Plastic Leaded Chip Carrier | Commercial |
| | | | | PALCE20V8-25PC | P13 | 24-Lead (300-Mil) Molded DIP | |
| | | | | PALCE20V8-25QC | Q13 | 24-Lead Quarter-Size Outline | |
| 130 | 25 | 20 | 20 | PALCE20V8-25JI | J64 | 28-Lead Plastic Leaded Chip Carrier | Industrial |
| | | | | PALCE20V8-25PI | P13 | 24-Lead (300-Mil) Molded DIP | |
| | | | | PALCE20V8-25QI | Q13 | 24-Lead Quarter-Size Outline | |
| | | | | PALCE20V8-25DMB | D14 | 24-Lead (300-Mil) CerDIP | Military |
| | | | | PALCE20V8-25LMB | L64 | 28-Pin Square Leadless Chip Carrier | |

Shaded areas contain preliminary information.

Ordering Information for PALCE20V8L

| I_{CC} (mA) | t_{PD} (ns) | t_S (ns) | t_{CO} (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------------|------------------|---------------|------------------|------------------|--------------|-------------------------------------|-----------------|
| 55 | 15 | 12 | 10 | PALCE20V8L-15JC | J64 | 28-Lead Plastic Leaded Chip Carrier | Commercial |
| | | | | PALCE20V8L-15PC | P13 | 24-Lead (300-Mil) Molded DIP | |
| | | | | PALCE20V8L-15QC | Q13 | 24-Lead Quarter-Size Outline | |
| 65 | 15 | 12 | 12 | PALCE20V8L-15JI | J64 | 28-Lead Plastic Leaded Chip Carrier | Industrial |
| | | | | PALCE20V8L-15PI | P13 | 24-Lead (300-Mil) Molded DIP | |
| | | | | PALCE20V8L-15QI | Q13 | 24-Lead Quarter-Size Outline | |
| | | | | PALCE20V8L-15DMB | D14 | 24-Lead (300-Mil) CerDIP | Military |
| | | | | PALCE20V8L-15LMB | L64 | 28-Pin Square Leadless Chip Carrier | |
| 55 | 25 | 15 | 12 | PALCE20V8L-25JC | J64 | 28-Lead Plastic Leaded Chip Carrier | Commercial |
| | | | | PALCE20V8L-25PC | P13 | 24-Lead (300-Mil) Molded DIP | |
| | | | | PALCE20V8L-25QC | Q13 | 24-Lead Quarter-Size Outline | |



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PALCE20V8

Ordering Information for PALCE20V8L (continued)

| I_{CC} (mA) | t_{PD} (ns) | t_S (ns) | t_{CO} (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|--------------------------------|--------------------------------|-------------------------------|--------------------------------|----------------------|---------------------|-------------------------------------|------------------------|
| 65 | 25 | 20 | 20 | PALCE20V8L-25JI | J64 | 28-Lead Plastic Leaded Chip Carrier | Industrial |
| | | | | PALCE20V8L-25PI | P13 | 24-Lead (300-Mil) Molded DIP | |
| | | | | PALCE20V8L-25QI | Q13 | 24-Lead Quarter-Size Outline | |
| | | | | PALCE20V8L-25DMB | D14 | 24-Lead (300-Mil) CerDIP | Military |
| | | | | PALCE20V8L-25LMB | L64 | 28-Pin Square Leadless Chip Carrier | |



**MILITARY SPECIFICATIONS
Group Subgroup Testing**

DC Characteristics

| Parameter | Subgroups |
|-----------------|-----------|
| V _{OH} | 1, 2, 3 |
| V _{OL} | 1, 2, 3 |
| V _{IH} | 1, 2, 3 |
| V _{IL} | 1, 2, 3 |
| I _{Ix} | 1, 2, 3 |
| I _{OZ} | 1, 2, 3 |
| I _{CC} | 1, 2, 3 |

Switching Characteristics

| Parameter | Subgroups |
|-----------------|-----------|
| t _{PD} | 9, 10, 11 |
| t _{CO} | 9, 10, 11 |
| t _S | 9, 10, 11 |
| t _H | 9, 10, 11 |

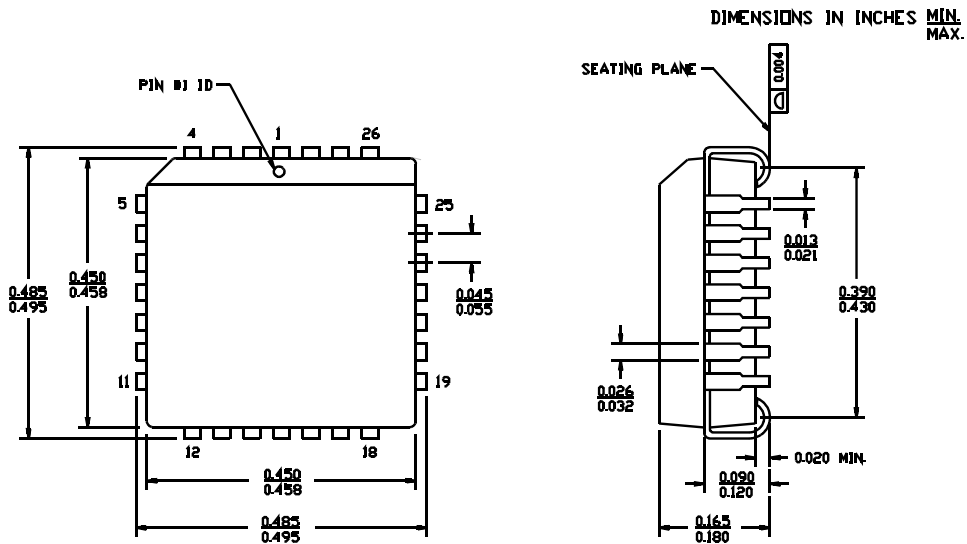
Package Diagrams

24-Lead (300-Mil) CerDIP D14
MIL-STD-1835 D-9 Config.A

51-80031-**

Package Diagrams (continued)

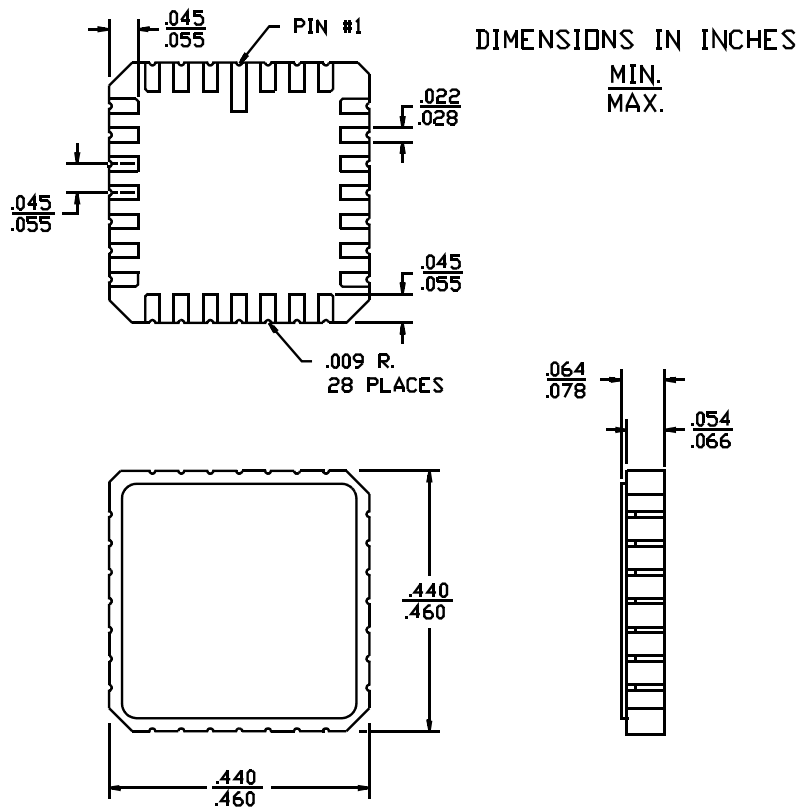
28-Lead Plastic Leaded Chip Carrier J64



51-85001-*A

28-Square Leadless Chip Carrier L64

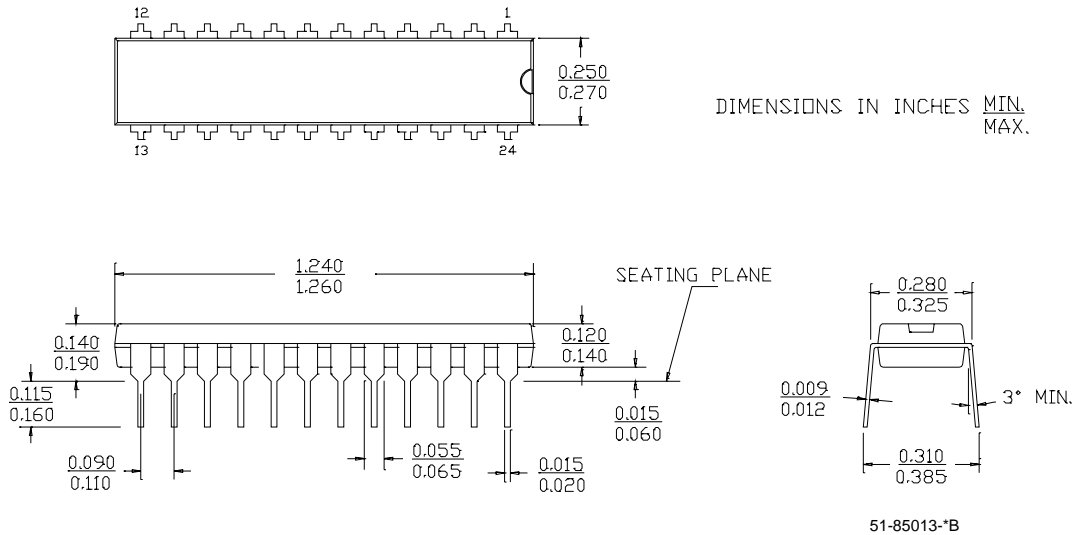
MIL-STD-1835 C-4



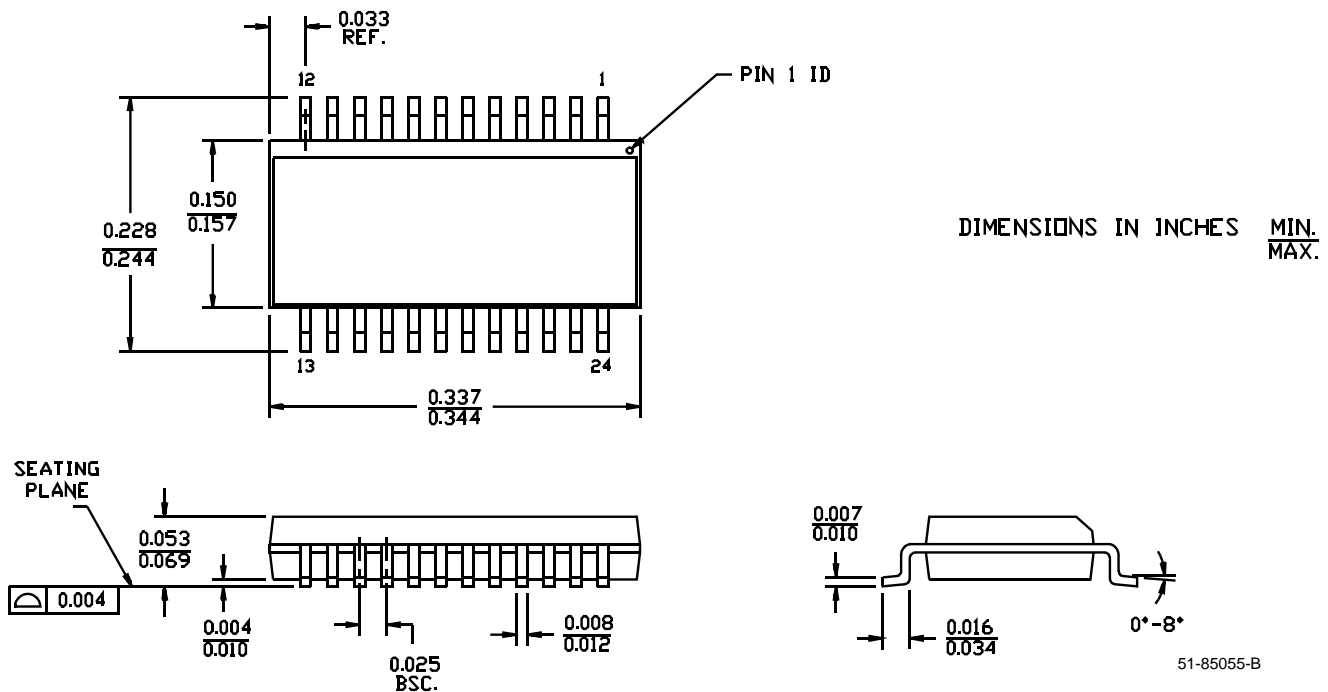
51-80051-**

Package Diagrams (continued)

24-Lead (300-Mil) PDIP P13



24-Lead Quarter Size Outline Q13



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PALCE20V8

Document History Page

| Document Title: PALCE20V8 Flash-Erasable Reprogrammable CMOS PAL® Device | | | | |
|---|----------------|-------------------|------------------------|--|
| Document Number: 38-03026 | | | | |
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 106371 | 07/11/01 | SZV | Changed from Spec Number: 38-00367 to 38-03026 |
| *A | 122231 | 12/28/02 | RBI | Added power-up requirements to Operating Range Information |
| *B | 213375 | See ECN | FSG | Added note to title page: "Use Ultra37000 For All New Designs" |