Reprogrammable CMOS PALC 16L8, 16R8, 16R6, 16R4

Features

- **CMOS EPROM technology for reprogrammability**
- **High performance at quarter power**
  - **— t_{PD} = 25 ns**
  - **— t_S = 20 ns**
  - **— t_{CO} = 15 ns**
  - **— I_{CC} = 45 mA**
- **High performance at military temperature**
  - **— t_{PD} = 20 ns**
  - **— t_S = 20 ns**
  - **— t_{CO} = 15 ns**
  - **— I_{CC} = 70 mA**
- **Commercial and military temperature range**
- **High reliability**
  - **— Proven EPROM technology**
  - **— >1500V input protection from electrostatic discharge**
  - **— 100% AC and DC tested**
  - **— 10% power supply tolerances**
  - **— High noise immunity**
  - **— Security feature prevents pattern duplication**
  - **— 100% programming and functional testing**

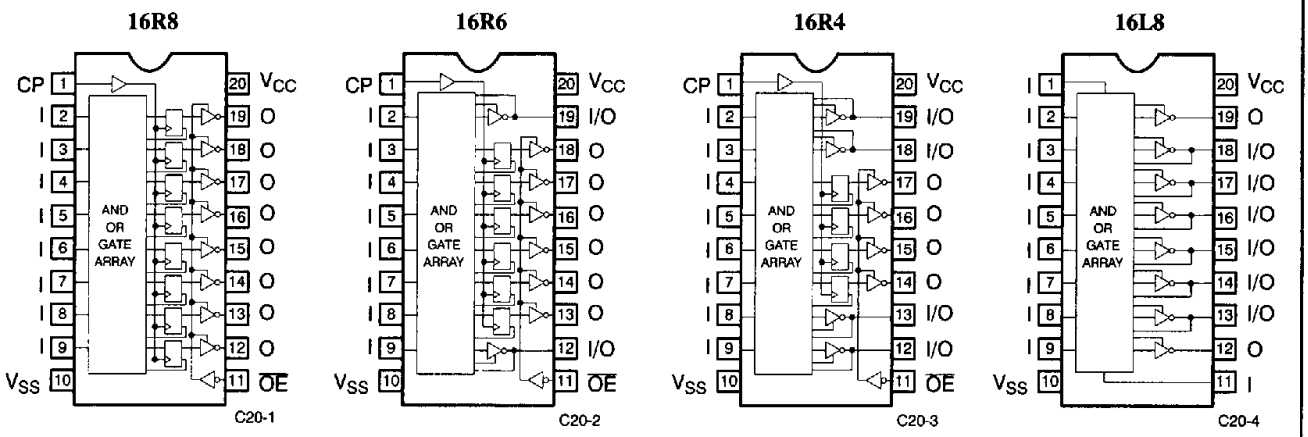
Functional Description

Cypress PALC20 Series devices are high-speed electrically programmable and UV-erasable logic devices produced in a proprietary N-well CMOS EPROM process. These devices utilize a sum-of-products (AND-OR) structure providing users with the ability to program custom logic functions serving unique requirements.

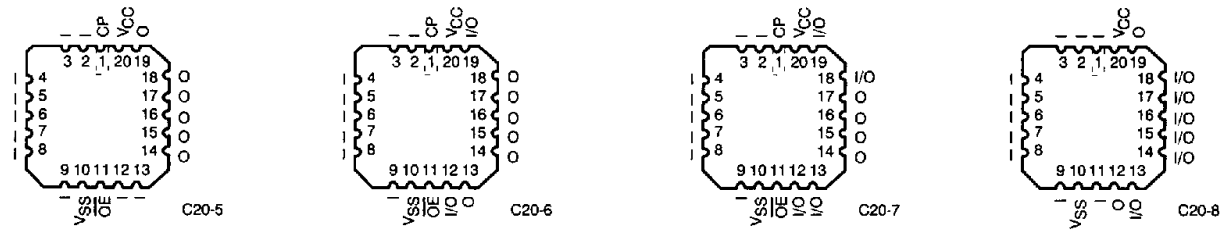
PALs are offered in 20-pin plastic and ceramic DIP, plastic SOJ, and ceramic LCC packages. The ceramic package can be equipped with an erasure window; when exposed to UV light, the PAL is erased and can then be reprogrammed.

Before programming, AND gates or product terms are connected via EPROM cells to both true and complement inputs. Programming an EPROM cell disconnects an input term from a product term. Selective programming of these cells allows a specific logic function to be implemented in a PALC device. PALC devices are supplied in four functional configurations designated 16R8, 16R6, 16R4, and 16L8. These 8 devices have potentially 16 inputs and 8 outputs configurable by the user. Output configurations of 8 registers, 8 combinatorial, 6 registers and 2 combinatorial as well as 4 registers and 4 combinatorial are provided by the 4 functional variations of the product family.

Logic Symbols and DIP and SOJ Pinouts



LCC Pinouts



PAL is a registered trademark of Advanced Micro Devices.

Functional Description (continued)

All combinatorial outputs on the 16R6 and 16R4 as well as 6 of the combinatorial outputs on the 16L8 may be used as optional inputs. All registered outputs have the $\overline{Q}$ bar side of the register fed back into the main array. The registers are automatically initialized upon power-up to Q output LOW and $\overline{Q}$ output HIGH. All unused inputs should be tied to ground.

All PALC devices feature a security function that provides the user with protection for the implementation of proprietary logic. When invoked, the contents of the normal array may no longer be accessed in the verify mode. Because EPROM technology is used as a storage mechanism, the content of the array is not visible under a microscope.

Cypress PALC products are produced in an advanced 1.2-micron N-well CMOS EPROM technology. The use of this proven EPROM technology is the basis for a superior product with inherent advantages in reliability, testability, programming, and functional yield. EPROM technology has the inherent advantage that all programmable elements may be programmed, tested, and erased during the manufacturing process. This also allows the device to be 100% functionally tested during manufacturing. An ability to preload the registers of registered devices during the testing operation makes the testing easier and more efficient. Combining these inherent and designed-in features provides an extremely high degree of functionality, programmability and assured AC performance, and testing becomes an easy task.

The register preload allows the user to initialize the registered devices to a known state prior to testing the device, significantly simplifying and shortening the testing procedure.

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Commercial and Industrial Selection Guide

Generic Part Number	Logic	Output Enable	Outputs	I_{CC} (mA)		t_{PD} (ns)		t_S (ns)		t_{CO} (ns)	
				L	Com'l/Ind	-25	-35	-25	-35	-25	-35
16L8	(8) 7-wide AND-OR-Invert	Programmable	(6) Bidirectional (2) Dedicated	45	70	25	35	—	—	—	—
16R8	(8) 8-wide AND-OR	Dedicated	Registered Inverting	45	70	—	—	20	30	15	25
16R6	(6) 8-wide AND-OR	Dedicated	Registered Inverting	45	70	25	35	20	30	15	25
	(2) 7-wide AND-OR-Invert	Programmable	Bidirectional								
16R4	(4) 8-wide AND-OR	Dedicated	Registered Inverting	45	70	25	35	20	30	15	25
	(4) 7-wide AND-OR-Invert	Programmable	Bidirectional								

Military Selection Guide

Generic Part Number	Logic	Output Enable	Outputs	I_{CC} (mA)	t_{PD} (ns)			t_S (ns)			t_{CO} (ns)		
					-20	-30	-40	-20	-30	-40	-20	-30	-40
16L8	(8) 7-wide AND-OR-Invert	Programmable	(6) Bidirectional (2) Dedicated	70	20	30	40	—	—	—	—	—	—
16R8	(8) 8-wide AND-OR	Dedicated	Registered Inverting	70	—	—	—	20	25	35	15	20	25
16R6	(6) 8-wide AND-OR	Dedicated	Registered Inverting	70	20	30	40	20	25	35	15	20	25
	(2) 7-wide AND-OR-Invert	Programmable	Bidirectional										
16R4	(4) 8-wide AND-OR	Dedicated	Registered Inverting	70	20	30	40	20	25	35	15	20	25
	(4) 7-wide AND-OR-Invert	Programmable	Bidirectional										

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with Power Applied ..... −55°C to +125°C
Supply Voltage to Ground Potential (Pin 20 to Pin 10) ..... −0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V
DC Input Voltage ..... −3.0V to +7.0V
Output Current into Outputs (LOW) ..... 24 mA
DC Programming Voltage 14.0V
UV Exposure ..... 7258 Wsec/cm^2
Static Discharge Voltage ..... >1500V (per MIL-STD-883, Method 3015)
Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%
Industrial	−40°C to +85°C	

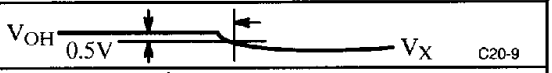
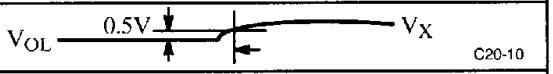
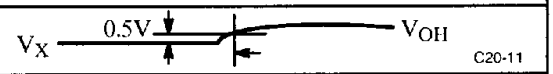
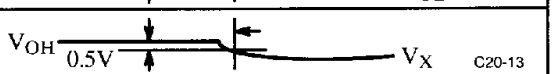
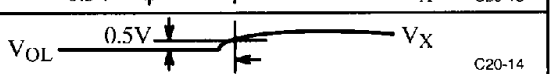
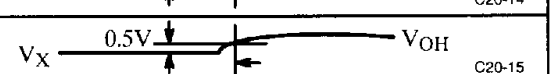
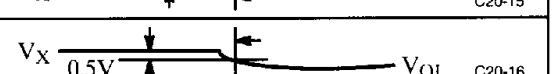
Electrical Characteristics Over the Operating Range (unless otherwise noted)[2]

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Com'l/Ind	2.4		V
			I_{OH} = −2 mA	Military			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA	Com'l/Ind		0.4	V
			I_{OL} = 12 mA	Military			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH[3] Voltage for All Inputs			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW[3] Voltage for All Inputs				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$			−10	10	μA
V_{PP}	Programming Voltage	I_{PP} = 50 mA Max.			13.0	14.0	V
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[4]				−300	mA
I_{CC}	Power Supply Current	All Inputs = GND, V_{CC} = Max., I_{OUT} = 0 mA[5]		"L"		45	mA
				Com'l/Ind		70	mA
				Military		70	mA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			−100	100	μA

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
5. $I_{CC(AC)}$ = (0.6 mA/MHz) × (Operating Frequency in MHz) + $I_{CC(DC)}$. $I_{CC(DC)}$ is measured with an unprogrammed device.

Electrical Characteristics Over the Operating Range (Unless Otherwise Noted)[2] (continued)

Parameter	V_X	Output Waveform—Measurement Level
t_{PXZ} (−)	1.5V	 C20-9
t_{PXZ} (+)	2.6V	 C20-10
t_{PZX} (+)	V_{thc}	 C20-11
t_{PZX} (−)	V_{thc}	 C20-12
t_{ER} (−)	1.5V	 C20-13
t_{ER} (+)	2.6V	 C20-14
t_{EA} (+)	V_{thc}	 C20-15
t_{EA} (−)	V_{thc}	 C20-16

Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{IN} = 0, V_{CC} = 5.0V	10	pF

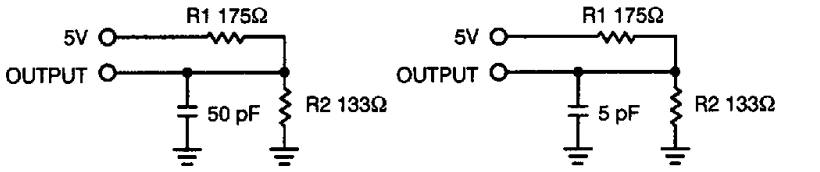
Switching Characteristics Over Operating Range[2, 7, 8]

Parameter	Description	Commercial/Industrial				Military						Unit
		−25		−35		−20		−30		−40		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output 16L8, 16R6, 16R4		25		35		20		30		40	ns
t_{EA}	Input to Output Enable 16L8, 16R6, 16R4		25		35		20		30		40	ns
t_{ER}	Input to Output Disable Delay 16L8, 16R6, 16R4		25		35		20		30		40	ns
t_{PZX}	Pin 11 to Output Enable 16R8, 16R6, 16R4		20		25		20		25		25	ns
t_{PXZ}	Pin 11 to Output Disable 16R8, 16R6, 16R4		20		25		20		25		25	ns
t_{CO}	Clock to Output 16R8, 16R6, 16R4		15		25		15		20		25	ns
t_S	Input or Feedback Set-Up Time 16R8, 16R6, 16R4	20		30		20		25		35		ns
t_H	Hold Time 16R8, 16R6, 16R4	0		0		0		0		0		ns
t_P	Clock Period	35		55		35		45		60		ns
t_W	Clock Width	15		20		12		20		25		ns
f_{MAX}	Maximum Frequency		28.5		18		28.5		22		16.5	MHz

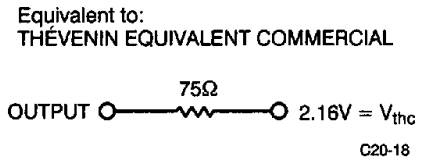
Notes:

6. Tested initially and after any design or process changes that may affect these parameters.
7. Part (a) (part (c) for military) of AC Test Loads and Waveforms is used for all parameters except t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}. Part (b) (part (d) for military) of AC Test Loads and Waveforms is used for t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}.
8. The parameters t_{ER} and t_{PXZ} are measured as the delay from the input disable logic threshold transition to V_{OH} − 0.5V for an enabled HIGH output or V_{OL} + 0.5V for an enabled LOW output. Please see Electrical Characteristics for waveforms and measurement reference levels.

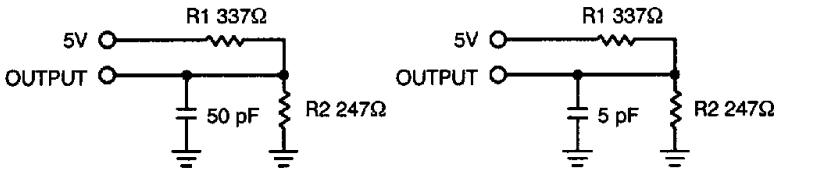
AC Test Loads and Waveforms



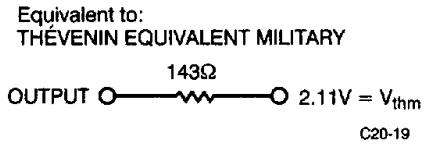
(a) Commercial (b) Commercial C20-17



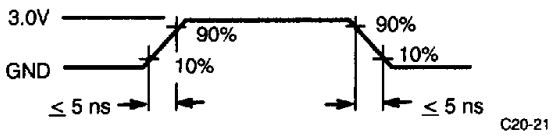
C20-18



(c) Military (d) Military C20-20



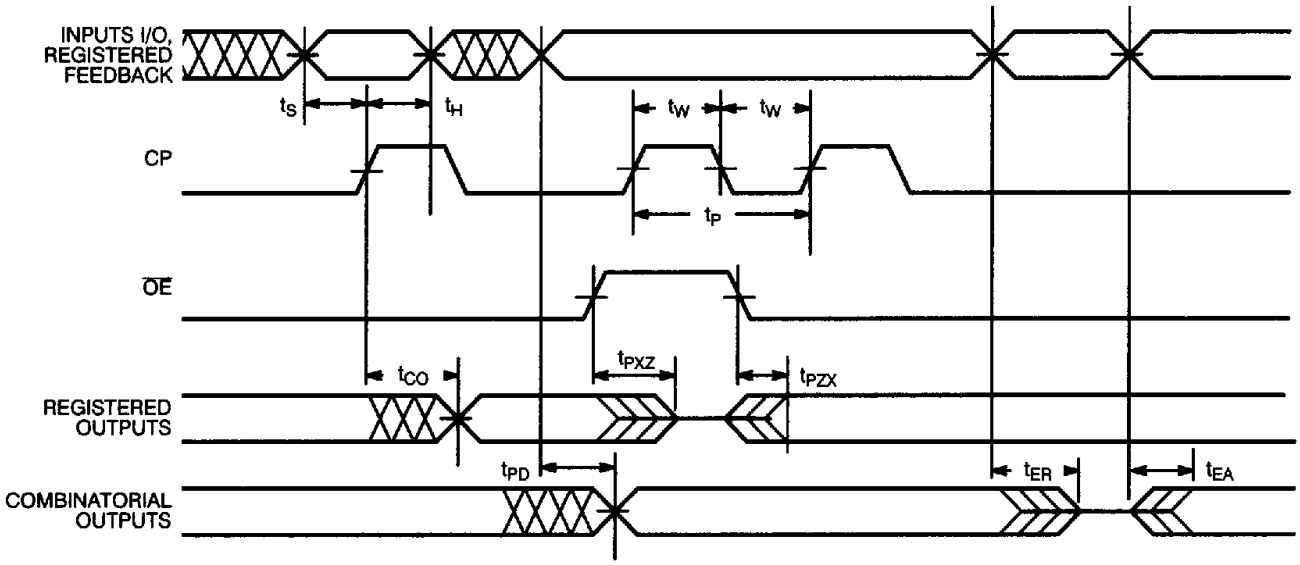
C20-19



C20-21

(e)

Switching Waveforms



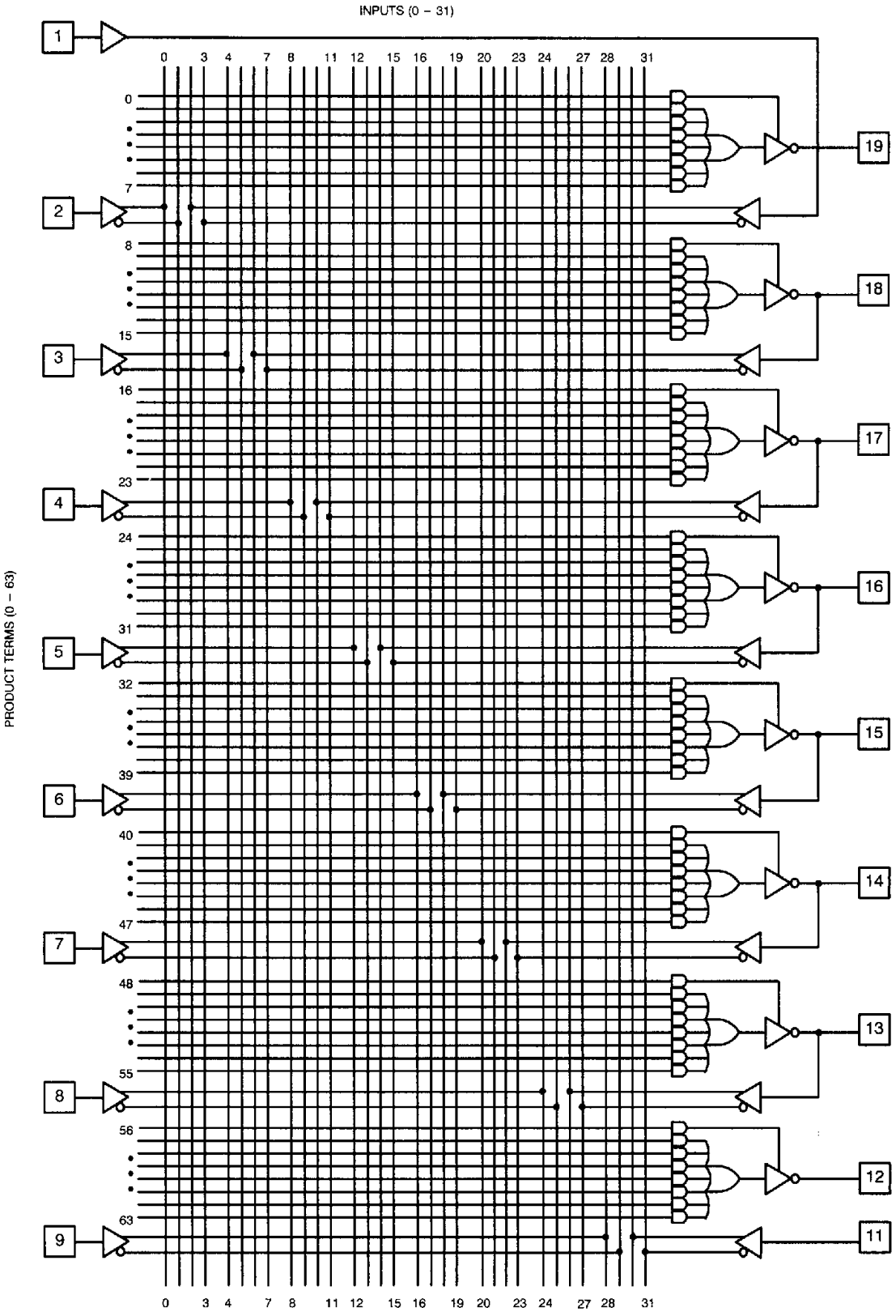
C20-22

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the PALC device. In addition, high ambient light levels can create hole-electron pairs that may cause "blank" check failures or "verify errors" when programming windowed parts. This phenomenon can be avoided by using an opaque label over the window during programming in high ambient light environments.

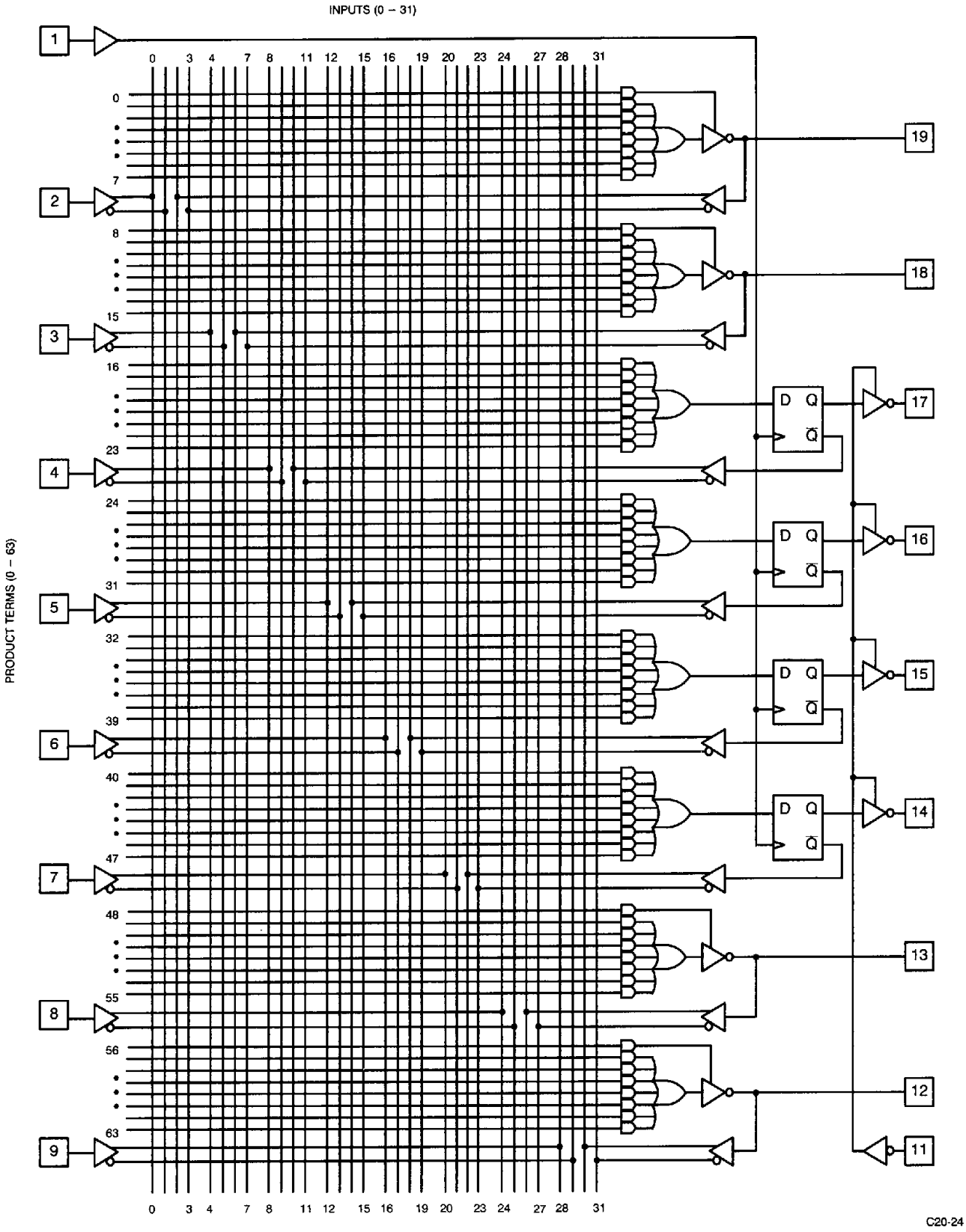
The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure would be approximately 35 minutes. The PALC device needs to be placed within 1 inch of the lamp during erasure. Permanent damage may result if the device is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Logic Diagram PALC16L8

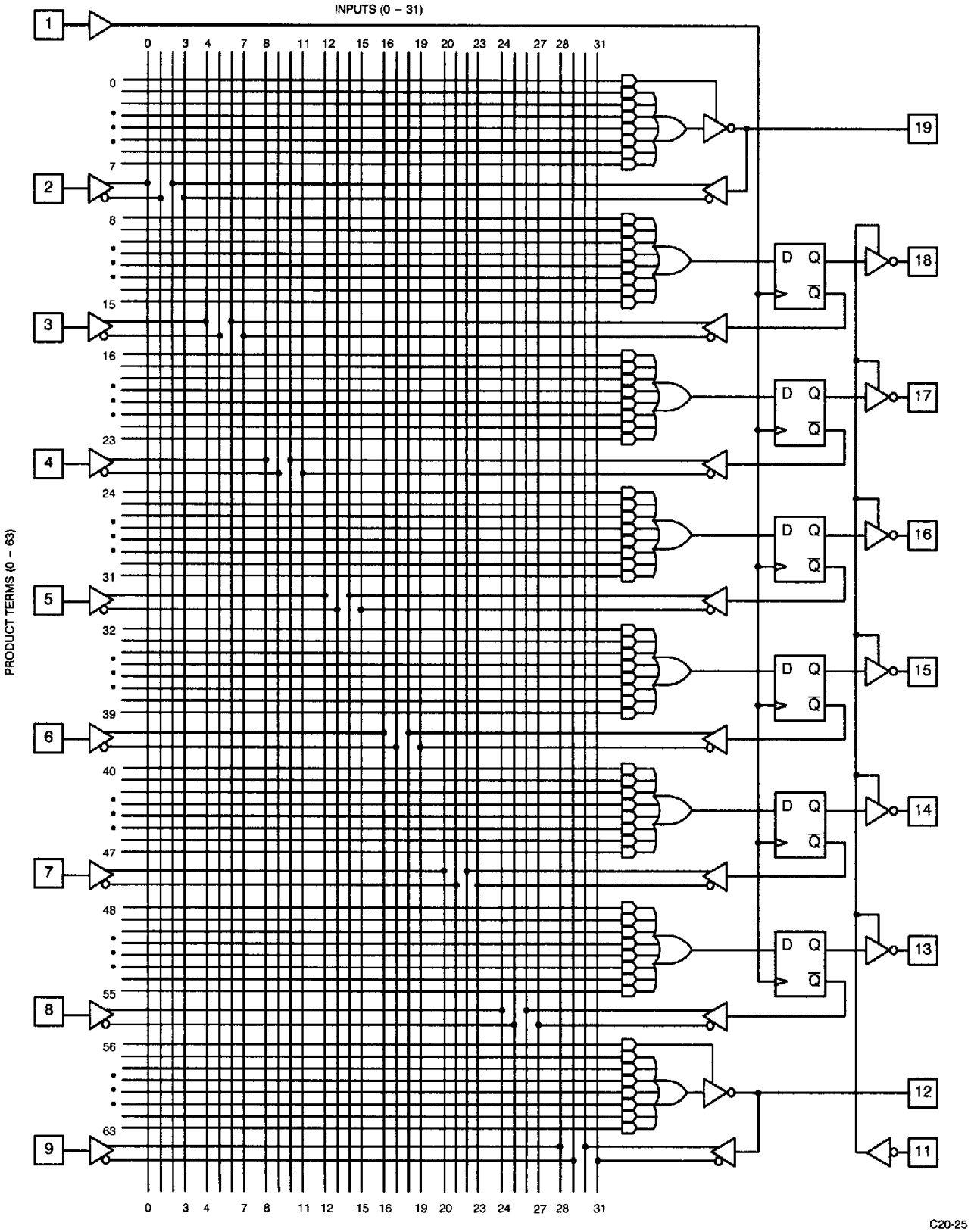


C20-23

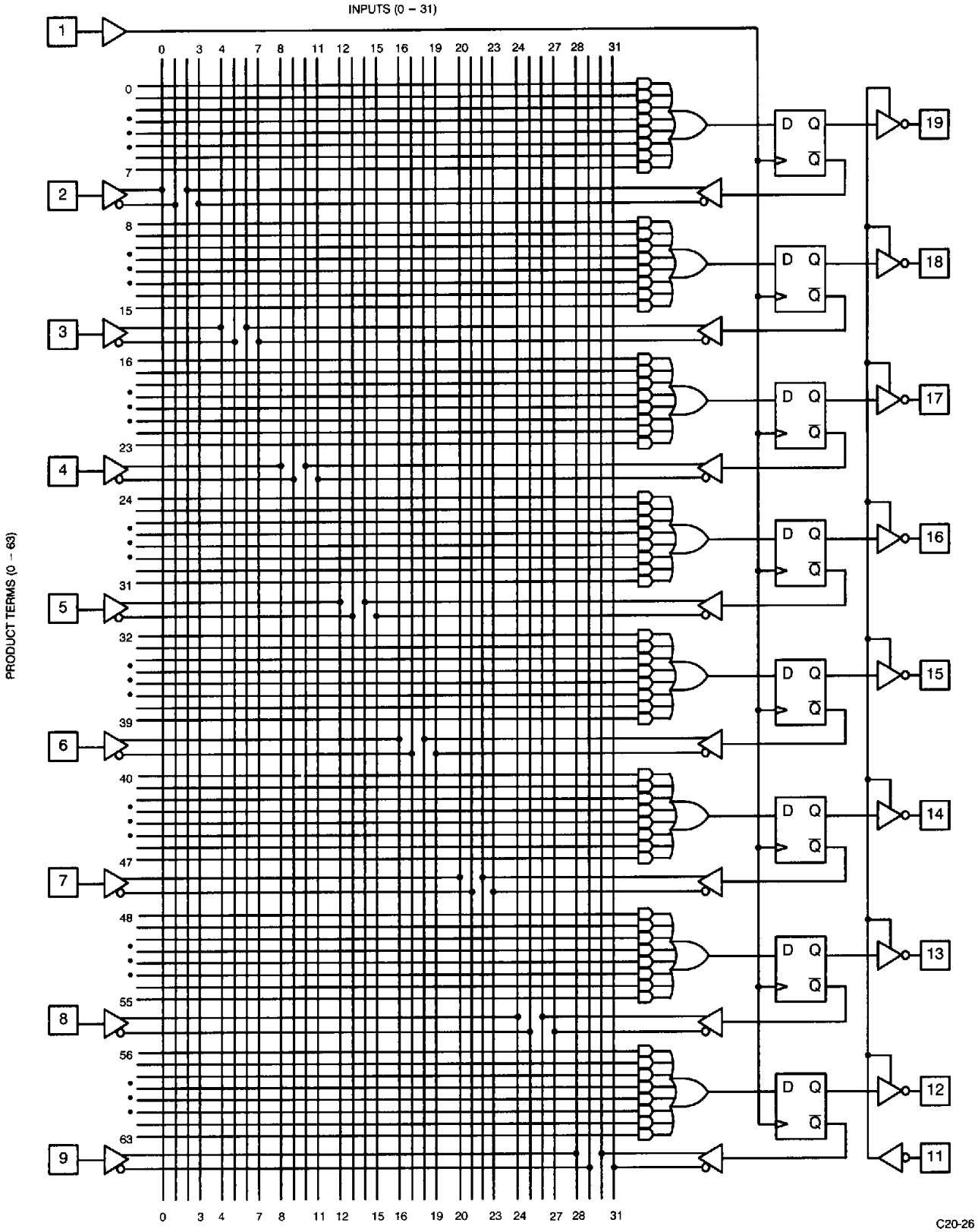
Logic Diagram PALC16R4



Logic Diagram PALC16R6

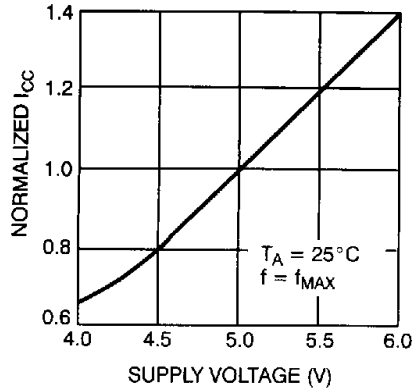


Logic Diagram PALC16R8

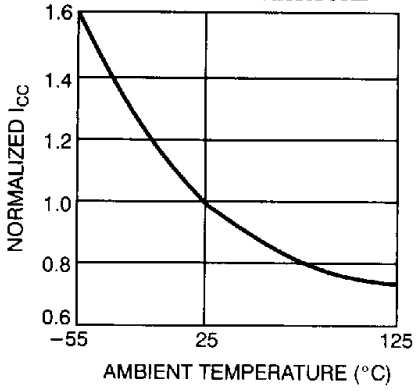


Typical DC and AC Characteristics

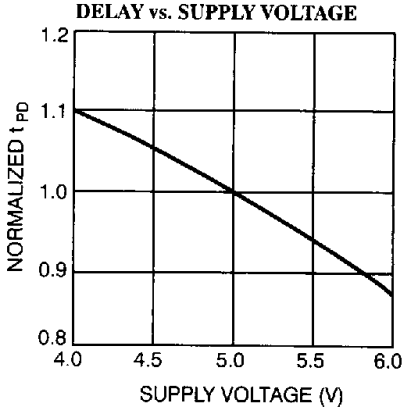
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



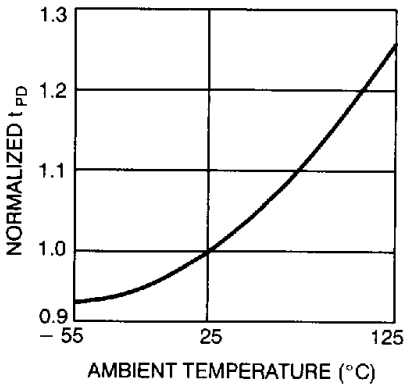
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



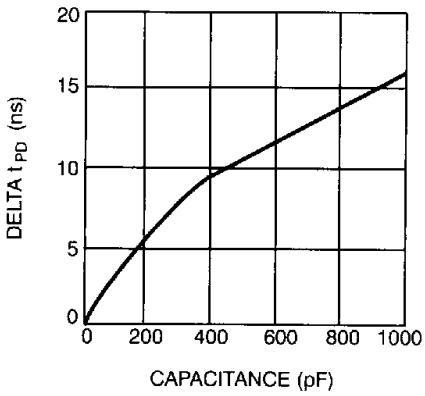
NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE



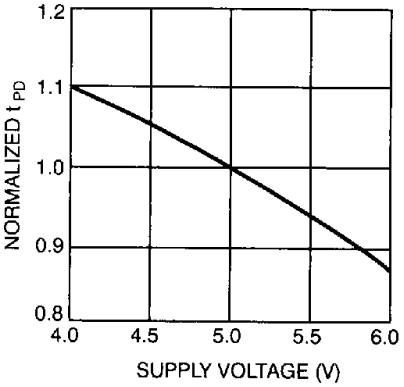
NORMALIZED PROPAGATION DELAY vs. TEMPERATURE



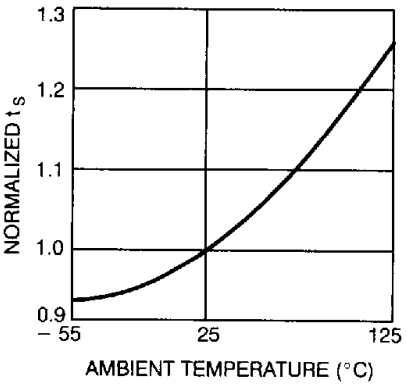
DELTA PROPAGATION TIME vs. OUTPUT LOADING



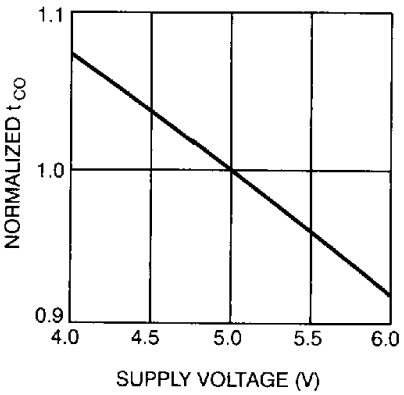
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



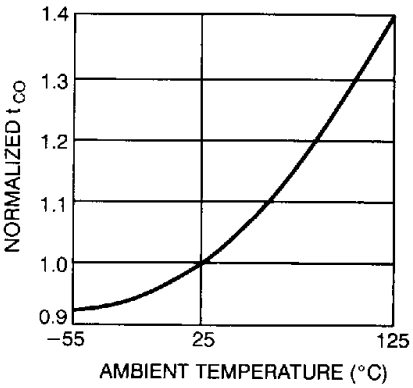
NORMALIZED SET-UP TIME vs. TEMPERATURE



NORMALIZED CLOCK-TO-OUTPUT TIME vs. SUPPLY VOLTAGE



NORMALIZED CLOCK-TO-OUTPUT TIME vs. TEMPERATURE



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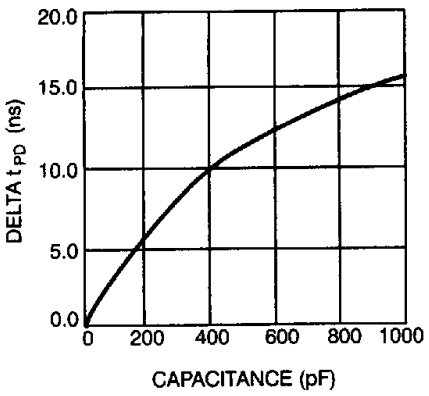
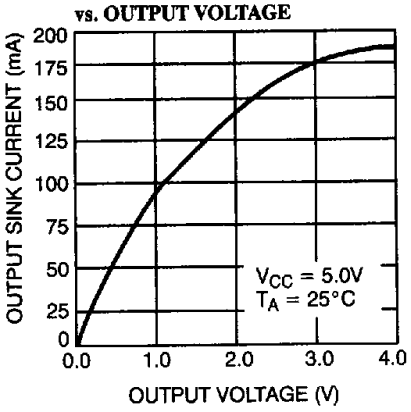
Typical DC and AC Characteristics (continued)

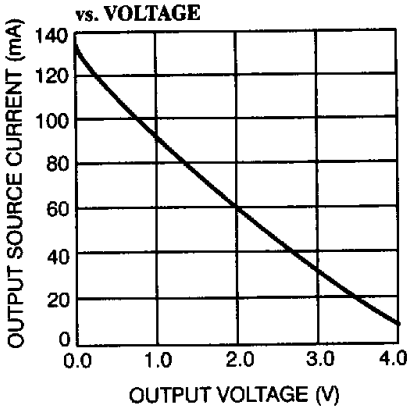
DELTA CLOCK-TO-OUTPUT TIME vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. VOLTAGE



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
20	—	—	70	PALC16L8–20DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16L8–20LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16L8–20QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16L8–20WMB	W6	20-Lead (300-Mil) Windowed CerDIP	
25	—	—	45	PALC16L8L–25PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
				PALC16L8L–25VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16L8L–25WC	W6	20-Lead (300-Mil) Windowed CerDIP	
			70	PALC16L8–25PC/PI	P5	20-Lead (300-Mil) Molded DIP	
				PALC16L8–25VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16L8–25WC	W6	20-Lead (300-Mil) Windowed CerDIP	
30	—	—	70	PALC16L8–30DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16L8–30LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16L8–30QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16L8–30WMB	W6	20-Lead (300-Mil) Windowed CerDIP	
35	—	—	45	PALC16L8L–35PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
				PALC16L8L–35VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16L8L–35WC	W6	20-Lead (300-Mil) Windowed CerDIP	
			70	PALC16L8–35PC/PI	P5	20-Lead (300-Mil) Molded DIP	
				PALC16L8–35VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16L8–35WC	W6	20-Lead (300-Mil) Windowed CerDIP	
40	—	—	70	PALC16L8–40DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16L8–40LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16L8–40QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16L8–40WMB	W6	20-Lead (300-Mil) Windowed CerDIP	

Ordering Information (continued)

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
20	20	15	70	PALC16R4–20DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16R4–20LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16R4–20QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16R4–20WMB	W6	20-Lead (300-Mil) Windowed CerDIP	
25	20	15	45	PALC16R4L–25PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
				PALC16R4L–25VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16R4L–25WC	W6	20-Lead (300-Mil) Windowed CerDIP	
			70	PALC16R4–25PC/PI	P5	20-Lead (300-Mil) Molded DIP	
				PALC16R4–25VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16R4–25WC	W6	20-Lead (300-Mil) Windowed CerDIP	
30	25	20	70	PALC16R4–30DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16R4–30LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16R4–30QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16R4–30WMB	W6	20-Lead (300-Mil) Windowed CerDIP	
35	30	25	45	PALC16R4L–35PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
				PALC16R4L–35VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16R4L–35WC	W6	20-Lead (300-Mil) Windowed CerDIP	
			70	PALC16R4–35PC/PI	P5	20-Lead (300-Mil) Molded DIP	
				PALC16R4–35VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16R4–35WC	W6	20-Lead (300-Mil) Windowed CerDIP	
40	35	25	70	PALC16R4–40DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16R4–40LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16R4–40QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16R4–40WMB	W6	20-Lead (300-Mil) Windowed CerDIP	

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Ordering Information (continued)

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
20	20	15	70	PALC16R6–20DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16R6–20LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16R6–20QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16R6–20WMB	W6	20-Lead (300-Mil) Windowed CerDIP	
25	20	15	45	PALC16R6L–25PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
				PALC16R6L–25VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16R6L–25WC	W6	20-Lead (300-Mil) Windowed CerDIP	
			70	PALC16R6–25PC/PI	P5	20-Lead (300-Mil) Molded DIP	
				PALC16R6–25VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16R6–25WC	W6	20-Lead (300-Mil) Windowed CerDIP	
30	25	20	70	PALC16R6–30DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16R6–30LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16R6–30QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16R6–30WMB	W6	20-Lead (300-Mil) Windowed CerDIP	
35	30	25	45	PALC16R6L–35PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
				PALC16R6L–35VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16R6L–35WC	W6	20-Lead (300-Mil) Windowed CerDIP	
			70	PALC16R6–35PC/PI	P5	20-Lead (300-Mil) Molded DIP	
				PALC16R6–35VC	V5	20-Lead (300-Mil) Molded SOJ	
				PALC16R6–35WC	W6	20-Lead (300-Mil) Windowed CerDIP	
40	35	25	70	PALC16R6–40DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16R6–40LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16R6–40QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16R6–40WMB	W6	20-Lead (300-Mil) Windowed CerDIP	

Ordering Information (continued)

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
—	20	15	70	PALC16R8–20DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16R8–20LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16R8–20QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16R8–20WMB	W6	20-Lead (300-Mil) Windowed CerDIP	
—	20	15	45	PALC16R8L–25PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
				PALC16R8L–25WC	W6	20-Lead (300-Mil) Windowed CerDIP	
			70	PALC16R8–25PC/PI	P5	20-Lead (300-Mil) Molded DIP	
				PALC16R8–25WC	W6	20-Lead (300-Mil) Windowed CerDIP	
—	25	20	70	PALC16R8–30DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16R8–30LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16R8–30QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16R8–30WMB	W6	20-Lead (300-Mil) Windowed CerDIP	
—	30	25	45	PALC16R8L–35PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
				PALC16R8L–35WC	W6	20-Lead (300-Mil) Windowed CerDIP	
			70	PALC16R8–35PC/PI	P5	20-Lead (300-Mil) Molded DIP	
				PALC16R8–35WC/WC	W6	20-Lead (300-Mil) Windowed CerDIP	
—	35	25	70	PALC16R8–40DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALC16R8–40LMB	L61	20-Pin Square Leadless Chip Carrier	
				PALC16R8–40QMB	Q61	20-Pin Windowed Square Leadless Chip Carrier	
				PALC16R8–40WMB	W6	20-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
V_{PP}	1, 2, 3
I_{CC}	1, 2, 3
I_{OZ}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{PZX}	9, 10, 11
t_{CO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11

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