REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Boilerplate update, part of 5 year review. ksr	07-04-02	Robert M. Heber

REV																				
SHEET																				
REV	A	A	A	A	A															
SHEET	15	16	17	18	19															
REV STATUS				REV			A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
94-04-21

REVISION LEVEL
A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, UV ERASEABLE PROGRAMMABLE LOGIC ARRAY, MONOLITHIC SILICON

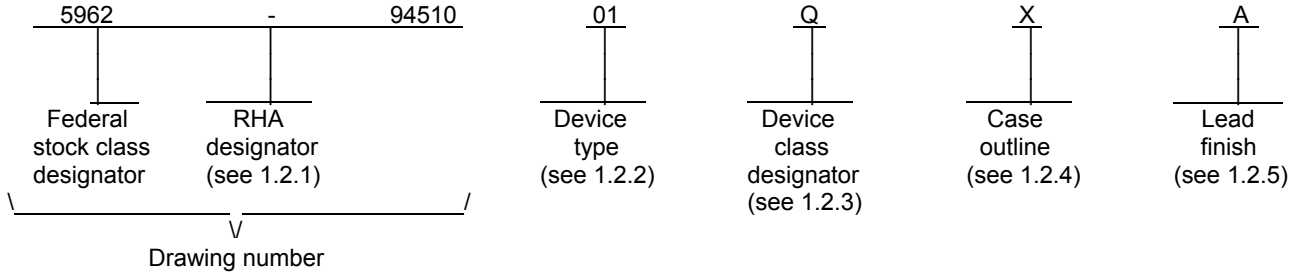
SIZE	CAGE CODE	
A	**67268**	**5962-94510**

SHEET 1 OF 19

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	f_{MAX3}
01	7C335	12 macrocell EPLD	50 MHz
02	7C335	12 macrocell EPLD	66 MHz
03	7C335	12 macrocell EPLD	83 MHz

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDIP3-T28 or GDIP4-T28	28	Dual-in-line package 1/
Y	GQCC1-J28	28	"J" lead chip carrier 1/
Z	CQCC1-N28	28	Square leadless chip carrier 1/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Lid shall be transparent to permit ultraviolet light erasure.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-2.0 V dc to +7.0 V dc 4/
Output voltage range applied	-0.5 V dc to +7.0 V dc 4/
Output sink current	12 mA
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Maximum power dissipation (P_D) 5/	1.1 W
Maximum junction temperature	+175°C
Lead temperature (soldering, 10 seconds maximum)	+300°C
Data retention	10 years (minimum)
Endurance	25 erase/write cycles (minimum)

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc maximum
Supply voltage (V_{SS})	0.0 V dc
High level input voltage (V_{IH})	2.2 V dc minimum
Low level input voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil from the Standardization Document Order Desk, 700 Robins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ All voltages referenced to V_{SS}.

4/ Minimum voltage is -0.6 V dc which may undershoot to -2.0 V dc for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} +0.75 V dc which may overshoot to +7.0 V dc for pulses of less than 20 ns.

5/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-00 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; http://www.astm.org.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201; http://www.jedec.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s).

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in screening (see 4.2 herein) or quality conformance inspection group A, C, D, or E (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test with a minimum of 50 percent of the total number of gates programmed or to any altered item drawing pattern which includes at least 25 percent of the total number of gates programmed.

3.2.3.2 Programmed devices. The requirements for supplying programmed devices shall be as specified by an attached item drawing.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Processing EPLDS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.6.1 Erasure of EPLDS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.6.

3.6.2 Programmability of EPLDS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.7.

3.6.3 Verification of erasure or programmed EPLDS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.7 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract.

3.7.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.7.2 Manufacturer programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.8 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.9 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.10 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.11 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.12 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.13 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitor. This reprogrammability test shall be done only for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but will guarantee the number of program/erase endurance cycles listed in section 1.3 herein. The vendor's procedure shall be under document control and shall be made available upon request.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions V_{SS} = O V 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.8 V I_O = -2.0 mA, V_{IH} = 2.2 V	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, V_{IL} = 0.8 V I_O = 8.0 mA, V_{IH} = 2.2 V	1, 2, 3	All		0.5	V
High impedance output leakage current	I_{OZ}	V_{CC} = 5.5 V	1, 2, 3	All	-40	40	µA
High level input current	I_{IH}	V_{IN} = 5.5 V	1, 2, 3	All		10	µA
Low level input current	I_{IL}	V_{IN} = GND	1, 2, 3	All	-10		µA
Supply current	I_{CC}	V_{CC} = 5.5 V, V_{IN} = GND Outputs open	1, 2, 3	All		160	mA
Output short circuit current 1/ 2/	I_{OS}	V_{CC} = 5.5 V, V_O = 0.5 V	1, 2, 3	All	-30	-90	mA
Input capacitance 2/	C_I	V_I = 2.0 V, V_{CC} = 5.0 V T_A = +25°C, f = 1.0 MHz see 4.4.1e	4	All		10	pF
Output capacitance 2/	C_O	V_O = 2.0 V, V_{CC} = 5.0 V T_A = +25°C, f = 1.0 MHz see 4.4.1e	4	All		10	pF
Functional tests		see 4.4.1c	7,8A,8B	All			
Input to output propagation delay	t_{PD}	V_{CC} = 4.5 V, C_L = 50 pF See figures 3 and 4 (circuit A) 3/	9, 10, 11	01 02 03		25 20 20	ns
Input to output enable 2/ 4/	t_{EA}		9, 10, 11	01 02 03		25 20 20	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{SS} = O V, 4.5 V ≤ V_{CC} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Input to output disable 2/ 4/	t_{ER}	V_{CC} = 4.5 V, C_L = 50 pF See figures 3 and 4 (circuit A) 3/	9, 10, 11	01		25	ns
				02		20	
				03		20	
Input registered mode parameters							
Input and output clock width high 2/	t_{WH}	V_{CC} = 4.5 V, C_L = 50 pF See figures 3 and 4 (circuit A) 3/	9, 10, 11	01	8		ns
				02	6		
				03	5		
Input and output clock width low 2/	t_{WL}		9, 10, 11	01	8		
				02	6		
				03	5		
Input or feedback set-up time to input clock	t_{IS}		9, 10, 11	All	3		
Input register hold time from input clock 2/	t_{IH}		9, 10, 11	All	3		
Input register clock to output delay	t_{ICO}		9, 10, 11	01		25	
				02		23	
				03		23	
Output data stable time from input clock 2/	t_{IOH}		9, 10, 11	All	3		
Output data stable from input clock minus input register hold time 2/ 5/	t_{IOH}-t_{IH}		9, 10, 11	All	0		
Pin 14 enable to output enabled 2/ 4/	t_{PZX}		9, 10, 11	01		20	
				02		15	
				03		15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{SS} = O V, 4.5 V ≤ V_{CC} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Pin 14 disable to output disabled 2/ 4/	t_{PXZ}	V_{CC} = 4.5 V, C_L = 50 pF See figures 3 and 4 (circuit A) 3/	9, 10, 11	01		20	ns
				02		15	
				03		15	
Maximum frequency of two devices in input registered mode lowest of $1/t_{ICO}+t_{IS}$ or $1/t_{WL}+t_{WH}$ 2/	f_{MAX1}		9, 10, 11	01	35.7		MHz
				02	38.4		
				03	38.4		
Maximum frequency data path in input registered mode lowest of $1/t_{ICO}$ or $1/t_{WL}+t_{WH}$ or $1/t_{IS}+t_{IH}$ 2/	f_{MAX2}		9, 10, 11	01	40		
				02	43.4		
				03	43.4		
Input clock to output enable 2/ 4/	t_{ICEA}		9, 10, 11	01		25	ns
				02		20	
				03		20	
Input clock to output disabled 2/ 4/	t_{ICER}		9, 10, 11	01		25	
				02		20	
				03		20	
Output registered mode parameters							
Output clock to output enabled 2/ 4/	t_{CEA}	V_{CC} = 4.5 V, C_L = 50 pF See figures 3 and 4 (circuit A) 3/	9, 10, 11	01		25	ns
				02		20	
				03		20	
Output clock to output disabled 2/ 4/	t_{CER}		9, 10, 11	01		25	ns
				02		20	
				03		20	
Output register input set-up time to output clock	t_S		9, 10, 11	01	15		
				02	12		
				03	10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{SS} = O V 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output register input hold time from output clock	t_H	V_{CC} = 4.5 V, C_L = 50 pF See figures 3 and 4 (circuit A) 3/	9, 10, 11	All	0		ns
Output register clock to output delay	t_{CO}		9, 10, 11	01		15	
				02		12	
				03		11	
Output register clock or latch enable to combinatorial output delay 2/	t_{CO2}		9, 10, 11	01		30	
				02		23	
				03		22	
Output data stable time from output clock 2/	t_{OH}		9, 10, 11	All	2		
Output data stable time from output clock 2/	t_{OH2}		9, 10, 11	All	3		
Output data stable time from output clock minus input register hold time 2/ 5/	t_{OH2}-t_{IH}		9, 10, 11	All	0		
Maximum frequency with internal feedback in output registered mode 2/	f_{MAX3}		9, 10, 11	01	50.0		MHz
				02	66.6		
				03	83.3		
Maximum frequency of 2 devices in output registered mode 2/	f_{MAX4}		9, 10, 11	01	33.3		
				02	41.6		
				03	47.6		
Maximum frequency data path in output registered mode 2/	f_{MAX5}		9, 10, 11	01	62.5		
				02	83.3		
				03	90.9		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{SS} = O V 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Pipelined mode parameters							
Input clock to Output clock	t_{COS}	V_{CC} = 4.5 V, C_L = 50 pF See figures 3 and 4 (circuit A) 3/	9, 10, 11	01	20		ns
				02	15		
				03	12		
Maximum frequency pipelined mode 2/	f_{MAX6}		9, 10, 11	01	50.0		MHz
				02	66.6		
				03	83.3		
Maximum frequency of 2 devices in pipelined mode 2/	f_{MAX7}		9, 10, 11	01	50.0		
				02	66.6		
				03	71.4		
Power-up reset time 2/ 6/	t_{POR}		9, 10, 11	All	0	1	µs

1/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed one second. Vout = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

2/ Tested initially and after any design or process changes that may affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

3/ AC tests are performed with input rise and fall times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load in figure 3A unless otherwise noted.

4/ See figure 3 test load B.

5/ This specification guarantees interface compatibility with other members of the device family. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.

6/ This device has been designed with the capability to reset during system power-up. Following power-up, the input and output registers will be reset to a logic low state. The output state will depend on how the array is programmed.

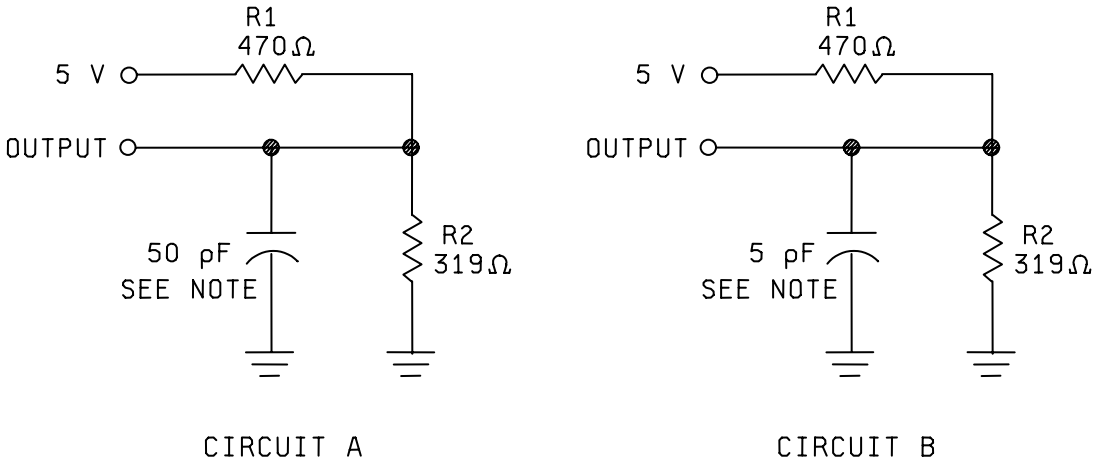
Device Types	All
Case Outlines	X,Y, and Z
Terminal Number	Terminal Symbol
1	CLK_1
2	I_0 / CLK_2
3	I_1 / CLK_3
4	I_2
5	I_3
6	I_4
7	I_5
8	V_{SS}
9	I_6
10	I_7
11	I_8
12	I_9
13	I_{10}
14	$\overline{OE}$ / I_{11}
15	I/O_{11}
16	I/O_{10}
17	I/O_9
18	I/O_8
19	I/O_7
20	I/O_6
21	V_{SS}
22	V_{CC}
23	I/O_5
24	I/O_4
25	I/O_3
26	I/O_2
27	I/O_1
28	I/O_0

FIGURE 1. Terminal connections.

Truth table												
Input pins												
CLK_1	I_0 /CLK_2	I_1 /CLK_3	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	$\overline{OE}$ /I_{11}
X	X	X	X	X	X	X	X	X	X	X	X	X
Output pins												
I/O_{11}	I/O_{10}	I/O_9	I/O_8	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	
Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	

NOTES:
1. Z = High impedance.
2. X = Don't care.

FIGURE 2. Truth table (unprogrammed).



NOTE: Including scope and jig (minimum values).

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall levels	≤ 3 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

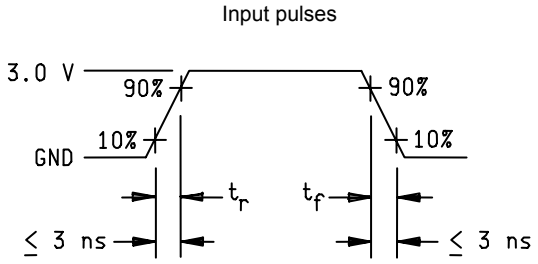


FIGURE 3. Output load circuits and test conditions.

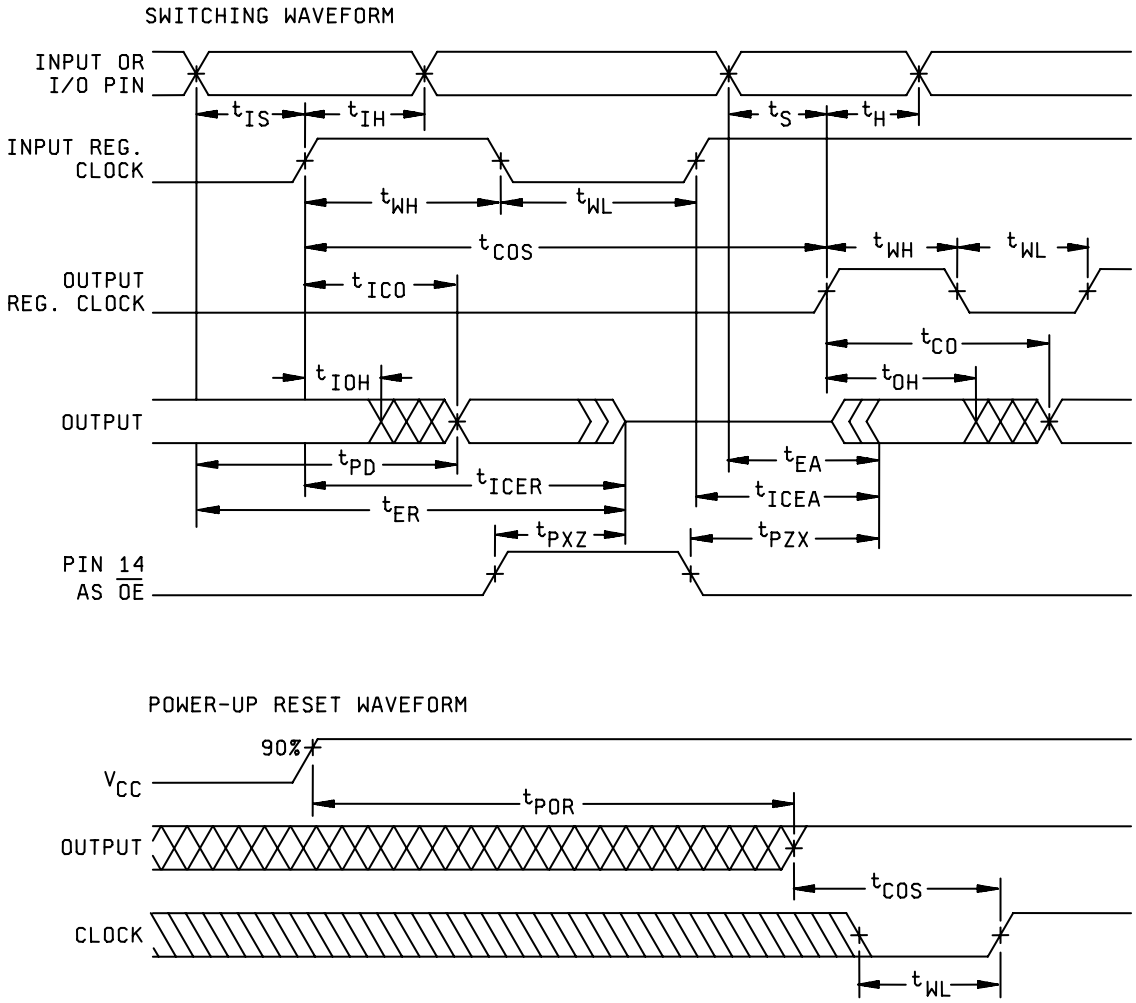


FIGURE 4. Timing waveforms.

3.14 Data retention. A data retention stress test shall be completed as part of the vendor's reliability process. This test shall be done initially and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but will guarantee the number of years listed in section 1.3 herein. The vendors' procedure shall be under document control and shall be made available upon request. Data retention capability shall be guaranteed over the full military temperature range.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. Prior to burn-in, the devices shall be programmed (see 4.7 herein) with a checkerboard pattern or equivalent (manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern). The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be included in the Percent Defective Allowable (PDA) calculation and shall be removed from the lot. The manufacturer as an option may use built-in test circuitry by testing the entire lot to verify programmability and AC performance without programming the user array.

c. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

d. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7, 8A, and 8B tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD78 may be used for reference.

e. Subgroup 4 (C_I and C_O measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency equal or less than 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

f. Devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.3.2). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9	1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B Δ	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d and also 4.4.1f.

Table IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{IL2}	±1% of specified value in table I
I_{IH2}	±1% of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ± 5°C, after exposure, to the subgroups specified in table IIA herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Erasing procedure. The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2,537 Angstroms (Ä). The integrated dose (i.e., ultraviolet intensity times exposure time) for erasure should be minimum of 15 Ws/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 $\mu W/cm^2$ power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7,258 Ws/cm^2 (1 week at 12,000 $\mu W/cm^2$). Exposure of the device to high intensity ultraviolet light for long periods may cause permanent damage.

4.7 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

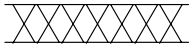
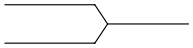
6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Symbols, definitions, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-STD-1331, and as follows:

C_I, C_O ..... Input and bidirectional output, terminal-to-GND capacitance.
GND ..... Ground zero voltage potential.
I_{CC} ..... Supply current.
I_{LI} ..... Input load current.
T_C ..... Case temperature.
T_A ..... Ambient temperature.
V_{CC} ..... Positive supply voltage.
O/V ..... Latch-up over-voltage

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. For example, address setup time would be shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. For example, the access time would be shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-04-02

Approved sources of supply for SMD 5962-94510 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9451001MXA	0C7V7	CY7C335-50WMB
5962-9451001MYA	0C7V7	CY7C335-50HMB
5962-9451001MZA	0C7V7	CY7C335-50QMB
5962-9451002MXA	0C7V7	CY7C335-66WMB
5962-9451002MYA	0C7V7	CY7C335-66HMB
5962-9451002MZA	0C7V7	CY7C335-66QMB
5962-9451003MXA	0C7V7	CY7C335-83WMB
5962-9451003MYA	0C7V7	CY7C335-83HMB
5962-9451003MZA	0C7V7	CY7C335-83QMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.