REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R166-92	92-03-30	Michael A. Frye
B	Boilerplate update, part of 5 year review. ksr	06-12-11	Raymond Monnin

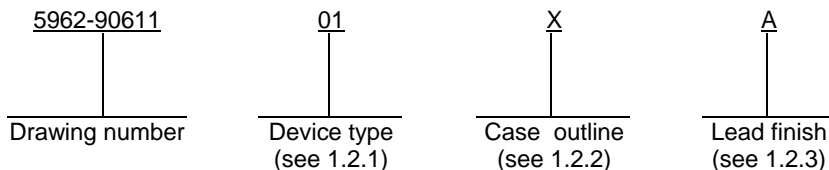THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																	
SHEET																	
REV	B	B															
SHEET	15	16															

REV STATUS		REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS		SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY James E. Jamison	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**		
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Kenneth Rice			
	APPROVED BY Michael A. Frye	MICROCIRCUIT, MEMORY, DIGITAL, CMOS UV ERASABLE PROGRAMMABLE LOGIC DEVICE, MONOLITHIC SILICON		
	DRAWING APPROVAL DATE 91-01-21			
	REVISION LEVEL B	SIZE A	CAGE CODE **67268**	**5962-90611**
		SHEET 1 OF 16		

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5962-E012-07

1. SCOPE

1.1 <u>Scope</u>. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 <u>Part or Identifying Number (PIN)</u>. The complete PIN is as shown in the following example:

```
5962-90611          01               X               A
    |                |                |               |
    |                |                |               |
____|____       _____|_____      _____|_____      ____|____
Drawing number  Device type     Case  outline    Lead finish
                (see 1.2.1)      (see 1.2.2)      (see 1.2.3)
```

1.2.1 <u>Device type(s)</u>. The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	t_{PD}
01		32-Macrocell EPLD	35 ns
02		32-Macrocell EPLD	25 ns

1.2.2 <u>Case outline(s)</u>. The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style	
X	GDIP4-T28 or CDIP3-T28	28	dual-in-line package	2/
Y	GQCC1-J28	28	J leaded chip carrier package	2/

1.2.3 <u>Lead finish</u>. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 <u>Absolute maximum ratings</u>.

Supply voltage to ground potential .... -2.0 V dc to +7.0 V dc
DC input voltage .... -2.0 V dc to +7.0 V dc
Maximum power dissipation 3/ .... 1.5 W
Lead temperature (soldering, 10 seconds) .... +260°C
Thermal resistance, junction-to-case (Θ_{JC}):
  Cases X and Y .... See MIL-STD-1835
Junction temperature (T_J) .... +175°C
Storage temperature range .... -65°C to +150°C
Temperature under bias .... -55°C to +125°C
Endurance .... 25 erase/write cycles (minimum)
Data retention .... 10 years, (minimum)

1.4 <u>Recommended operating conditions</u>.

Supply voltage (V_{CC}) .... +4.5 V dc to +5.5 V dc
Ground voltage (GND) .... 0 V dc
Input high voltage (V_{IH}) .... 2.2 V dc minimum
Input low voltage (V_{IL}) .... 0.8 V dc maximum
Operating case temperature range (T_C) .... -55°C to +125°C

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103.

2/ Lid shall be transparent to permit ultraviolet light erasure.

3/ Must withstand the added P_D due to short circuit test; (e.g., I_{OS}).

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2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535   - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883   -   Test Method Standard Microcircuits.
MIL-STD-1835   -   Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 -   List of Standard Microcircuit Drawings.
MIL-HDBK-780 -   Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 <u>Item requirements</u>. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 <u>Case outlines</u>. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 <u>Terminal connections</u>. The terminal connections shall be as specified on figure 1.

3.2.3 <u>Truth tables</u>. The truth tables shall be as specified on figure 2.

3.2.3.1 <u>Unprogrammed or erased devices</u>. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, C, or D (see 4.3), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at least 25 percent of the total number of cells to any altered item drawing.

3.2.3.2 <u>Programmed devices</u>. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 <u>Electrical performance characteristics</u>. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

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3.5 <u>Marking</u>. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 <u>Certification/compliance mark</u>. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 <u>Certificate of compliance</u>. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 <u>Certificate of conformance</u>. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 <u>Notification of change</u>. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 <u>Verification and review</u>. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 <u>Processing EPLDs</u>. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 <u>Erasure of EPLDs</u>. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4 herein.

3.10.2 <u>Programmability of EPLDs</u>. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 herein.

3.10.3 <u>Verification of erasure of programmed EPLDs</u>. When specified, devices shall be verified as either programmed to specified program or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.11 <u>Endurance</u>. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done only for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but will guarantee the number of program/erase endurance cycles listed in section 1.3 herein. The vendors procedure shall be under document control and shall be made available upon request.

4. VERIFICATION

4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

   a. Burn-in test, method 1015 of MIL-STD-883.

     (1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

     (2) T_A = +125°C, minimum.

   b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps: (Steps 1 through 4 may be performed at the wafer level. The maximum storage temperature shall not exceed 200°C for packaged devices and 300°C for unassembled devices.)

Margin test method.

(1) Program a minimum of 95% of the total number of cells, including the slowest programming cell (see 3.10.2).
(2) Bake, unbiased, for 72 hours at +140°C, or for 48 hours at +150°C, or for 8 hours at +200°C, or for unassembled devices only 2 hours at 300°C.
(3) Perform electrical test (see 4.2b) at 25° including a margin test at Vm = 5.7 V and loose timing (i.e., = 1 μs).
(4) Erase (see 3.10.1).
(5) Program a minimum of 50 percent of the total number of cells, including the slowest programming cell (see 3.10.2).
(6) Perform electrical test (see 4.2b) at 25° including a margin test at Vm = 5.7 V and loose timing (i.e., = 1 μs).
(7) Perform burn-in (see 4.2a).
(8) Perform electrical test (see 4.2b) at 25° including a margin test at Vm = 5.7 V and loose timing (i.e., = 1 μs).
(9) Repeat step 8 at t_C = +125°C and -55°C.
(10) Erase (see 3.10.1). Devices may be submitted for groups A, C, and D testing prior to erasure provided the devices have been 100 percent seal tested in accordance with method 5004 of MIL-STD-883.
(11) Verify erasure (see 3.10.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. See footnote 4/ of table II.

e. All devices selected for testing shall be programmed per 3.2.3.1 herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) The devices selected for testing shall be programmed per 3.2.3.1 herein. After completion of testing, the devices shall be erased and verified (except devices submitted for group D testing).

(2) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(3) T_A = +125°C, minimum.

(4) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE I. <u>Electrical performance characteristics.</u>

Test	Symbol	Conditions -55°C ≤ T_C ≤+125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA V_{IH} = 2.2 V, V_{IL} = 0.8 V	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8.0 mA V_{IH} = 2.2 V, V_{IL} = 0.8 V	1, 2, 3	All		0.45	V
Input high voltage <u>1</u>/ <u>2</u>/	V_{IH}		1, 2, 3	All	2.2		V
Input low voltage <u>1</u>/ <u>2</u>/	V_{IL}		1, 2, 3	All		0.8	V
Input leakage current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 5.5 V to GND	1, 2, 3	All	-10	10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, V_{OUT} = 5.5 V to GND	1, 2, 3	All	-40	40	µA
Output short circuit current <u>2</u>/ <u>3</u>/	I_{OS}	V_{CC} = 5.5 V and 4.5 V,, V_{OUT} = 0.5 V	1, 2, 3	All	-30	-90	µA
Power supply current <u>2</u>/ <u>4</u>/	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA f = f_{MAX1} V_{IN} = V_{CC} to GND	1, 2, 3	All		270	mA
Power supply current (standby) <u>4</u>/	I_{CC2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA V_{IN} = V_{CC} to GND	1, 2, 3	All		200	mA
Input capacitance <u>2</u>/	C_{IN}	V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz	4	All		10	pF
Output capacitance <u>2</u>/	C_{OUT}	V_{IN} = 0.0 V See 4.3.1c	4	All		12	pF
Functional tests		See 4.3.1d	7,8A, 8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T_C ≤+125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
			External Synchronous Switching Characteristics				
Dedicated input to combinatorial output delay 6/	t_{PD1}	See figure 4 5/	9, 10, 11	01		35	ns
				02		25	
I/O input to combinatorial output delay 7/	t_{PD2}		9, 10, 11	01		35	ns
				02		25	
Dedicated input to combinatorial output delay with expander delay 2/ 8/	t_{PD3}		9, 10, 11	01		60	ns
				02		40	
I/O input to combinatorial output delay with expander delay 2/ 9/	t_{PD4}		9, 10, 11	01		60	ns
				02		40	
Input to output enable delay 2/ 10/	t_{EA}		9, 10, 11	01		35	ns
				02		25	
Input to output disable delay 2/ 10/	t_{ER}		9, 10, 11	01		35	ns
				02		25	
Synchronous clock input to output delay	t_{CO1}		9, 10, 11	01		23	ns
				02		15	
Synchronous clock to local feedback to combinatorial output 2/ 11/	t_{CO2}		9, 10, 11	01		46	ns
				02		30	
Any input or feedback setup time to synchronous clock input	t_S		9, 10, 11	01	21		ns
				02	15		
Input hold time from synchronous clock input	t_H		9, 10, 11	All	0		ns
Synchronous clock input high time 2/	t_{WH}		9, 10, 11	01	10		ns
				02	8		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T_C ≤+125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
External Synchronous Switching Characteristics							
Synchronous clock input low time 2/	t_{WL}	See figure 4 5/	9, 10, 11	01	10		ns
				02	8		
Asynchronous clear width 12/	t_{RW}		9, 10, 11	01	33		ns
				02	28		
Asynchronous clear recovery time 12/	t_{RR}		9, 10, 11	01	35		ns
				02	25		
Asynchronous clear to registered output delay 12/	t_{RO}		9, 10, 11	01		33	ns
				02		28	
Asynchronous preset width 12/	t_{PW}		9, 10, 11	01	33		ns
				02	28		
Asynchronous preset recovery time 12/	t_{PR}		9, 10, 11	01	38		ns
				02	25		
Asynchronous preset to registered output delay 12/	t_{PO}		9, 10, 11	01		33	ns
				02		28	
Synchronous clock to local feedback input 2/ 13/	t_{CF}		9, 10, 11	01		13	ns
				02		7	
External synchronous clock period (t_{CO1} + t_S)	t_P		9, 10, 11	01	44		ns
				02	30		
External maximum frequency 1/ (t_{CO1} + t_S) 14/	f_{MAX1}		9, 10, 11	01	22.7		MHz
				02	33.3		
Maximum frequency with internal only feedback 1/ (t_{CF} + t_S) 2/ 15/	f_{MAX2}		9, 10, 11	01	29.4		MHz
				02	45.4		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
External Synchronous Switching Characteristics							
Data path maximum frequency, least of $1/(t_{WH} + t_{WL})$, $1/(t_H + t_{S1})$ or $1/(t_{CO1})$ 12/ 16/	f_{MAX3}	See figure 4 5/	9, 10, 11	01	43.4		MHz
				02	62.5		
Maximum register toggle frequency $1/(t_{WH} + t_{WL})$ 12/ 17/	f_{MAX4}		9, 10, 11	01	50.0		MHz
				02	62.5		
Output data stable time from synchronous clock input 12/ 18/	t_{OH}		9, 10, 11	All	2		ns
External Asynchronous Switching Characteristics							
Asynchronous clock input to output delay	t_{ACO1}	See figure 4 5/	9, 10, 11	01		35	ns
				02		25	
Asynchronous clock input to local feedback to combinatorial output 2/ 19/	t_{ACO2}		9, 10, 11	01		62	ns
				02		46	
Dedicated input or feedback setup time to asynchronous clock input	t_{AS}		9, 10, 11	01	15		ns
				02	12		
Input hold time from asynchronous clock input	t_{AH}		9, 10, 11	01	17.5		ns
				02	12		
Asynchronous clock input high time 2/	t_{AWH}		9, 10, 11	01	30		ns
				02	11		
Asynchronous clock input low time 2/	t_{AWL}		9, 10, 11	01	30		ns
				02	11		
Asynchronous clock to local feedback input 2/ 20/	t_{ACF}		9, 10, 11	01		27	ns
				02		21	

See footnotes at end of table.

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TABLE I. <u>Electrical performance characteristics</u> - Continued.

Test	Symbol	Conditions -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
External asynchronous clock period (t_{ACO1} + t_{AS}) or (t_{AWH} + t_{AWL}) 2/	t_{AP}	See figure 4 5/	9, 10, 11	01	50		ns
				02	37		
External maximum frequency in asynchronous mode 1/(t_{AP}) 2/ 21/	f_{MAXA1}		9, 10, 11	01	20.0		MHz
				02	27.0		
Maximum internal asynchronous frequency 1/ (t_{ACF} + t_{AS}) 2/ 22/	f_{MAXA2}		9, 10, 11	01	16.6		MHz
				02	25.0		
Data path maximum frequency in asynchronous mode 2/ 23/	f_{MAXA3}		9, 10, 11	01	16.6		MHz
				02	40.0		
Maximum asynchronous register toggle frequency 1/(t_{AWH} + t_{AWL}) 2/ 24/	f_{MAXA4}		9, 10, 11	01	16.6		MHz
				02	45.0		
Output data stable time from asynchronous clock input 12/ 25/	t_{AOH}		9, 10, 11	All	14		ns

External Synchronous Switching Characteristics

1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

2/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in Table I.

3/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed one second.

4/ Measured with device programmed with manufacturer test pattern and the test pattern shall be made available upon request.

5/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load on figure 3, circuit A.

6/ This parameter is the delay from an input signal applied to a dedicated input pin to a combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function. (see figure 4)

7/ This parameter is the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.

8/ This parameter is the delay from an input signal applied to a dedicated input pin to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.

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TABLE I. <u>Electrical performance characteristics</u> - Continued.

9/ This parameter is the delay from an input signal applied to an I/O macrocell pin to any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.

10/ Transition is measured $\pm$ 0.5 V from steady state voltage on the output from the 1.5 V level on the input with the load on figure 3, circuit B.

11/ This specification is a measure of the delay from synchronous register clock input to internal feedback of the register output signal to a combinatorial output for which the registered output signal is used as an input. This parameter assumes that no expanders are used in the logic of the combinatorial output and the register is synchronously clocked. (see figure 4)

12/ Values guaranteed by design and are not tested.

13/ This specification is a measure of the delay associated with the internal register feedback path. This delay plus the register set-up time, t_S, is the minimum internal period for an internal state machine configuration.

14/ This specification indicates the guaranteed maximum frequency at which a state machine configuration with external only feedback can operate.

15/ This specification indicates the guaranteed maximum frequency at which a state machine with internal only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO1}$. This specification assumes no expander logic is used.

16/ This frequency indicates the maximum frequency at which the device may operate in data path mode (dedicated input pin to output pin). This assumes that no expander logic is used.

17/ This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycled by a clock signal applied to either a dedicated input pin or an I/O pin.

18/ This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

19/ This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to a combinatorial output for which the registered output signal is used as an input. Assumes no expanders are used in logic of combinatorial output or the asynchronous clock input.

20/ This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clocked register. This delay plus the asynchronous register setup time, t_{AS}, is the minimum internal period for an asynchronously clocked state machine configuration. This delay assumes no expander logic in the asynchronous clock path. (see figure 4)

21/ This parameter indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed no expander logic is employed in the clock signal path or data input path.

22/ This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal only feedback can operate.   If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$. This specification assumes no expander logic is utilized.

23/ This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode. If this frequency is less than $1/(t_{ACO1})$ or $1/(t_{AS} + t_{AH})$. It also indicates the maximum frequency at which the device may operate in the asynchronously clocked data path mode. Assumes no expander logic used.

24/ This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to either a dedicated input or an I/O pin.

25/ This parameter indicates the minimum time that the previous register output data is maintained on the output pin, after an asynchronous register clock is input to an external dedicated input or I/O pin.

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Device types	ALL	
Case outlines	X	Y
Terminal number	Terminal symbol	
1	I	V_{CC}
2	I/CLK	I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I
7	V_{CC}	I
8	GND	I
9	I/O	I/CLK
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	I	I/O
14	I	V_{CC}
15	I	GND
16	I	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I
21	GND	I
22	V_{CC}	I
23	I/O	I
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I	I/O
28	I	GND

FIGURE 1. Terminal connections.

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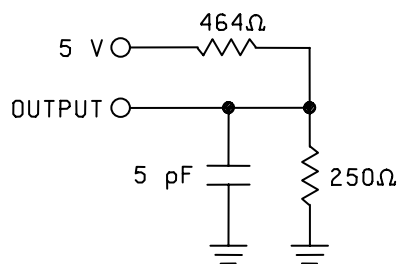|	Input pins	Output pins
CP/I	I	I/O
X	X	Z

NOTES:
1. X = Don't care
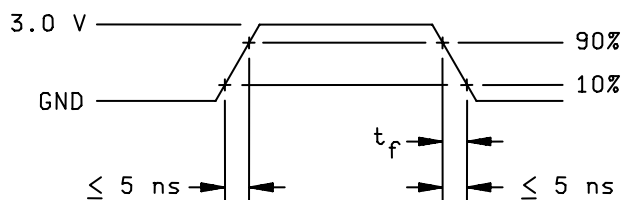2. Z = High impedance

FIGURE 2. <u>Truth table (unprogrammed).</u>
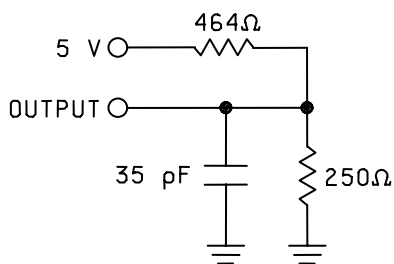
CIRCUIT A
OUTPUT LOAD

CIRCUIT B
OUTPUT LOAD FOR t_{EA} AND t_{ER}

INPUT PULSES

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times	≤ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 3. <u>Output load circuit and test conditions</u>.

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EXTERNAL COMBINATORIAL

DEDICATED INPUT/
I/O INPUT

$t_{PD1,2,3,4}$

COMBINATORIAL
OUTPUT

t_{ER}

COMBINATORIAL OR
REGISTERED OUTPUT

HIGH IMPEDANCE
3-STATE

t_{EA}

HIGH IMPEDANCE
3-STATE

VALID OUTPUT

EXTERNAL SYCHRONOUS

t_P

t_H/t_{CF}

DEDICATED INPUTS OR
REGISTERED FEEDBACK

t_S

t_{WH}

t_{WL}

SYNCHRONOUS
CLOCK

t_{CO1}

t_{OH}

t_{RW}/t_{PW}

t_{RR}/t_{PR}

ASYNCHRONOUS
CLEAR/PRESET

t_{RO}/t_{PO}

REGISTERED
OUTPUTS

t_{CO2}

COMBINATORIAL OUTPUT FROM
REGISTERED FEEDBACK (10)

FIGURE 4. Switching waveforms.

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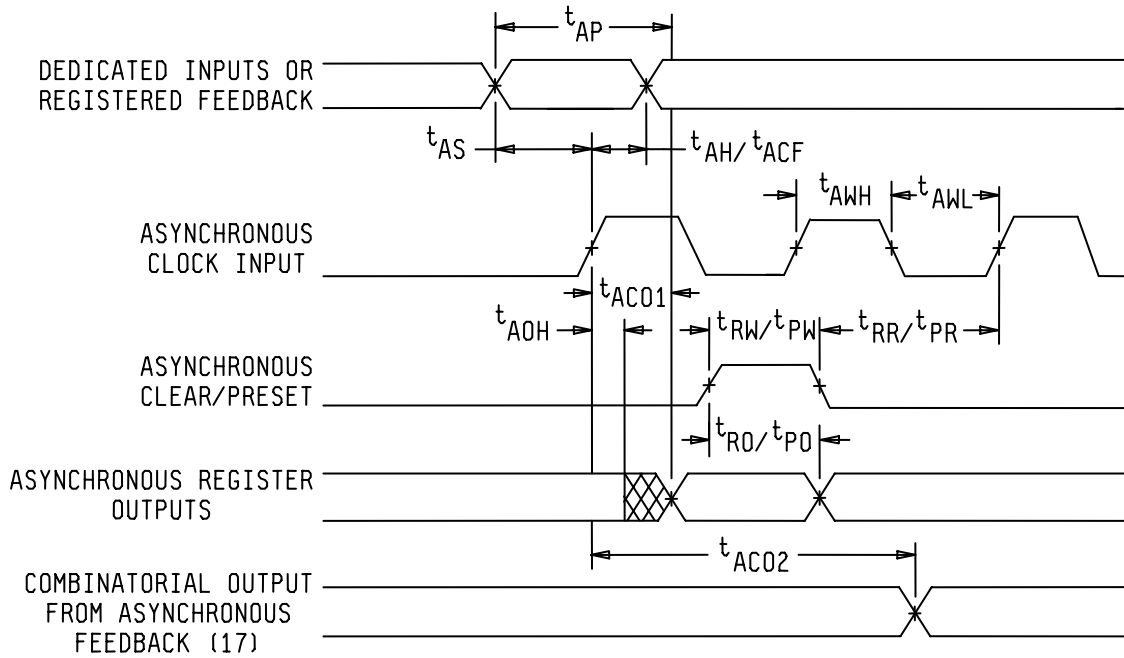APR 97

EXTERNAL ASYNCHRONOUS

FIGURE 4. Switching waveforms - Continued.

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4.4 <u>Erasing procedure</u>. The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2,537 Angstroms (Ä). The integrated dose (i.e., ultraviolet intensity times exposure time) for erasure should be minimum of 25 Ws/cm^2. The erasure time with this dosage is approximately 35 minutes using an ultraviolet lamp with a 12,000 µW/cm^2 power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7,258 Ws/cm^2 (1 week at 12,000 µW/cm^2). Exposure of the device to high intensity ultraviolet light for long periods may cause permanent damage.

4.5 <u>Programming procedures</u>. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 <u>Packaging requirements</u>. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

TABLE II. <u>Electrical test requirements</u>.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

1/ (*) indicates PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high speed testers.
3/ (**) see 4.3.1c.
4/ Subgroup 7 functional tests shall verify that no cells are programmed for
     unprogrammed devices, and that the altered item drawing pattern exists
     for programmed devices, or that the devices comply with 3.2.3.1 herein.

6. NOTES

6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 <u>Record of users</u>. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 <u>Comments</u>. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 <u>Approved sources of supply</u>. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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Approved sources of supply for SMD 5962-90611 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9061101XA	0C7V7	CY7C344-35WMB
5962-9061101YA	0C7V7	CY7C344-35HMB
5962-9061102XA	0C7V7 3/	CY7C344-25WMB EPM5032DM883B
5962-9061102YA	0C7V7 3/	CY7C344-25HMB EPM5032JM883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.