REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added 3 devices, 02 - 04. Updated format, editorial change throughout.	94-10-24	M. A. Frye
B	Add 05 device, update format, editorial changes throughout.	97-02-26	Ray Monnin
C	Boilerplate update, part of 5 year review. ksr	07-03-23	Robert M. Heber

REV																				
SHEET																				
REV	C	C	C	C	C															
SHEET	15	16	17	18	19															

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
92-03-27

REVISION LEVEL
C

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COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, UV ERASEABLE PROGRAMMABLE LOGIC ARRAY, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89468**

SHEET 1 OF 19

DSCC FORM 2233
APR 97

5962-E311-07

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89468	01	X	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Propagation Delay
01		128-Macrocell EPLD	35 ns
02		128-Macrocell EPLD	30 ns
03		128-Macrocell EPLD	25 ns
04		128-Macrocell EPLD	20 ns
05		128-Macrocell EPLD	15 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA15-PN	68	pin grid array package 2/
Y	GQCC1-J68	68	J-leaded chip carrier 2/
Z	See figure 1	68	quad flat package 2/

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage to ground potential	2.0 V dc to +7.0 V dc
DC Input voltage	2.0 V dc to +7.0 V dc
Maximum power dissipation 3/	2.5 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case outlines X and Y	See MII-STD-1835
Case outline Z	10°C/W 4/
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Temperature under bias	-55°C to +125°C
Endurance	25 erase/write cycles (minimum)
Data retention	10 years minimum

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.2 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1 Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103.
2/ Lid shall be transparent to permit ultraviolet light erasure.
3/ Must withstand the added P_D due to short circuit test (e.g., I_{SC}).
4/ When the thermal resistance for this case is specified in MIL-STD-1835 that value shall supersede the value indicated herein.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with figure 1 and 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 3. When required in groups A, B, or C (see 4.3), the devices shall be programmed by the manufacturer prior to test with a minimum of 50 percent of the total number of gates programmed or to any altered item drawing pattern which includes at least 25 percent of the total number of gates programmed.

3.2.3.2 Programmed devices. The truth tables for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5V \le V_{CC} \le 5.5V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, V_{IH} = 2.2 V, I_{OH} = -4.0 mA, V_{IL} = 0.8 V	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, V_{IH} = 2.2 V, I_{OL} = 8.0 mA, V_{IL} = 0.8 V	1, 2, 3	All		0.45	V
Input high voltage 1/ 2/	V_{IH}		1, 2, 3	All	2.2		V
Input low voltage 1/ 2/	V_{IL}		1, 2, 3	All		0.8	V
Input leakage current	I_{IX}	V_{CC} = 5.5 V, V_{IN} = 5.5 V and GND	1, 2, 3	All	-10	10	uA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, V_{OUT} = 5.5 V and GND	1, 2, 3	All	-40	40	uA
Output short circuit current 2/ 3/	I_{SC}	V_{CC} = 5.5 V, V_{OUT} = 0.5 V	1, 2, 3	All	-30	-90	mA
Power supply current 2/ 4/	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = V_{CC} to GND, f = $1/t_{PD1}$	1, 2, 3	All		700	mA
Power supply current 4/ (Standby)	I_{CC2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = GND	1, 2, 3	All		300	mA
Input capacitance 2/	C_{IN}	V_{CC} = 5.0 V, V_{IN} = 0.0 V, T_A = 25°C, f = 1MHz (see 4.3.1c)	4	All		10	pF
Output capacitance 2/	C_{OUT}	V_{CC} = 5.0 V, V_{OUT} = 0.0 V, T_A = 25°C, f = 1MHz (see 4.3.1c)	4	All		20	pF
Functional tests		See 4.3.1d	7,8A,8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5V \le V_{CC} \le 5.5V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
External Synchronous Switching Characteristics							
Dedicated input to combinatorial output delay 6/	t_{PD1}	See figure 5 5/	9, 10, 11	01		35	ns
				02		30	
				03		25	
				04		20	
				05		15	
I/O input to combinatorial output delay 7/	t_{PD2}		9, 10, 11	01		55	ns
				02		46	
				03		40	
				04		33	
				05		25	
Dedicated input to combinatorial output delay with expander delay 2/ 8/	t_{PD3}		9, 10, 11	01		55	ns
				02		44	
				03		37	
				04		30	
				05		23	
I/O input to combinatorial output delay with expander delay 2/ 9/	t_{PD4}		9, 10, 11	01		75	ns
				02		60	
				03		51	
				04		43	
				05		33	
Input to output enable delay 2/ 6/	t_{EA}		9, 10, 11	01		35	ns
				02		30	
				03		25	
				04		20	
				05		15	
Input to output disable delay 2/ 6/ 10/	t_{ER}		9, 10, 11	01		35	ns
				02		30	
				03		25	
				04		20	
				05		15	
Synchronous clock input to output delay	t_{CO1}		9, 10, 11	01		20	ns
				02		16	
				03		14	
				04		8	
				05		7	
2/ 11/ Synchronous clock to local feedback to combinatorial output	t_{CO2}		9, 10, 11	01		42	ns
				02		35	
				03		30	
				04		22	
				05		17	
6/ 13/ Dedicated input or feedback setup time to synchronous clock input	t_{S1}		9, 10, 11	01	25		ns
				02	20		
				03	15		
				04	13		
				05	10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5V \le V_{CC} \le 5.5V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
I/O input setup time to synchronous clock input 2/ 6/	t_{S2}	See figure 5 5/	9, 10, 11	01	45		ns
				02	36		
				03	29		
				04	26		
				05	20		
Input hold time from 6/ synchronous clock input	t_H		9, 10, 11	All	0		ns
Synchronous clock input high time 2/	t_{WH}		9, 10, 11	01	12.5		ns
				02	10		
				03	8		
				04	7		
				05	5		
Synchronous clock input low time 2/	t_{WL}		9, 10, 11	01	12.5		ns
				02	10		
				03	8		
				04	7		
				05	5		
Asynchronous clear width 2/ 6/ 12/	t_{RW}		9, 10, 11	01	35		ns
				02	30		
				03	25		
				04	22		
				05	15		
Asynchronous clear recovery time 2/ 6/ 12/	t_{RR}		9, 10, 11	01	35		ns
				02	30		
				03	25		
				04	22		
				05	15		
Asynchronous clear to registered output delay 6/	t_{RO}		9, 10, 11	01		35	ns
				02		30	
				03		25	
				04		20	
				05		15	
Asynchronous preset width 2/ 6/ 12/	t_{PW}		9, 10, 11	01	35		ns
				02	30		
				03	25		
				04	22		
				05	15		
Asynchronous preset recovery time 2/ 6/ 12/	t_{PR}		9, 10, 11	01	35		ns
				02	30		
				03	25		
				04	22		
				05	15		
Asynchronous preset to registered output delay 6/	t_{PO}		9, 10, 11	01		35	ns
				02		30	
				03		25	
				04		20	
				05		15	
Synchronous clock to local feedback 2/ 14/ input	t_{CF}		9, 10, 11	01		6	ns
				02-05		3	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5V \le V_{CC} \le 5.5V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
External synchronous clock period ($t_{CO1} + t_S$) 2/	t_P	See figure 5 5/	9, 10, 11	01	45		ns
				02	36		
				03	29		
				04	21		
				05	12		
External feedback maximum frequency $1/(t_{CO1} + t_{S1})$ 2/ 15/	f_{MAX1}		9, 10, 11	01	22.2		
				02	27.7		
				03	34.5		
				04	47.6		
				05	58.8		
2/ 16/ Internal local feedback maximum frequency, lesser of $1/(t_{S1} + t_{CF})$ or $1/(t_{CO1})$	f_{MAX2}		9, 10, 11	01	32.2		MHz
				02	43.4		
				03	55.5		
				04	62.5		
				05	76.9		
Data path maximum frequency, least of $1/(t_{WL} + t_{WH})$, $1/(t_{S1} + t_H)$ or $1/(t_{CO1})$ 12/ 17/	f_{MAX3}		9, 10, 11	01	40.0		
				02	50.0		
				03	62.5		
				04	71.4		
				05	100		
Maximum register toggle frequency $1/(t_{WH} + t_{WL})$ 12/ 18/	f_{MAX4}		9, 10, 11	01	40.0		
				02	50.0		
				03	62.5		
				04	71.4		
				05	100		
Output data stable time from synchronous clock input 12/ 19/	t_{OH}		9, 10, 11	All	3		ns
External Asynchronous Switching Characteristics							
6/ Asynchronous clock input to output delay	t_{ACO1}	See figure 5 5/	9, 10, 11	01		35	ns
				02		30	
				03		25	
				04		20	
				05		15	
2/ 20/ Asynchronous clock input to local feedback to combinatorial output	t_{ACO2}		9, 10, 11	01		55	ns
				02		49	
				03		41	
				04		32	
				05		25	
6/ Dedicated input or feedback setup time to asynchronous clock input	t_{AS1}		9, 10, 11	01	8		ns
				02	6		
				03-05	5		
12/ 6/ I/O input setup time to asynchronous clock input	t_{AS2}		9, 10, 11	01	28		ns
				02	22		
				03	19		
				04	18		
				05	14.5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C≤T_C≤+125°C 4.5V ≤ V_{CC} ≤ 5.5V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Input hold time from asynchronous clock input 6/	t_{AH}	See figure 5 5/	9, 10, 11	01	10		ns
				02	8		
				03	6		
				04	6		
				05	5		
Asynchronous clock input high time 2/ 6/	t_{AWH}		9, 10, 11	01	16		ns
				02	14		
				03	11		
				04	7		
				05	9		
Asynchronous clock input low time 2/ 6/	t_{AWL}		9, 10, 11	01	16		ns
				02	14		
				03	11		
				04,05	7		
Asynchronous clock to local feedback input 2/ 21/	t_{ACF}		9, 10, 11	01		22	ns
				02		18	
				03		15	
				04		13	
				05		11	
External asynchronous clock period (t_{ACO1} + t_{AS1}) or (t_{AWH} + t_{AWL}) 2/	t_{AP}		9, 10, 11	01	43		ns
				02	28		
				03	22		
				04	14		
				05	16		
External feedback maximum frequency in asynchronous mode 1/(t_{AP}) 2/ 22/	f_{MAXA1}		9, 10, 11	01	23.2		MHz
				02	27.7		
				03	33.3		
				04	40		
				05	50		
Maximum internal asynchronous frequency 1/(t_{AS2} + t_{ACF}) or 1/t_{ACO1} 2/ 25/	f_{MAXA2}		9, 10, 11	01	20		MHz
				02	25		
				03	29.4		
				04	32.3		
				05	62.5		
Data path maximum frequency in asynchronous mode 1/(t_{AWH} + t_{AWL}) or 1/(t_{AS1} + t_{AH}) or 1/t_{ACO1} 12/ 24/	f_{MAXA3}		9, 10, 11	01	28.5		MHz
				02	33.3		
				03	40		
				04	50		
				05	66.6		
Maximum asynchronous register toggle frequency 12/ 23/ 1/(t_{AWH} + t_{AWL})	f_{MAXA4}		9, 10, 11	01	31.2		MHz
				02	35.7		
				03	45.5		
				04	71.4		
				05	62.5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5V \le V_{CC} \le 5.5V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
12/ 26/ Output data stable time from asynchronous clock input	t_{AOH}	See figure 5 5/	9, 10, 11	All	12		ns

1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

2/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

3/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed one second.

4/ Specified with device programmed as a 16-bit counter in each LAB. Tested with manufacturer test pattern and shall be made available upon request.

5/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load on figure 4, circuit A.

6/ This parameter is the delay from an input signal applied to a dedicated input pin to a combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.

When this note is applied to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic.

If an input signal is applied to an I/O pin an additional delay equal to t_{PIA} should be added to the comparable delay for a dedicated input. If expanders are used add the maximum expander delay t_{EXP} to the overall delay for the comparable delay without expanders.

7/ This parameter is the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.

8/ This parameter is the delay from an input signal applied to a dedicated input pin to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.

9/ This parameter is the delay from an input signal applied to an I/O macrocell pin to any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.

10/ Transition is measured $\pm$ 0.5 V from steady state voltage on the output from the 1.5 V level on the input with the load on figure 4, circuit B.

11/ This specification is the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes that no expanders are used, register is synchronously clocked and all feedback is within the same LAB.

12/ Values guaranteed by design and are not tested.

13/ If data is applied to an I/O input for capture by a macrocell register, the I/O pin input set-up time minimums should be observed. These parameters are t_{S2} for synchronous operation and t_{AS2} for asynchronous operation.

14/ This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t_{S1}, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB.

15/ This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs. All feedback is assumed to be local originating within the same LAB.

TABLE I. Electrical performance characteristics - Continued.

16/ This specification indicates the guaranteed maximum frequency at which a state machine with internal only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO1}$.

17/ This frequency indicates the maximum frequency at which the device may operate in data path mode (dedicated input pin to output pin). This assumes data input signals are applied to dedicated input pins and no expander logic is used. If any of the data inputs are I/O pins, t_{S2} is the appropriate t_S for calculation.

18/ This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycled by a clock signal applied to the dedicated clock input pin.

19/ This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

20/ This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in logic of combinatorial output or the asynchronous clock input. The clock signal is applied to the dedicated clock input pin and all feedback is within a single LAB.

21/ This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register setup time, t_{AS1}, is the minimum internal period for an internal asynchronously clocked state machine configuration. This delay is for feedback within the same LAB, assumes no expander logic in the clock path and assumes that the clock input signal is applied to a dedicated input pin.

22/ This parameter indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs and that no expander logic is employed in the clock signal path or data path.

23/ This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.

24/ This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the least of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS1} + t_{AH})$ or $1/(t_{ACO1})$. It assumes data and clock input signals are applied to dedicated input pins and no expander logic is used.

25/ This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal only feedback can operate. This parameter is determined by the lesser of $(1/(t_{ACF} + t_{AS}))$ or $(1/(t_{AWH} + t_{AWL}))$. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$.
This specification assumes no expander logic is utilized, all data inputs and clock inputs are applied to dedicated inputs, and all state feedback is within a single LAB.

26/ This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input applied to an external dedicated input pin.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

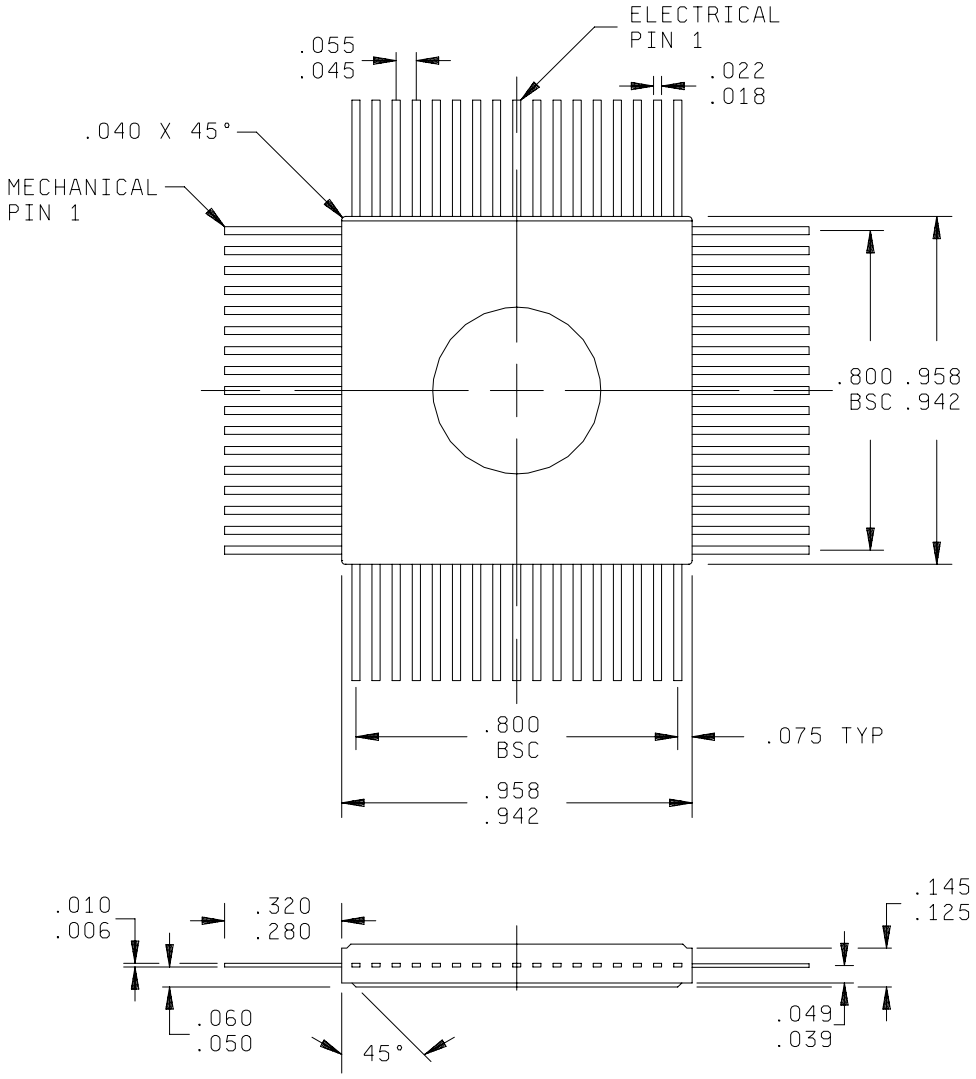
3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

Case Z



Inches	mm	Inches	mm	Inches	mm
.006	0.15	.049	1.24	.280	7.11
.010	0.25	.050	1.27	.320	8.13
.018	0.46	.055	1.40	.800	20.32
.022	0.56	.060	1.52	.942	23.93
.039	0.99	.075	1.91	.958	24.33
.040	1.02	.125	3.18		
.045	1.14	.145	3.68		

NOTES:

1. Dimension are in inches.
2. Metric equivalents are given for general information only.

FIGURE 1. Case outlines.

Device types	All	Device types	All
Case outlines	Y,Z	Case outlines	Y,Z
Terminal number 1/	Terminal symbol	Terminal number 1/	Terminal symbol
1	I/CLK	35	I
2	I	36	I
3	VCC	37	VCC
4	I/O	38	I/O
5	I/O	39	I/O
6	I/O	40	I/O
7	I/O	41	I/O
8	I/O	42	I/O
9	I/O	43	I/O
10	I/O	44	I/O
11	I/O	45	I/O
12	I/O	46	I/O
13	I/O	47	I/O
14	I/O	48	I/O
15	I/O	49	I/O
16	GND	50	GND
17	I/O	51	I/O
18	I/O	52	I/O
19	I/O	53	I/O
20	VCC	54	VCC
21	I/O	55	I/O
22	I/O	56	I/O
23	I/O	57	I/O
24	I/O	58	I/O
25	I/O	59	I/O
26	I/O	60	I/O
27	I/O	61	I/O
28	I/O	62	I/O
29	I/O	63	I/O
30	I/O	64	I/O
31	I/O	65	I/O
32	I	66	I
33	GND	67	GND
34	I	68	I

1/ Terminal numbers are referenced to the electrical pin one.

FIGURE 2. Terminal connections.

Case outline X

1	2	3	4	5	6	7	8	9	10	11	
	I/O	I/O	I	I	I	I/O	I/O	I/O	I/O		L
I/O	I/O	I/O	I/O	GND	I	V_{CC}	I/O	I/O	I/O	I/O	K
I/O	I/O								I/O	I/O	J
I/O	I/O								I/O	I/O	H
I/O	VCC								GND	I/O	G
I/O	I/O								I/O	I/O	F
I/O	GND								VCC	I/O	E
I/O	I/O								I/O	I/O	D
I/O	I/O	1/							I/O	I/O	C
I/O	I/O	I/O	I/O	VCC	I / CLK	GND	I/O	I/O	I/O	I/O	B
	I/O	I/O	I/O	I/O	I	I	I	I/O	I/O		A
1	2	3	4	5	6	7	8	9	10	11	

BOTTOM VIEW

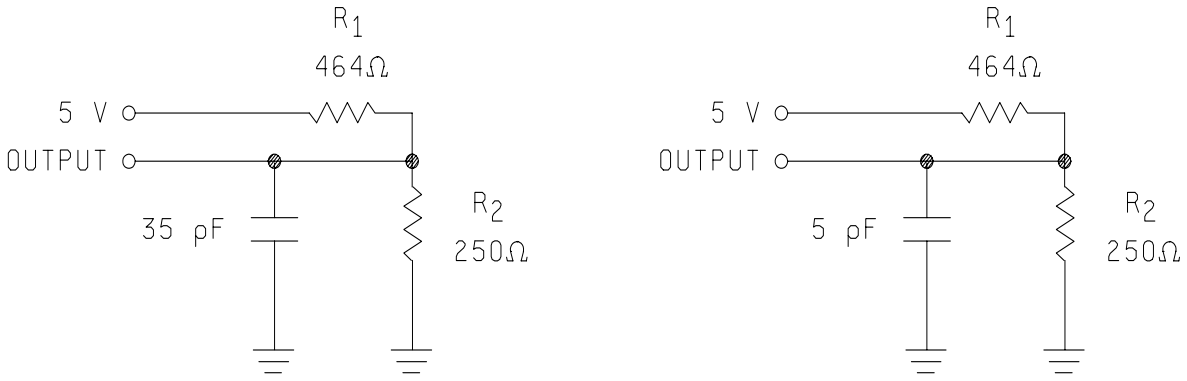
1/ Reference mark

FIGURE 2. Terminal connections - Continued.

Truth table		
Input pins		Output pins
CP/I	I	I/O
X	X	Z

NOTES:
1. X = Don't care
2. Z = High impedance

FIGURE 3. Truth table (unprogrammed).



Circuit A
Output load

Circuit B
Output load for t_{ER}

Input pulses
AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall levels	≤ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

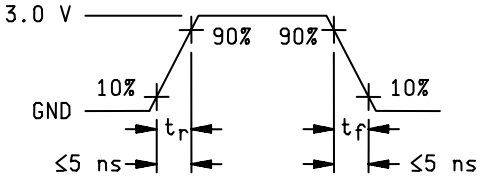
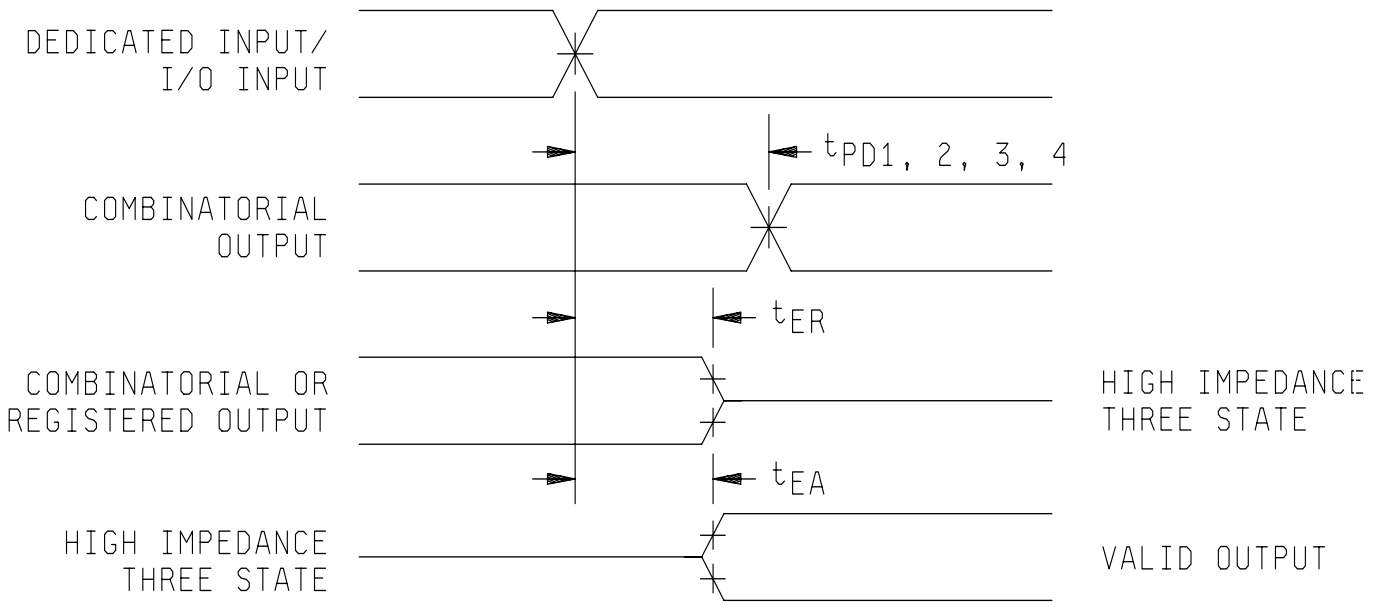


FIGURE 4. Output load circuit and test conditions.

External combinatorial



External synchronous

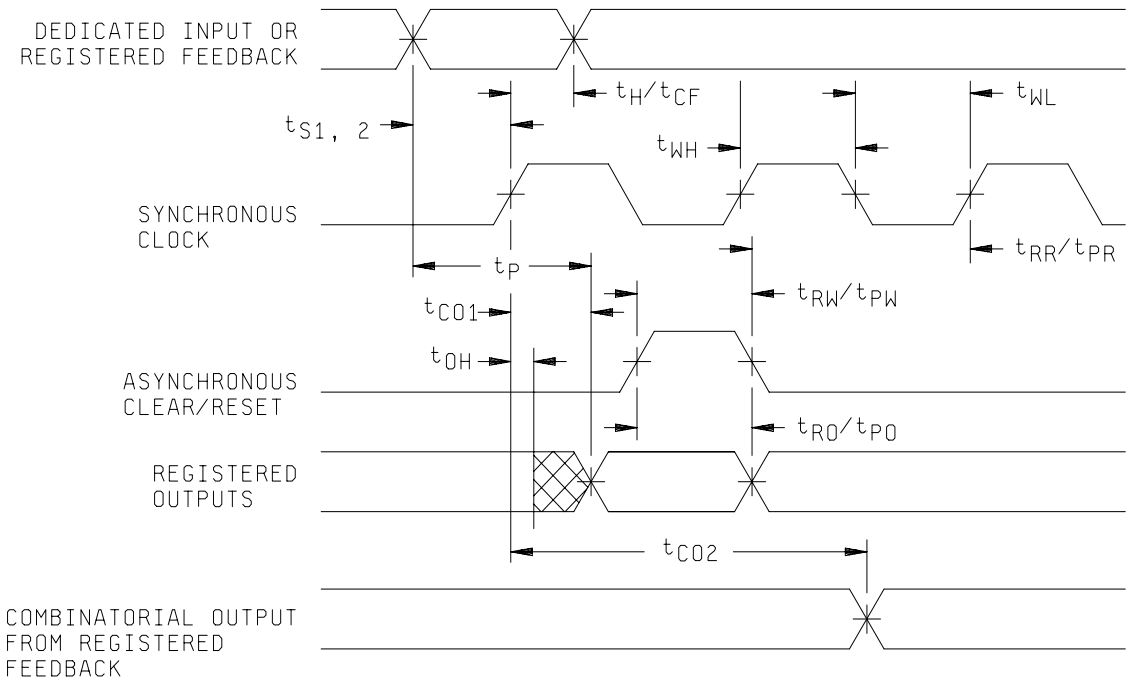


FIGURE 5. Switching waveforms.

External asynchronous

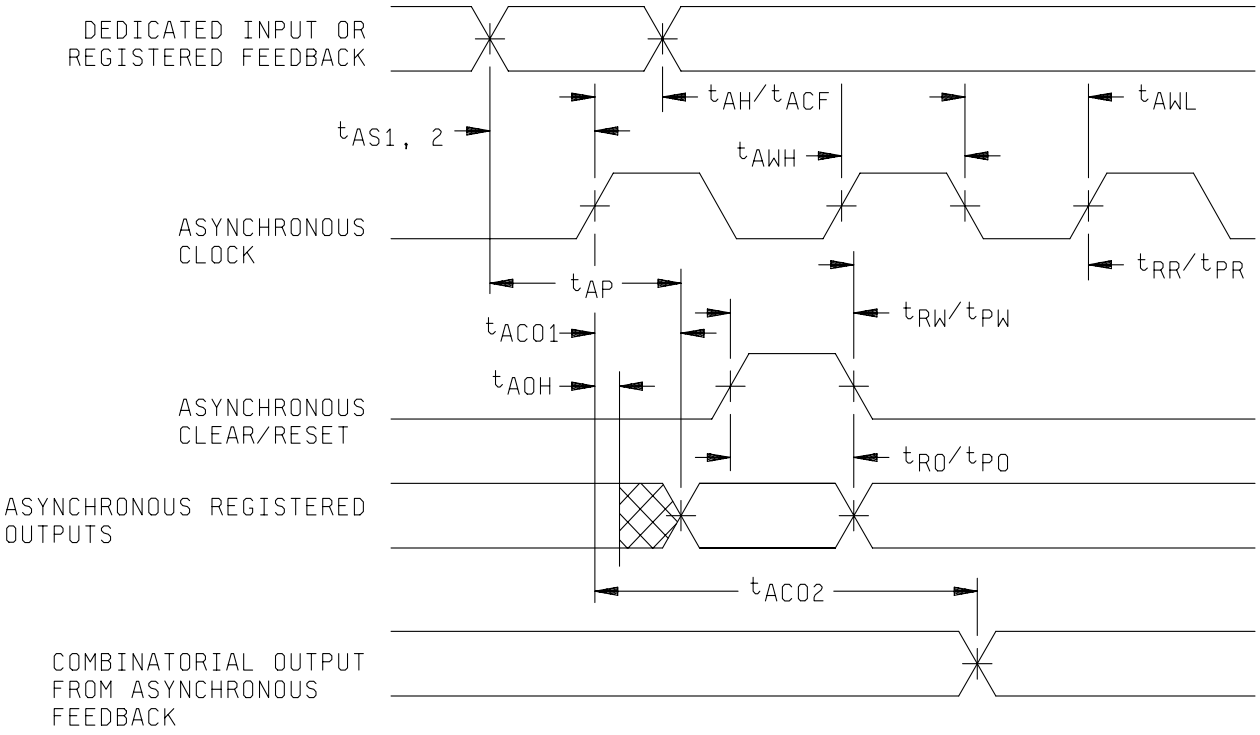


FIGURE 5. Switching waveforms - Continued.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing EPLD's. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EPLD's. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.10.2 Programmability of EPLD's. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.10.3 Verification of erasure or programmed EPLD's. When specified, devices shall be verified as either programmed (see 4.5 herein) to the specified pattern or erased (see 4.4 herein). As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.11 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitor. This reprogrammability test shall be done only for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but will guarantee the number of program/erase endurance cycles listed in section 1.3 herein. The vendor's procedure shall be under document control and shall be made available upon request.

3.12 Data retention. A data retention stress test shall be completed as part of the vendor's reliability process. This test shall be done initially and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but will guarantee the number of years listed in section 1.3 herein. The vendors procedure shall be under document control and shall be made available upon request. Data retention capability shall be guaranteed over the full military temperature range.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Prior to burn-in, the devices shall be programmed (see 4.7 herein) with a checkerboard pattern or equivalent (manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern). The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be included in the Percent Defective Allowable (PDA) calculation and shall be removed from the lot. The manufacturer as an option may use built-in test circuitry by testing the entire lot to verify programmability and AC performance without programming the user array.

b. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

c. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures and all input and output terminals tested.

d. See 4/ of table II.

e. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. Procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.

f. Devices shall be tested for programmability and ac performance compliance to the requirements of Group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:

(1) Testing all devices submitted for test using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing per the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, all samples submitted for testing shall be programmed in accordance with 3.2.3.1 or 3.2.3.2 as applicable. After completion of all testing, the devices shall be erased and verified except devices submitted to groups C and D testing.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for programmed devices	1*, 2, 3, 7*, 8A, 8B, 9
Group A test requirements (method 5005)	1,2,3,4**,7, 9, 10,11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

1/ * indicates PDA applies to subgroups 1 and 7.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ ** see 4.3.1c.

4/ Subgroups 7, 8A, and 8B functional tests shall also verify that no cells are programmed for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) The devices selected for testing shall be programmed per 3.2.3.1 herein. After completion of testing, the devices shall be erased and verified (except devices submitted for group D testing).

(2) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(3) T_A = +125°C, minimum.

(4) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of twenty-five Ws/cm^2. The erasure time with this dosage is approximately 35 minutes using an ultraviolet lamp with a 12000 uW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12000 uW/cm^2). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-03-23

Approved sources of supply for SMD 5962-89468 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8946801XC	0C7V7 3/ 3/	CY7C342B-35RMB CY7C342-35RMB EPM5128GM883B
5962-8946801YA	0C7V7 3/ 3/	CY7C342B-35HMB CY7C342-35HMB EPM5128GM883B
5962-8946801ZA	3/ 3/	CY7C342B-35TMB CY7C342-35TMB
5962-8946802XC	0C7V7 3/	CY7C342B-30RMB CY7C342-30RMB
5962-8946802YA	0C7V7 3/	CY7C342B-30HMB CY7C342-30HMB
5962-8946802ZA	3/ 3/	CY7C342B-30TMB CY7C342-30TMB
5962-8946803XC	0C7V7	CY7C342B-25RMB
5962-8946803YA	0C7V7	CY7C342B-25HMB
5962-8946803ZA	3/	CY7C342B-25TMB
5962-8946804XC	0C7V7	CY7C342B-20RMB
5962-8946804YA	0C7V7	CY7C342B-20HMB
5962-8946804ZA	3/	CY7C342B-20TMB
5962-8946805XC	0C7V7	CY7C342B-15RMB
5962-8946805YA	0C7V7	CY7C342B-15HMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.