REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to current requirements. Editorial changes throughout. - gap	02-02-21	Raymond Monnin
B	Add QP Semiconductor as an approved source of supply and editorial changes throughout. - tcr	06-06-22	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED

REV																			
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REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

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DRAWING APPROVAL DATE
92-08-12

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, ONE TIME PROGRAMMABLE, ASYNCHRONOUS PROGRAMMABLE LOGIC DEVICE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-90555**

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-90555	01	K	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	t_{PD}
01	C20RA10	Asynchronous PLD	35 ns
02	C20RA10	Asynchronous PLD	25 ns
03	C20RA10	Asynchronous PLD	20 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or CDFP3-F24	24	Flat pack
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3, X	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage to ground potential	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs in high Z state	-0.5 V dc to +7.0 V dc
DC input voltage	-3.0 V dc to +7.0 V dc
Maximum power dissipation (P_D) 2/	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Temperature under bias	-55°C to +125°C
Output current into outputs (low)	-16 mA

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.0 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, C, or D (see 4.3), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at least 25 percent of the total number of cells to any altered item drawing.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

3.10.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.10.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -2.0 mA, $V_{IN} = V_{IH}, V_{IL}$	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8.0 mA, $V_{IN} = V_{IH}, V_{IL}$	1, 2, 3	All		0.5	V
Input high voltage 1/	V_{IH}		1, 2, 3	All	2.0		V
Input low voltage 1/	V_{IL}		1, 2, 3	All		0.8	V
Input leakage current	I_{IX}	V_{IN} = 5.5 V to GND	1, 2, 3	All	-10	10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, V_{OUT} = 5.5 V and GND	1, 2, 3	All	-40	40	µA
Output short circuit current 2/ 3/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = 0.5 V	1, 2, 3	All	-30	-90	mA
Standby power supply current	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = GND	1, 2, 3	All		80	mA
Power supply current at frequency 3/	I_{CC2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = 0 to 3 V, f = f_{MAX}	1, 2, 3	All		85	mA
Input capacitance 3/	C_{IN}	V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz (see 4.3.1c)	4	All		10	pF
Output capacitance 3/	C_{OUT}		4	All		10	pF
Functional tests		see 4.3.1d	7, 8A, 8B	All	L	H	V
Input or feedback to nonregistered output 4/	t_{PD}		9, 10, 11	01		35	ns
				02		25	
				03		20	
Input to output enable 5/	t_{EA}		9, 10, 11	01		35	ns
				02		30	
				03		20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input to output disable 3/ 5/	t_{ER}		9, 10, 11	01		35	ns
				02		30	
				03		20	
$\overline{OE}$ to output enable 5/	t_{PZX}		9, 10, 11	01		25	ns
				02		20	
				03		15	
$\overline{OE}$ to output disable 3/ 5/	t_{PXZ}		9, 10, 11	01		25	ns
				02		20	
				03		15	
Clock to output 4/	t_{CO}		9, 10, 11	01		35	ns
				02		25	
				03		20	
Input or feedback setup time 4/	t_{SU}		9, 10, 11	01	20		ns
				02	15		
				03	10		
Hold time 4/	t_H		9, 10, 11	01, 02	5		ns
				03	3		
Clock period ($t_{SU} + t_{CO}$) 4/	t_P		9, 10, 11	01	55		ns
				02	40		
				03	30		
Clock width high 4/	t_{WH}		9, 10, 11	01	25		ns
				02	18		
				03	12		
Clock width low 4/	t_{WL}		9, 10, 11	01	25		ns
				02	18		
				03	12		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Maximum frequency (1/(t_P)) 3/ 4/	f_{MAX}		9, 10, 11	01	18.1		MHz
				02	25.0		
				03	33.3		
Input to asynchronous set of registered output 4/	t_S		9, 10, 11	01		40	ns
				02		25	
				03		20	
Input to asynchronous reset of registered output 4/	t_R		9, 10, 11	01		40	ns
				02		25	
				03		20	
Asynchronous set/reset recovery time 4/	t_{AR}		9, 10, 11	01	20		ns
				02	15		
				03	12		
Preload pulse width 4/	t_{WP}		9, 10, 11	All	15		ns
Preload setup time 3/ 4/	t_{SUP}		9, 10, 11	All	15		ns
Preload hold time 3/ 4/	t_{HP}		9, 10, 11	All	15		ns

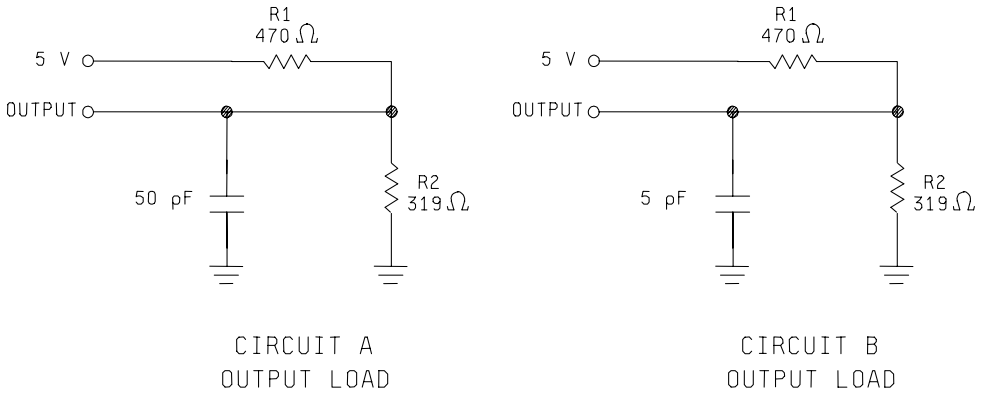
1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 1 second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.
3/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
4/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load on figure 3, circuit A. See figure 4 for waveforms.
5/ Measured using the test load on figure 3, circuit B. See figure 4 for waveforms.

Device types	01 through 03		
Case outlines	K, L	3	X
Terminal number	Terminal symbol		
1	$\overline{PL}$	$\overline{PL}$	$\overline{PL}$
2	I_0	I_0	I_0
3	I_1	I_1	I_1
4	I_2	NC	I_2
5	I_3	I_2	NC
6	I_4	I_3	I_3
7	I_5	I_4	I_4
8	I_6	I_5	NC
9	I_7	I_6	I_5
10	I_8	I_7	I_6
11	I_9	NC	NC
12	GND	I_8	I_7
13	$\overline{OE}$	I_9	I_8
14	I/O_9	GND	I_9
15	I/O_8	$\overline{OE}$	GND
16	I/O_7	I/O_9	$\overline{OE}$
17	I/O_6	I/O_8	I/O_9
18	I/O_5	NC	I/O_8
19	I/O_4	I/O_7	NC
20	I/O_3	I/O_6	I/O_7
21	I/O_2	I/O_5	I/O_6
22	I/O_1	I/O_4	I/O_5
23	I/O_0	I/O_3	I/O_4
24	V_{CC}	I/O_2	I/O_3
25	---	NC	I/O_2
26	---	I/O_1	I/O_1
27	---	I/O_0	I/O_0
28	---	V_{CC}	V_{CC}

Truth table			
Input pins			Output pins
$\overline{OE}$	$\overline{PL}$	I	O
X	X	X	Z

NOTES:
1. Z = High impedance
2. X = Don't care

FIGURE 2. Truth table.



* Including scope and jig (minimum values)

AC test conditions	
Input pulse levels	GND to 3.0 V
Input rise and fall times	≤ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

Input pulses

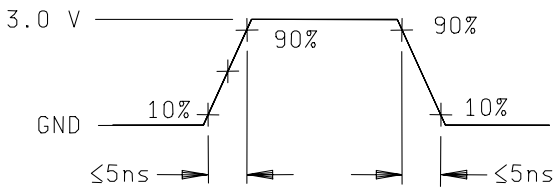


FIGURE 3. Output load circuits and test conditions.

Output control switching waveform

PARAMETER	V_X	OUTPUT WAVEFORM - MEASUREMENT LEVEL
$t_{PXZ(-)}$ $t_{ER(-)}$	1.5 V	V_{OH}, 0.5 V, V_X
$t_{PXZ(+)}$ $t_{ER(+)}$	2.6 V	V_{OL}, 0.5 V, V_X
$t_{PZX(+)}$ $t_{EA(+)}$	2.02 V	V_X, 0.5 V, V_{OH}
$t_{PZX(-)}$ $t_{EA(-)}$	2.02 V	V_X, 0.5 V, V_{OL}

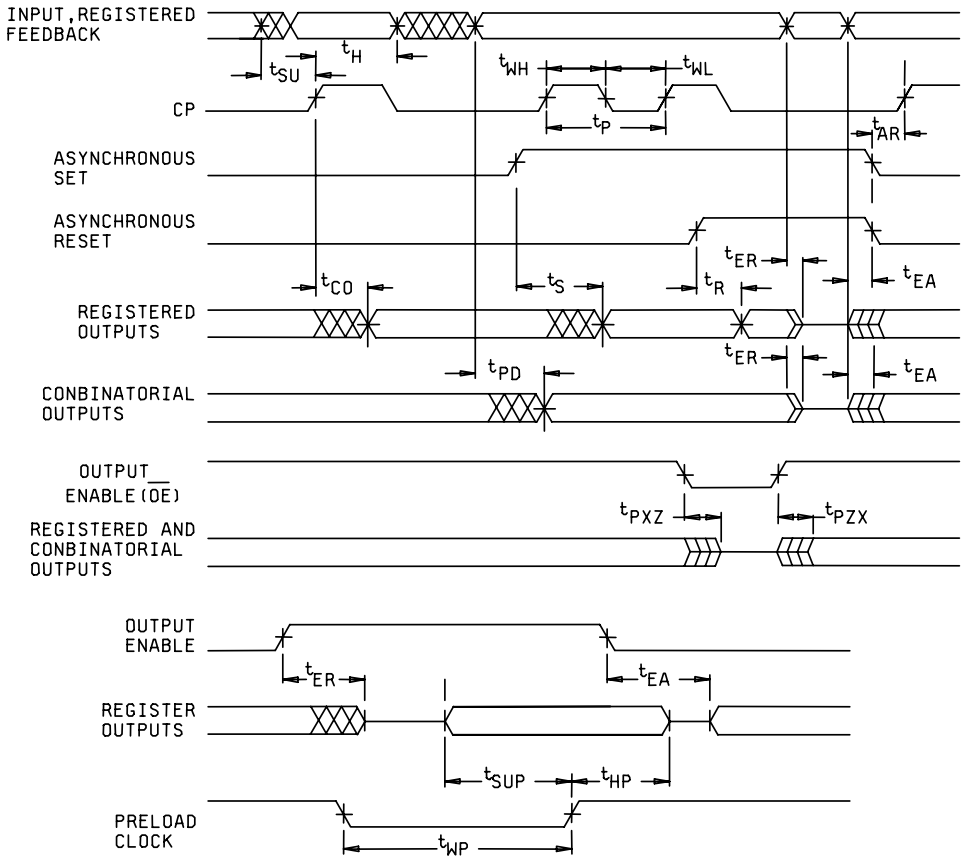


FIGURE 4. Switching waveforms.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-90555
		REVISION LEVEL B	SHEET 10

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for unprogrammed devices	1*, 2, 3, 7*, 8A, 8B
Final electrical test parameters (method 5004) for programmed devices	1*, 2, 3, 7*, 8A, 8B, 9
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

1/ * indicates PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ ** see 4.3.1c.
4/ Subgroups 7 and 8 functional tests shall also verify that no cells are programmed for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 shall include verification of the truth table.

e. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11.

(1) A sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.3.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable.

(2) Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.5 Electrostatic discharge sensitivity (ESDS) inspection. ESDS testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-06-22

Approved sources of supply for SMD 5962-90555 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9055501KA	0C7V7	PLDC20RA10-35KMB
5962-9055501LA	0C7V7	PLDC20RA10-35DMB
5962-90555013A	0C7V7	PLDC20RA10-35LMB
5962-9055501XA	3/	CG1690BA
5962-9055502KA	0C7V7	PLDC20RA10-25KMB
5962-9055502LA	0C7V7	PLDC20RA10-25DMB
5962-90555023A	0C7V7	PLDC20RA10-25LMB
5962-9055502XA	3/	CG1690AA
5962-9055503KA	0C7V7	PLDC20RA10-20KMB
5962-9055503LA	0C7V7	PLDC20RA10-20DMB
5962-90555033A	0C7V7	PLDC20RA10-20LMB
5962-9055503XA	3/	CG1690CA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051 - 0812

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.