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REALVIEW® VERSATILE FAMILY

DATA SHEET

The ARM® RealView® family of feature rich development boards provides an excellent environment for prototyping system-on-chip designs. Through a range of plug-in options, hardware and software applications can be developed and debugged.

The high performance Versatile family enhances the end-user experience for benchmarking and application development. It simplifies hardware and software development, which shortens time to market.

This datasheet describes a new RealView product: the Core Tile for ARM1156T2F-S or CT1156T2F-S. This board is based on the first implementation of the ARM1156T2F-S processor in silicon.

Together, this Core Tile and the RealView Emulation Baseboard provide an ideal Thumb-2 software development platform. Owing to the similarities between the Cortex-R4 and ARM1156T2F-S processors, the CT1156T2F-S is also the best solution available at the moment for Cortex-R4 software development. By adding RealView Logic Tiles to this system, it becomes a fast platform for AMBA AXI peripheral prototyping on FPGA.

Core Tile for ARM1156T2F-S

The CT1156T2F-S is a compact development board based on the ARM1156T2F-S test chip, the first silicon to implement the Thumb-2 instruction set. This device is based around a hardened ARM1156T2F-S CPU running at up to 360MHz.

The ARM1156T2F-S test chip has a 64-bit AXI master interface, which is routed to the Core Tile's stacking connectors. The Core Tile has been designed to work on top of a baseboard that provides power and implements the memory system and peripherals.

The Core Tile includes a MICTOR connector to trace software execution with an external trace port analyzer such as RealView Trace. The Core Tile also provides ADC and DAC circuits to modify the core voltage and measure the current on the test chip's power rails. This feature allows the measurement of power consumption with different software loads.

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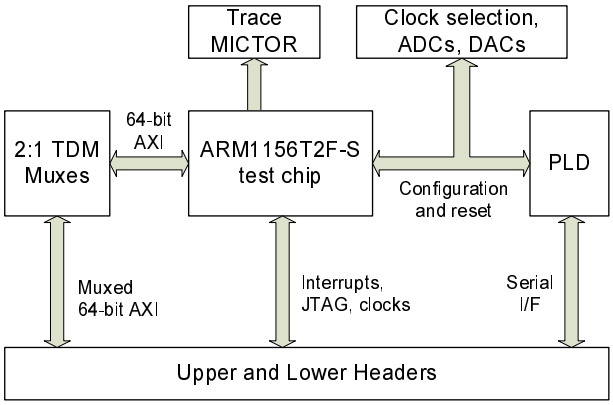
Specification

CT1156T2F-S Features

- ARM1156T2F-S CPU with VFP
- 16KB instruction and data caches
- 64KB instruction and data TCMs
- ETM11CS and ETB11
- CPU, caches and TCMs running at 360MHz
- 512KB of on-chip AXI RAM at 180MHz
- JTAG connection for processor debug via board below
- DACs to control CPU's voltage
- ADCs to measure power consumption
- Control PLD to configure test chip and Core Tile hardware
- 3 user LEDs

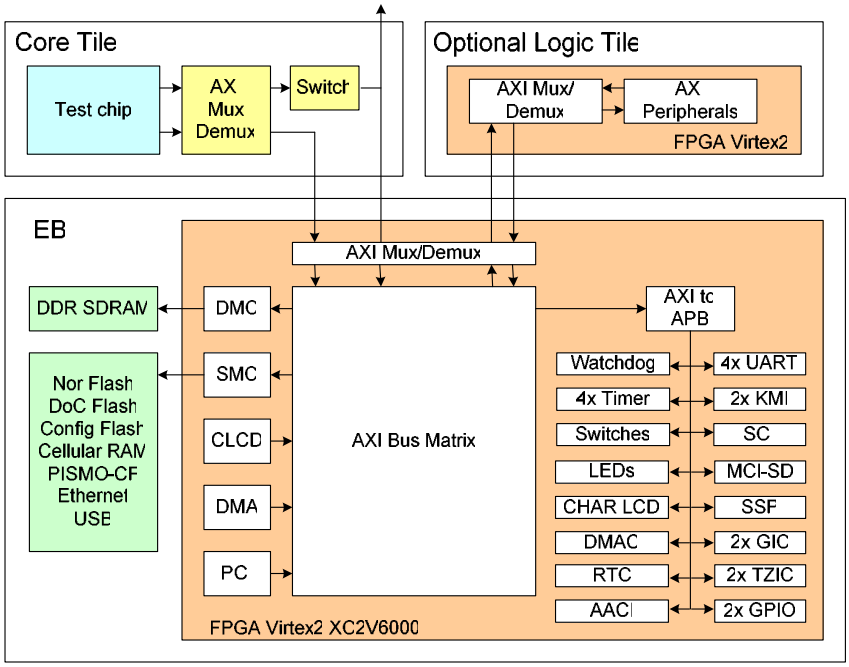


Comparison between AXI-based Core Tiles

Feature	CT11MPCore	CT1156T2F-S
CPU	ARM11 MPCore x4	ARM1156T2F-S
CPU features	MMU, Jazelle, arch v6 SMP	MPU, Thumb2
Trace	-	ETM11CS and ETB11
Level1 cache	32KB I and D	16KB I and D
Level2 cache	1MB shared	-
On-Chip AXI RAM	-	512KB
Tightly coupled memories	-	64KB I and D
CPU speed	200MHz	360MHz

Emulation Baseboard Features

- 2 sites for Core Tiles, Logic Tiles or Interface Tiles
- Virtex-II XC2V6000 FPGA
- 256MB DDR SDRAM and 2MB Cellular RAM
- 64MB NOR Flash
- PISMO expansion site (www.pismoworld.org)
- JTAG connector
- In-built hardware to program the FPGAs and PLDs of the system with a USB cable
- Standard frequency: 30MHz AXI or AHB



Deliverables

- FPGA RTL, synthesis scripts and bit files
- Example RTL for Logic Tiles on top of EB
- Boot monitor software
  - o System configuration
  - o NOR and DiskOnChip Flash utilities
  - o Retarget of standard C library
- Self-test software
  - o Checks that the hardware is functional
  - o Useful as example peripheral drivers
- Example software
  - o Loading of software from Ethernet or a Multimedia card to Flash
  - o Access to PCI system

Ordering Information

Part number	Description	Distributor
CTB56-BD-0230A	RealView Core Tile for ARM1156T2F-S (available Q4 06)	
VEREB-BD-0228ALF	RealView Emulation Baseboard	