SAA7144HL

Quadruple video input processor

Rev. 01 — 21 April 2005 | Product data sheet

1. General description

The SAA7144HL is a combination of four stand alone multistandard video decoders.

The SAA7144HL is a pure 3.3 V (5 V tolerant inputs and I/Os) CMOS circuit and a highly integrated circuit for video surveillance applications. All four video decoders are based on the principle of line-locked clock decoding and are able to decode the color of PAL, SECAM and NTSC signals into *“CCIR 601”* compatible color component values.

The SAA7144HL accepts as analog inputs in total eight CVBS sources from TV or VTR (two selectable CVBS sources for each of the four decoders).

Each of the four video decoders (A, B, C, D) contains an analog preprocessing circuit including source selection for two CVBS sources, anti-aliasing filter and Analog-to-Digital Converter (ADC), an automatic clamp and gain control, a Clock Generation Circuit (CGC), a digital multistandard decoder (PAL, NTSC and SECAM), a Brightness Contrast Saturation (BCS) control circuit, a multistandard text slicer see Figure 1 and a 27 MHz VBI data bypass.

The integrated high performance multistandard data slicer supports several VBI data standards:

- Teletext [WST (World Standard Teletext), CCST (Chinese teletext)] (625 lines)
- Teletext [US-WST, NABTS (North American Broadcast Text System) and MOJI (Japanese teletext)] (525 lines)
- Closed caption [Europe, US (line 21)]
- Wide Screen Signalling (WSS)
- Video Programming Signal (VPS)
- Time codes (VITC EBU/SMPTE)
- HIGH-speed VBI data bypass for Intercast™ application.

The circuit is I^2C-bus controlled via two I^2C-bus interfaces where two video decoders share one I^2C-bus interface on different I^2C-bus slave addresses. Each of the four video decoders of the SAA7144HL uses a register mapping which is compatible to the SAA7113H register mapping.

2. Features

2.1 General

- Four stand alone video decoder instances (A, B, C, D) with two selectable CVBS video inputs each and digital video outputs
- Programming register mapping identical to SAA7113H
- Small package (LQFP128)
- Requires only one crystal (24.576 MHz) for all standards shared by all video decoder instances
- CMOS 3.3 V device with 5 V tolerant digital inputs and I/O ports
- All four decoder instances are I^2C-bus controlled. Two decoder instances share one I^2C-bus interface (full read-back ability by an external controller, bit rate up to 400 kbit/s).

2.2 Features of each of the four video decoder instances A, B, C and D

- Two analog CVBS inputs with internal analog source selectors
- One analog preprocessing channel in differential CMOS style with built-in analog anti-aliasing filter
- Fully programmable static gain or automatic gain control for the selected CVBS channel
- Switchable white peak control
- Line-locked system clock frequencies
- Digital PLL for horizontal sync processing and clock generation, horizontal and vertical sync detection
- Automatic detection of 50 Hz and 60 Hz field frequency and automatic switching between PAL and NTSC standards
- Luminance and chrominance signal processing for PAL BGHI, PAL N, combination PAL N, PAL M, NTSC M, NTSC N, NTSC 4.43, NTSC Japan and SECAM
- User programmable luminance peaking or aperture correction
- Cross-color reduction for NTSC by chrominance comb filtering
- PAL delay line for correcting PAL phase errors
- Brightness Contrast Saturation (BCS) and hue control on-chip
- Multistandard VBI data slicer decoding World Standard Teletext (WST), North American Broadcast Text System (NABTS), closed caption, Wide Screen Signalling (WSS), Video Programming System (VPS), Vertical Interval Time Code (VITC) variants (EBU/SMPTE), etc.
- Standard ITU-R BT 656 Y-C_B-C_R 4 : 2 : 2 format (8-bit) on VPO output bus
- Enhanced ITU-R BT 656 output format on VPO output bus containing:
    - Active video
    - Decoded VBI data
- Boundary scan test circuit complies with the *“IEEE Std. 1149.b1 - 1994”*.

3. Applications

- Surveillance application.

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
V_{DDA}	analog supply voltage		3.1	3.3	3.5	V
T_{amb}	ambient temperature		0	25	70	°C
P_{A+D}	analog and digital power dissipation		-	1.1	-	W

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
SAA7144HL	LQFP128	plastic low profile quad flat package; 128 leads; body 14 × 20 × 1.4 mm	SOT425-1

6. Block diagram

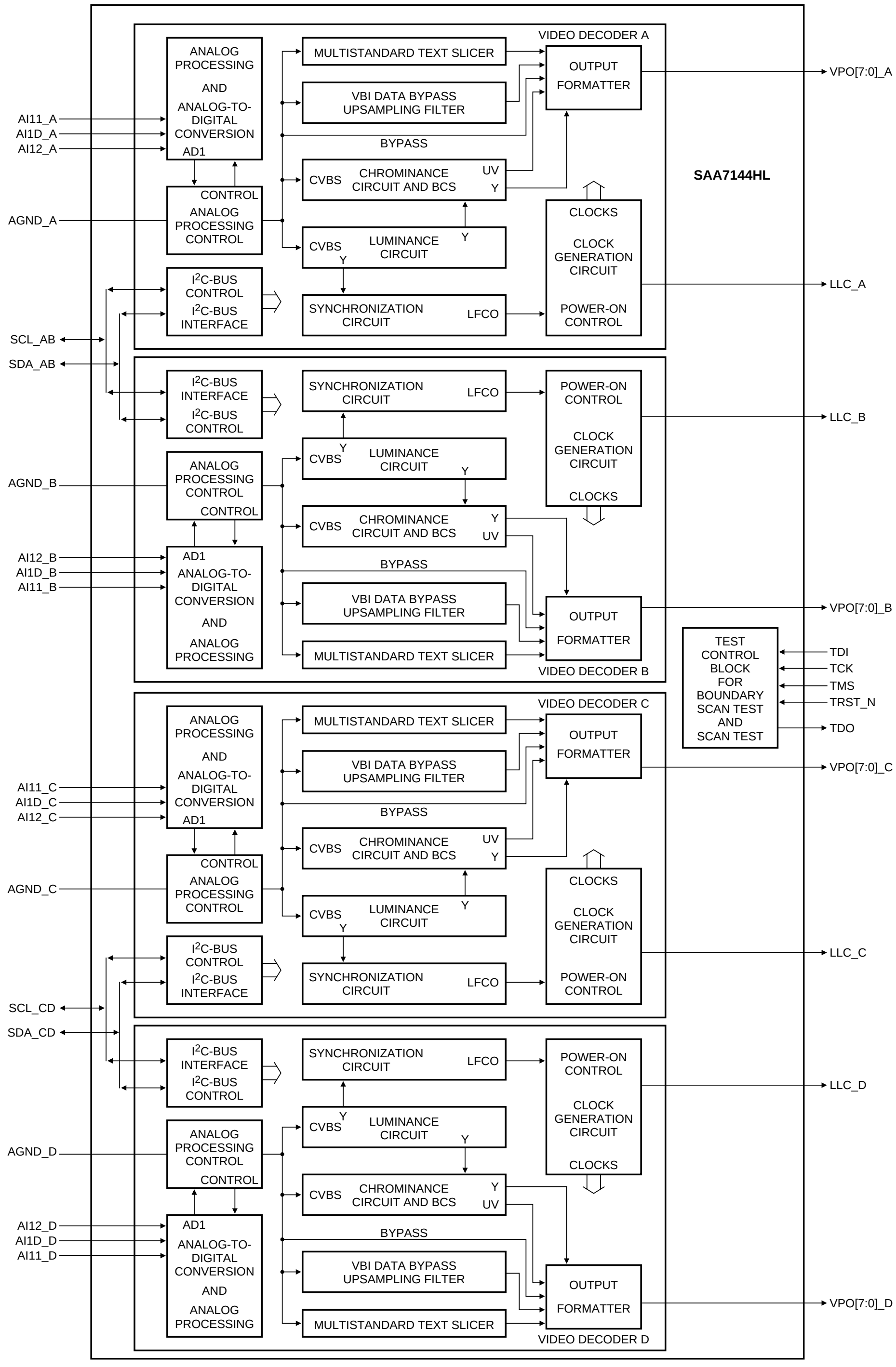


Fig 1. Block diagram of SAA7144HL.

7. Pinning information

7.1 Pinning

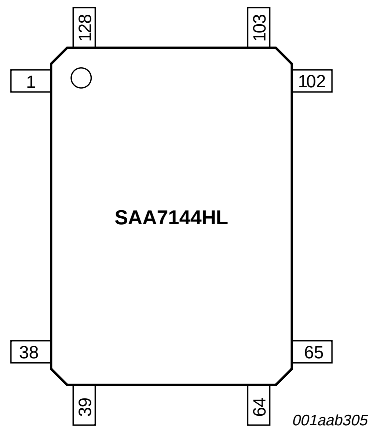


Fig 2. Pin configuration for LQFP128.

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
$V_{SSA1(DECA)}$	1	analog ground for analog supply of the Analog-to-Digital Converter (ADC) of video decoder A
$V_{DDA1(DECA)}$	2	analog supply voltage for the ADC (3.3 V) of video decoder A
AI11_A	3	analog input 11 of video decoder A
AI12_A	4	analog input 12 of video decoder A
AI1D_A	5	differential analog input for AI11 and AI12 of video decoder A; see Figure 28
AGND_A	6	analog ground reference for video decoder A
DNC1	7	do not connect; leave open
$V_{DDA0(DECA)}$	8	analog supply voltage for the internal Clock Generation Circuit (CGC) of video decoder A
$V_{SSA0(DECA)}$	9	analog ground for the internal CGC of video decoder A
$V_{SSA1(DECB)}$	10	analog ground for analog supply of the ADC of video decoder B
$V_{DDA1(DECB)}$	11	analog supply voltage for the ADC (3.3 V) of video decoder B
AI11_B	12	analog input 11 of video decoder B
AI12_B	13	analog input 12 of video decoder B
AI1D_B	14	differential analog input for AI11 and AI12 of video decoder B; see Figure 28
AGND_B	15	analog ground reference for video decoder B
DNC2	16	do not connect; leave open
DNC3	17	do not connect; leave open
$V_{DDA0(DECB)}$	18	analog supply voltage for the internal CGC of video decoder B

Table 3: Pin description *…continued*

Symbol	Pin	Description
$V_{SSA0(DECB)}$	19	analog ground for the internal CGC of video decoder B
$V_{SSA1(DECC)}$	20	analog ground for analog supply of the ADC of video decoder C
$V_{DDA1(DECC)}$	21	analog supply voltage for the ADC (3.3 V) of video decoder C
DNC4	22	do not connect; leave open
AI11_C	23	analog input 11 of video decoder C
AI12_C	24	analog input 12 of video decoder C
AI1D_C	25	differential analog input for AI11 and AI12 of video decoder C; see Figure 28
AGND_C	26	analog ground reference for video decoder C
DNC5	27	do not connect; leave open
$V_{DDA0(DECC)}$	28	analog supply voltage for the internal CGC of video decoder C
$V_{SSA0(DECC)}$	29	analog ground for the internal CGC of video decoder C
$V_{SSA1(DECD)}$	30	analog ground for analog supply of the ADC of video decoder D
$V_{DDA1(DECD)}$	31	analog supply voltage for the ADC (3.3 V) of video decoder D
AI11_D	32	analog input 11 of video decoder D
AI12_D	33	analog input 12 of video decoder D
AI1D_D	34	differential analog input for AI11 and AI12 of video decoder D; see Figure 28
AGND_D	35	analog ground reference for video decoder D
DNC6	36	do not connect; leave open
$V_{DDA0(DECD)}$	37	analog supply voltage for the internal CGC of video decoder D
$V_{SSA0(DECD)}$	38	analog ground for the internal CGC of video decoder D
DNC7	39	do not connect; leave open
DNC8	40	do not connect; leave open
DNC9	41	do not connect; leave open
DNC10	42	do not connect; leave open
DNC11	43	do not connect; leave open
DNC12	44	do not connect; leave open
DNC13	45	do not connect; leave open
SCL_AB	46	serial clock input (I^2C-bus) for instances A and B
SDA_AB	47	serial data input/output (I^2C-bus) for instances A and B
SCL_CD	48	serial clock input (I^2C-bus) for instances C and D
SDA_CD	49	serial data input/output (I^2C-bus) for instances C and D
LLC_D	50	line-locked clock output (27 MHz) of video decoder D
VPO7_D	51	digital video output bus signal VPO7 of video decoder D
VPO6_D	52	digital video output bus signal VPO6 of video decoder D
VPO5_D	53	digital video output bus signal VPO5 of video decoder D
V_{DDDE}	54	supply for digital pad ring (3.3 V)
V_{SSDE}	55	ground for digital pad ring
VPO4_D	56	digital video output bus signal VPO4 of video decoder D
VPO3_D	57	digital video output bus signal VPO3 of video decoder D

Table 3: Pin description *…continued*

Symbol	Pin	Description
V_{SSDI}	58	ground for digital core
V_{DDDI}	59	supply for digital core (3.3 V)
VPO2_D	60	digital video output bus signal VPO2 of video decoder D
VPO1_D	61	digital video output bus signal VPO1 of video decoder D
VPO0_D	62	digital video output bus signal VPO0 of video decoder D
LLC_C	63	line-locked clock output (27 MHz) of video decoder C
VPO7_C	64	digital video output bus signal VPO7 of video decoder C
VPO6_C	65	digital video output bus signal VPO6 of video decoder C
DNC14	66	do not connect; leave open
VPO5_C	67	digital video output bus signal VPO5 of video decoder C
VPO4_C	68	digital video output bus signal VPO4 of video decoder C
V_{DDDE}	69	supply for digital pad ring (3.3 V)
V_{SSDE}	70	ground for digital pad ring
VPO3_C	71	digital video output bus signal VPO3 of video decoder C
VPO2_C	72	digital video output bus signal VPO2 of video decoder C
V_{SSDI}	73	ground for digital core
V_{DDDI}	74	supply for digital core (3.3 V)
DNC15	75	do not connect; leave open
DNC16	76	do not connect; leave open
VPO1_C	77	digital video output bus signal VPO1 of video decoder C
DNC17	78	do not connect; leave open
VPO0_C	79	digital video output bus signal VPO0 of video decoder C
V_{SSDA}	80	oscillator supply ground
XTALO	81	oscillator output
DNC18	82	do not connect; leave open
DNC19	83	do not connect; leave open
XTALI	84	oscillator input
V_{DDDA}	85	oscillator supply voltage (3.3 V)
LLC_B	86	line-locked clock output (27 MHz) of video decoder B
VPO7_B	87	digital video output bus signal VPO7 of video decoder B
DNC20	88	do not connect; leave open
VPO6_B	89	digital video output bus signal VPO6 of video decoder B
DNC21	90	do not connect; leave open
V_{SSDI}	91	ground for digital core
DNC22	92	do not connect; leave open
V_{DDDI}	93	supply for digital core (3.3 V)
VPO5_B	94	digital video output bus signal VPO5 of video decoder B
VPO4_B	95	digital video output bus signal VPO4 of video decoder B
V_{DDDE}	96	supply for digital pad ring (3.3 V)
V_{SSDE}	97	ground for digital pad ring
DNC23	98	do not connect; leave open

Table 3: Pin description *…continued*

Symbol	Pin	Description
VPO3_B	99	digital video output bus signal VPO3 of video decoder B
VPO2_B	100	digital video output bus signal VPO2 of video decoder B
VPO1_B	101	digital video output bus signal VPO1 of video decoder B
DNC24	102	do not connect; leave open
VPO0_B	103	digital video output bus signal VPO0 of video decoder B
LLC_A	104	line-locked clock output (27 MHz) of video decoder A
VPO7_A	105	digital video output bus signal VPO7 of video decoder A
VPO6_A	106	digital video output bus signal VPO6 of video decoder A
VPO5_A	107	digital video output bus signal VPO5 of video decoder A
V_{SSDI}	108	ground for digital core
V_{DDDI}	109	supply for digital core (3.3 V)
VPO4_A	110	digital video output bus signal VPO4 of video decoder A
V_{DDDE}	111	supply for digital pad ring (3.3 V)
V_{SSDE}	112	ground for digital pad ring
VPO3_A	113	digital video output bus signal VPO3 of video decoder A
VPO2_A	114	digital video output bus signal VPO2 of video decoder A
VPO1_A	115	digital video output bus signal VPO1 of video decoder A
VPO0_A	116	digital video output bus signal VPO0 of video decoder A
TDI	117	test data input for boundary scan test [1]
TDO	118	test data output for boundary scan test [1]
TMS	119	test mode select input for boundary scan test or scan test [1]
TCK	120	test clock for boundary scan test [1]
TRST_N	121	test reset input (active LOW), for boundary scan test [1] [2] [3]
DNC25	122	do not connect; leave open
DNC26	123	do not connect; leave open
DNC27	124	do not connect; leave open
DNC28	125	do not connect; leave open
DNC29	126	do not connect; leave open
DNC30	127	do not connect; leave open
DNC31	128	do not connect; leave open

[1] In accordance with the *"IEEE1149.1"* standard the pads TDI, TMS, TCK and TRST_N are input pads with an internal pull-up transistor and TDO is a 3-state output pad.

[2] For board design without boundary scan implementation connect the TRST_N pin to ground.

[3] This pin provides easy initialization of the Boundary Scan Test (BST) circuit. TRST_N can be used to force the Test Access Port (TAP) controller to the TEST_LOGIC_RESET state (normal operation) at once.

8. Functional description

The following functional descriptions are related to each of the four stand alone decoder cores (A, B, C and D).

8.1 Analog input processing

The analog input processing part consists of a source switch to select one out of two video inputs, clamp circuit, analog amplifier, anti-alias filter and video 9-bit CMOS ADC; see Figure 6.

8.2 Analog control circuits

The anti-alias filters are adapted to the line-locked clock frequency via a filter control circuit. The characteristic is shown in Figure 3. During the vertical blanking period, gain and clamping control are frozen.

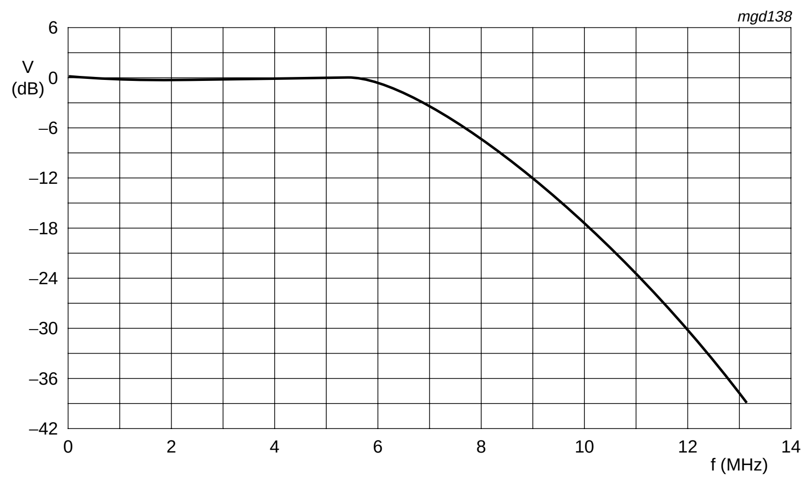


Fig 3. Anti-alias filter.

8.2.1 Clamping

The clamp control circuit controls the correct clamping of the analog input signals. The coupling capacitor is also used to store and filter the clamping voltage. An internal digital clamp comparator generates the information with respect to clamp-up or clamp-down. The clamping levels for the two ADC channels are fixed for luminance (120) and chrominance (256). Clamping time in normal use is set with the HCL pulse on the back porch of the video signal.

8.2.2 Gain control

The gain control circuit receives (via the I^2C-bus) the static gain levels for the analog amplifier or controls this amplifier automatically via a built-in Automatic Gain Control (AGC) as part of the Analog Input Control (AICO).

The AGC (automatic gain control for luminance) is used to amplify a CVBS signal to the required signal amplitude, matched to the ADC input voltage range. The AGC active time is the sync bottom of the video signal.

Signal (white) peak control limits the gain at signal overshoots. The flow charts (see Figure 7 and Figure 8) show more details of the AGC. The influence of supply voltage variation within the specified range is automatically eliminated by clamp and automatic gain control.

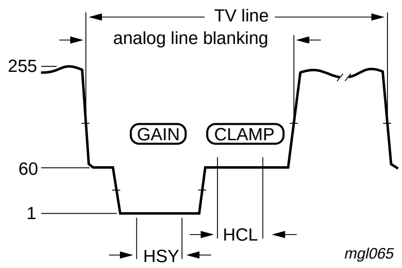


Fig 4. Analog line with clamp (HCL) and gain range (HSY).

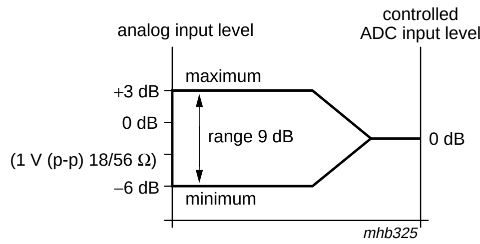
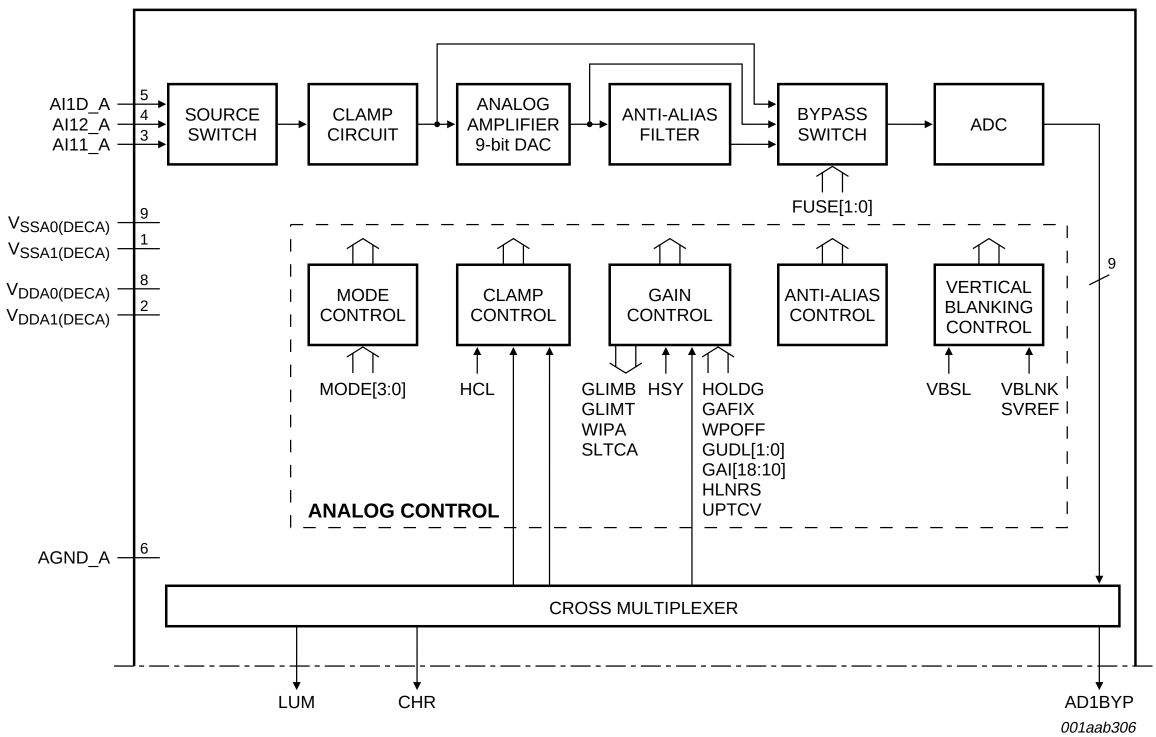
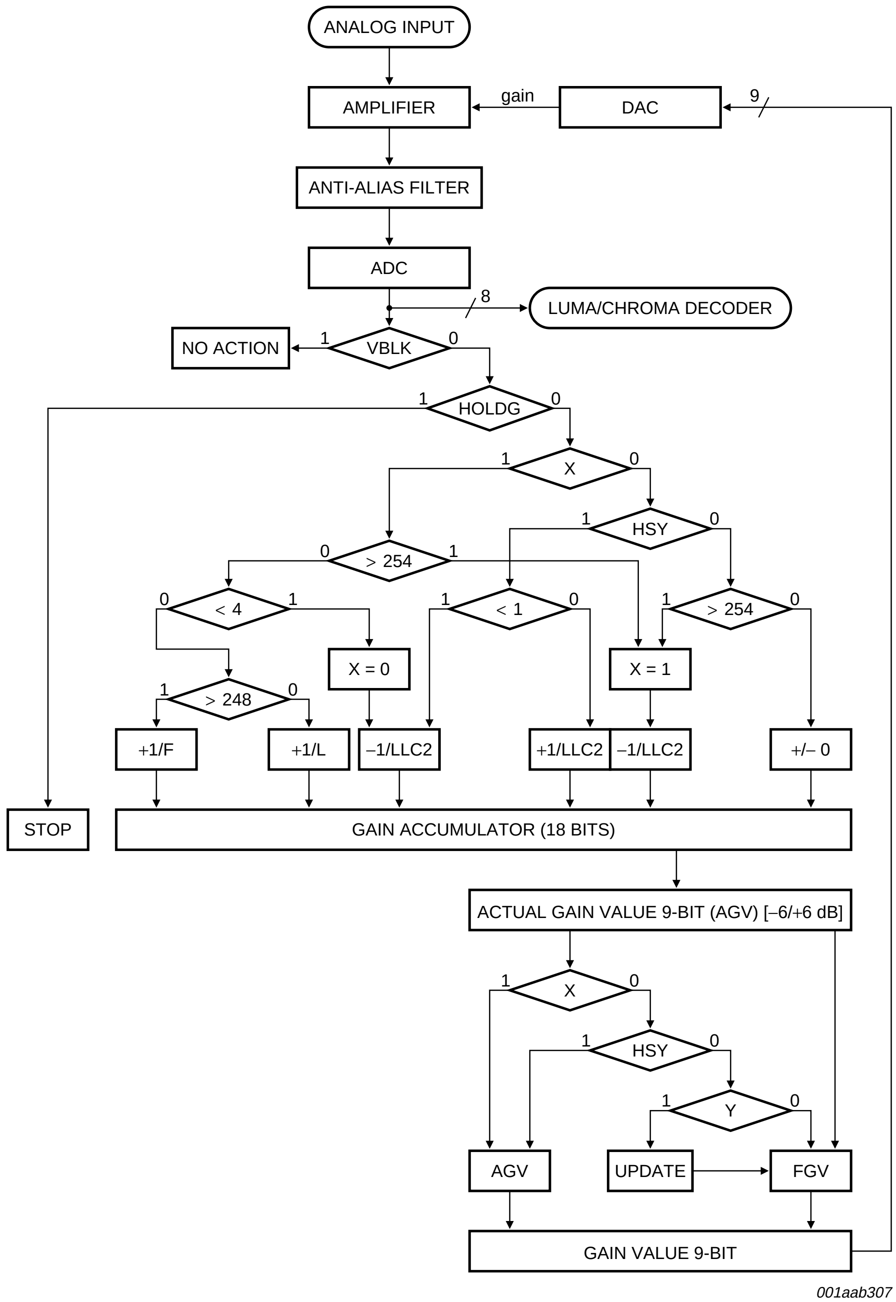


Fig 5. Automatic gain range.



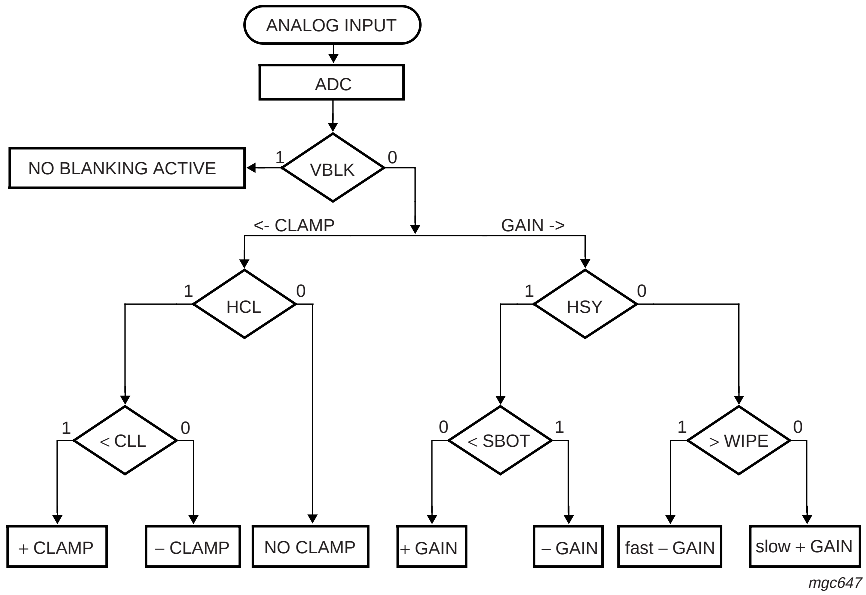
This is valid for decoder A, B, C and D. Here an example for decoder A is shown.

Fig 6. Analog input processing using the SAA7144HL as differential front-end with 9-bit ADC (continued in Figure 10).



X = system variable; $Y = |AGV - FGV| > GUDL$; GUDL = gain update level (adjustable);
VBLK = vertical blanking pulse; HSY = horizontal sync pulse; AGV = actual gain value;
FGV = frozen gain value.

Fig 7. Gain flow chart.



WIPE = white peak level (254).

SBOT = sync bottom level (1).

CLL = clamp level [60 Y (128 C)].

HSY = horizontal sync pulse.

HCL = horizontal clamp pulse.

Fig 8. Clamp and gain flow.

8.3 Chrominance processing

The 9-bit chrominance signal is fed to the multiplication inputs of a quadrature demodulator, where two subcarrier signals from the local oscillator DTO are applied (0° and 90° phase relationship to the demodulator axis). The frequency is dependent on the present color standard.

The output signals of the multipliers are low-pass filtered (four programmable characteristics) to achieve the desired bandwidth for the color difference signals (PAL, NTSC) or the 0° and 90° FM signals (SECAM).

The color difference signals are fed to the Brightness Contrast Saturation (BCS) block, which contains the following five functions:

- AGC (automatic gain control for chrominance PAL and NTSC)
- Chrominance amplitude matching (different gain factors for (R – Y) and (B – Y) to achieve CCIR-601 levels C_R and C_B for all standards)
- Chrominance saturation control
- Luminance contrast and brightness
- Limiting Y-C_B-C_R to the values 1 (minimum) and 254 (maximum) to fulfil CCIR-601 requirements.

The SECAM processing contains the following blocks:

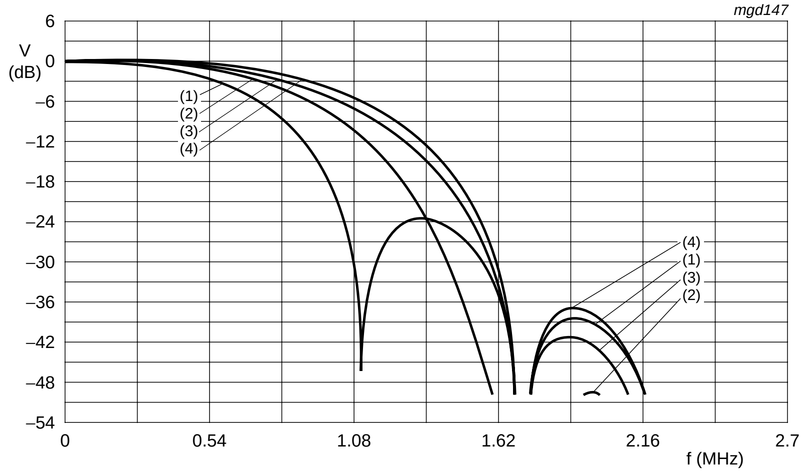
- Baseband ‘bell’ filters to reconstruct the amplitude and phase equalized 0° and 90° FM signals
- Phase demodulator and differentiator (FM-demodulation)
- De-emphasis filter to compensate the pre-emphasized input signal, including frequency offset compensation (DB or DR white carrier values are subtracted from the signal, controlled by the SECAM switch signal).

The burst processing block provides the feedback loop of the chrominance PLL and contains the following:

- Burst gate accumulator
- Color identification and color killer
- Comparison nominal/actual burst amplitude (PAL/NTSC standards only)
- Loop filter chrominance gain control (PAL/NTSC standards only)
- Loop filter chrominance PLL (only active for PAL/NTSC standards)
- PAL/SECAM sequence detection, H/2-switch generation
- Increment generation for DTO with divider to generate stable subcarrier for non-standard signals.

The chrominance comb filter block eliminates crosstalk between the chrominance channels in accordance with the PAL standard requirements. For NTSC color standards the chrominance comb filter can be used to eliminate crosstalk from luminance to chrominance (cross-color) for vertical structures. The comb filter can be switched off if desired. The embedded line delay is also used for SECAM recombination (cross-over switches).

The resulting signals are fed to the variable Y-delay compensation and the output interface, which contains the VPO output formatter and the output control logic; see Figure 10.



Transfer characteristics of the chrominance low-pass dependent on CHBW[1:0] settings.

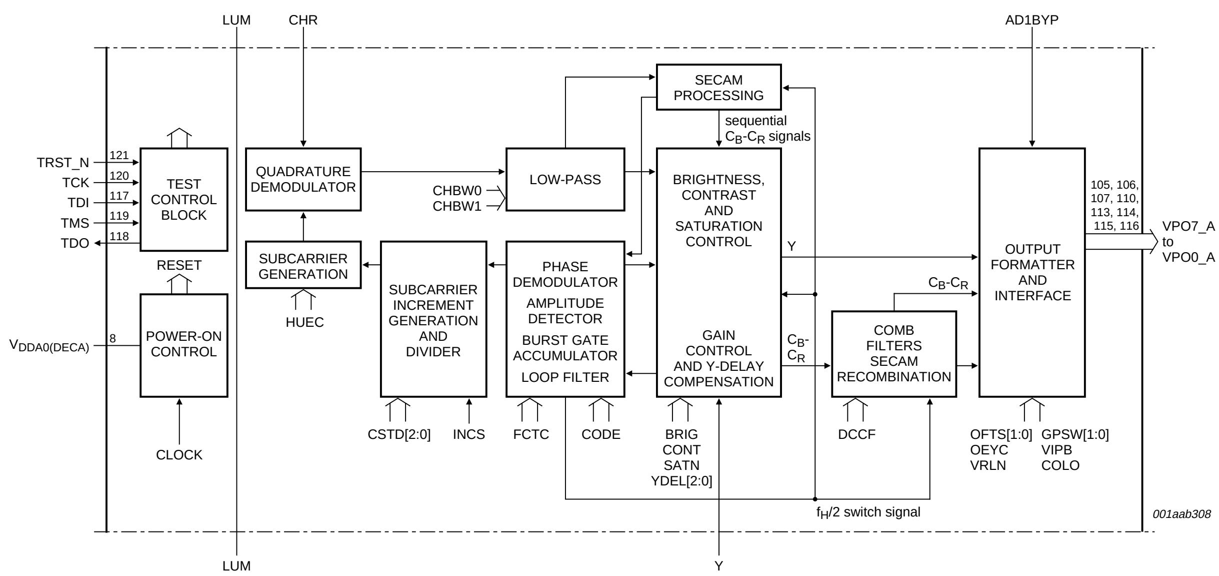
(1) CHBW[1:0] = 00.

(2) CHBW[1:0] = 01.

(3) CHBW[1:0] = 10.

(4) CHBW[1:0] = 11.

Fig 9. Chrominance filter.



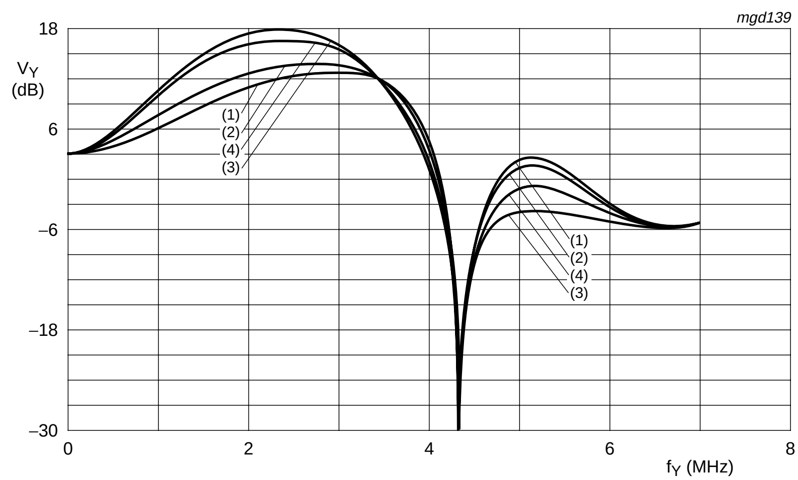
This is valid for decoder A, B, C and D. Here an example for decoder A is shown.

Fig 10. Chrominance circuit, text slicer, VBI-bypass, output formatting, power and test control (continued from Figure 6 and continued in Figure 17).

8.4 Luminance processing

The 9-bit luminance signal, a digital CVBS format, is fed through a switchable prefilter. High frequency components are emphasized to compensate for loss. The following chrominance trap filter (f_0 = 4.43 MHz or 3.58 MHz center frequency set according to the selected color standard) eliminates most of the color carrier signal. It can be bypassed via I^2C-bus bit BYPS (subaddress 09h, bit 7).

The high frequency components of the luminance signal can be peaked (control for sharpness improvement via I^2C-bus subaddress 09h, see Table 33) in two band-pass filters with selectable transfer characteristic. This signal is then added to the original (unpeaked) signal. For the resulting frequency characteristics see Figure 11 to Figure 16. A switchable amplifier achieves common DC amplification, because the DC gains are different in both chrominance trap modes. The improved luminance signal is fed to the BCS control located in the chrominance processing block; see Figure 17.



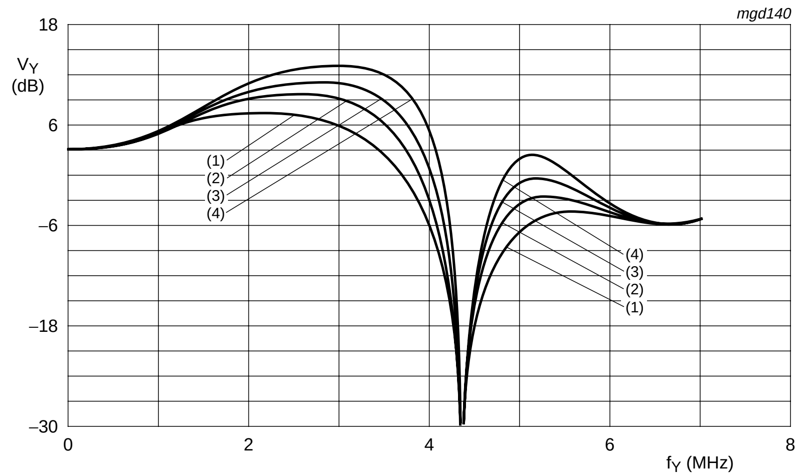
(1) 43h

(2) 53h

(3) 63h

(4) 73h

Fig 11. Luminance control SA 09h, 4.43 MHz trap, prefilter on, different aperture band-pass center frequencies.



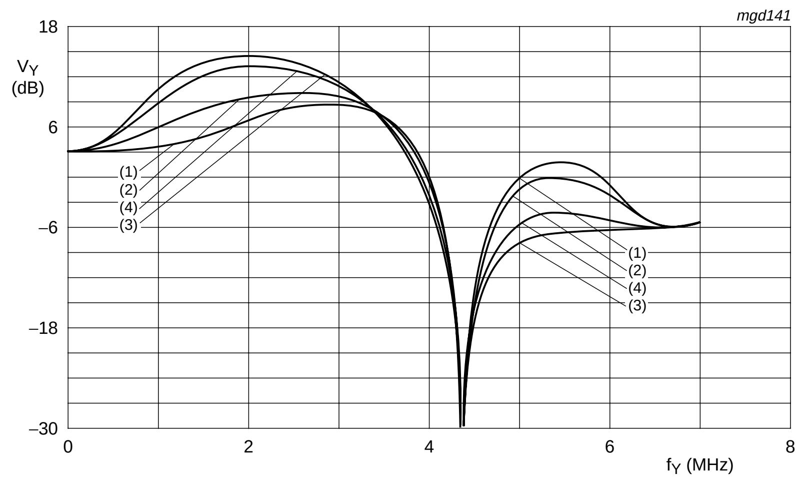
(1) 40h

(2) 41h

(3) 42h

(4) 43h

Fig 12. Luminance control SA 09h, 4.43 MHz trap, prefilter on, different aperture factors.



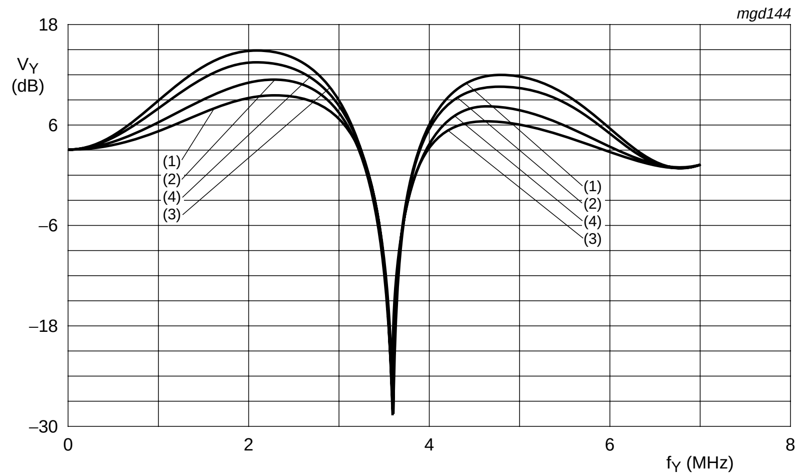
(1) 03h

(2) 13h

(3) 23h

(4) 33h

Fig 13. Luminance control SA 09h, 4.43 MHz trap, prefilter off, different aperture band-pass center frequencies.



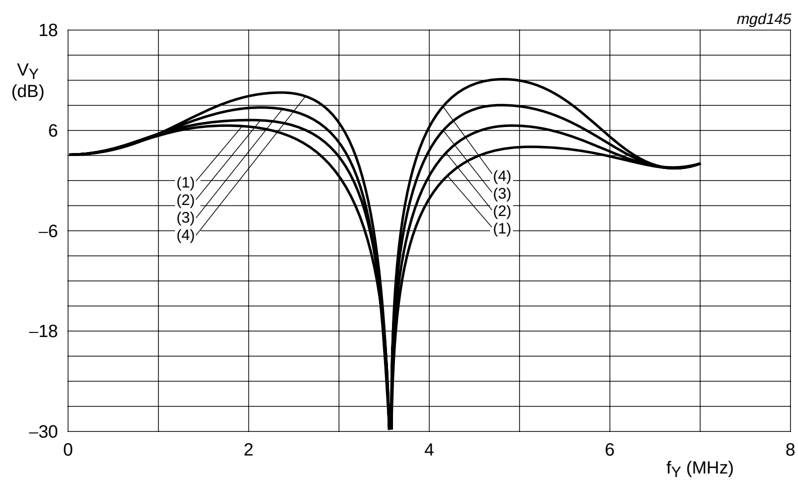
(1) 43h

(2) 53h

(3) 63h

(4) 73h

Fig 14. Luminance control SA 09h, 3.58 MHz trap, prefilter on, different aperture band-pass center frequencies.



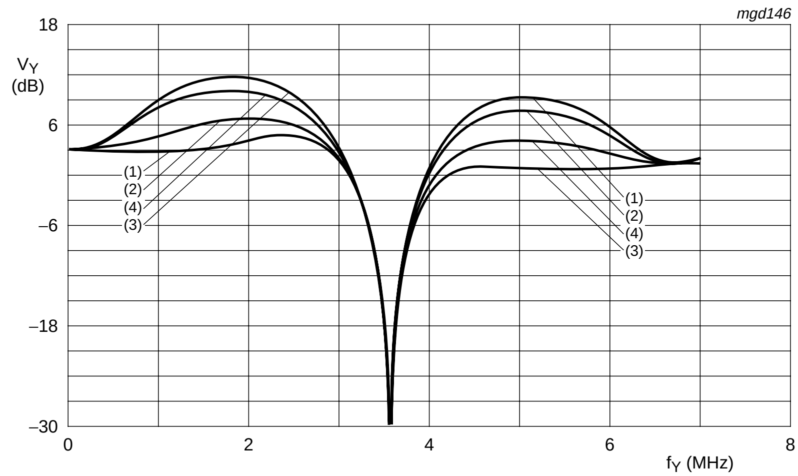
(1) 40h

(2) 41h

(3) 42h

(4) 43h

Fig 15. Luminance control SA 09h, 3.58 MHz trap, prefilter on, different aperture factors.



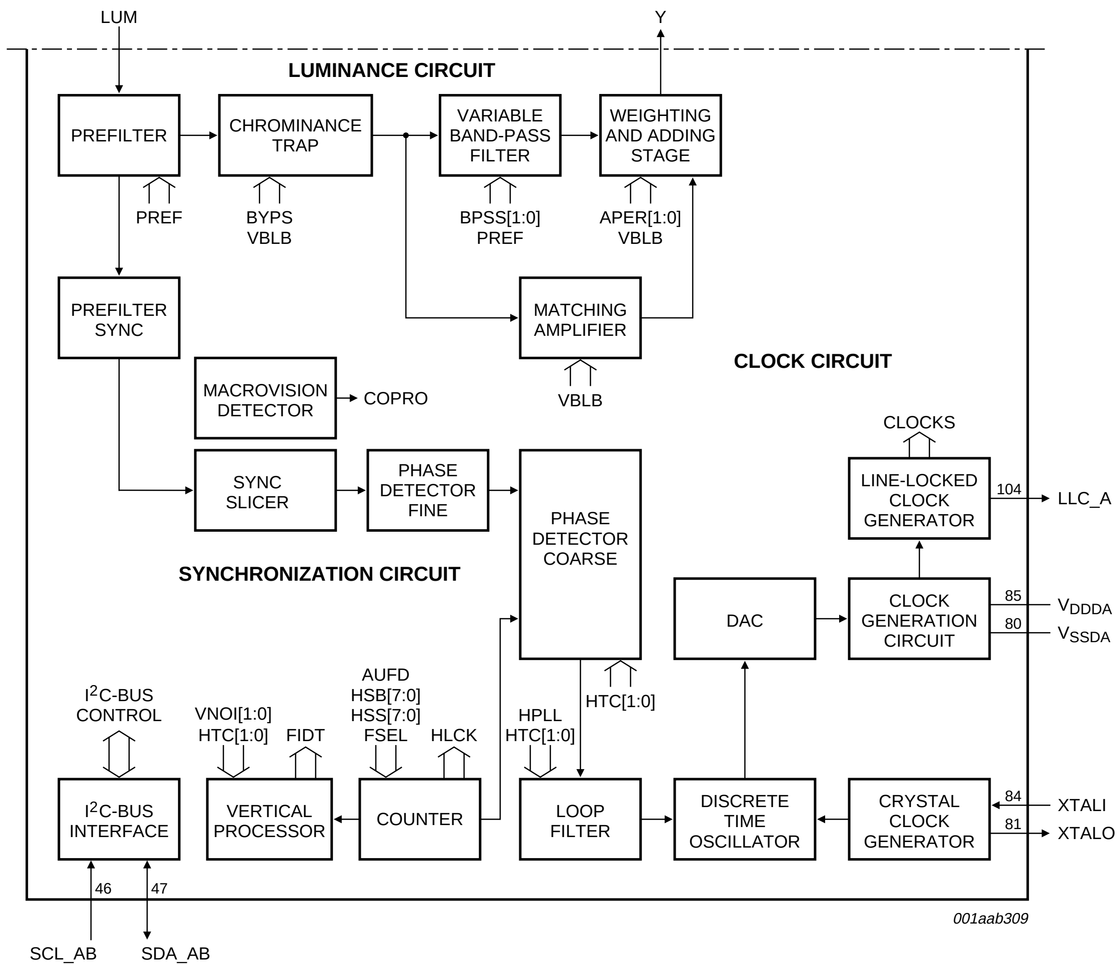
(1) 03h

(2) 13h

(3) 23h

(4) 33h

Fig 16. Luminance control SA 09h, 3.58 MHz trap, prefilter off, different aperture band-pass center frequencies.



This is valid for decoder A, B, C and D. Here an example for decoder A is shown.

Fig 17. Luminance and sync processing (continued from Figure 10).

8.5 Synchronization

The prefiltered luminance signal is fed to the synchronization stage. Its bandwidth is further reduced to 1 MHz in a low-pass filter. The sync pulses are sliced and fed to the phase detectors where they are compared with the sub-divided clock frequency. The resulting output signal is applied to the loop filter to accumulate all phase deviations. Internal signals (e.g. HCL and HSY) are generated in accordance with analog front-end requirements. The loop filter signal drives an oscillator to generate the line frequency control signal LFCO; see Figure 18.

The detection of ‘pseudo syncs’ as part of the Macrovision® copy protection standard is also achieved within the synchronization circuit.

The result is reported as flag COPRO within the decoder status byte at subaddress 1Fh.

8.6 Clock generation circuit

The internal CGC generates all clock signals required for the video input processor.

The internal signal LFCO is a digital-to-analog converted signal provided by the horizontal PLL. It is the multiple of the line frequency:

6.75 MHz = 429 $\times$ f_H (50 Hz), or

6.75 MHz = 432 $\times$ f_H (60 Hz).

The LFCO signal is multiplied by a factor of 2 and 4 in the internal PLL circuit (including phase detector, loop filtering, VCO and frequency divider) to obtain the output clock signals. The rectangular output clocks have a 50 % duty factor.

Table 4: Clock frequencies

Clock	Frequency (MHz)
XTAL	24.576
LLC	27
LLC2 (internal)	13.5
LLC4 (internal)	6.75
LLC8 (virtual)	3.375

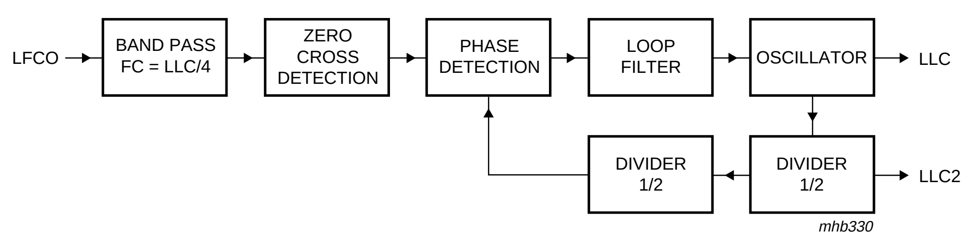
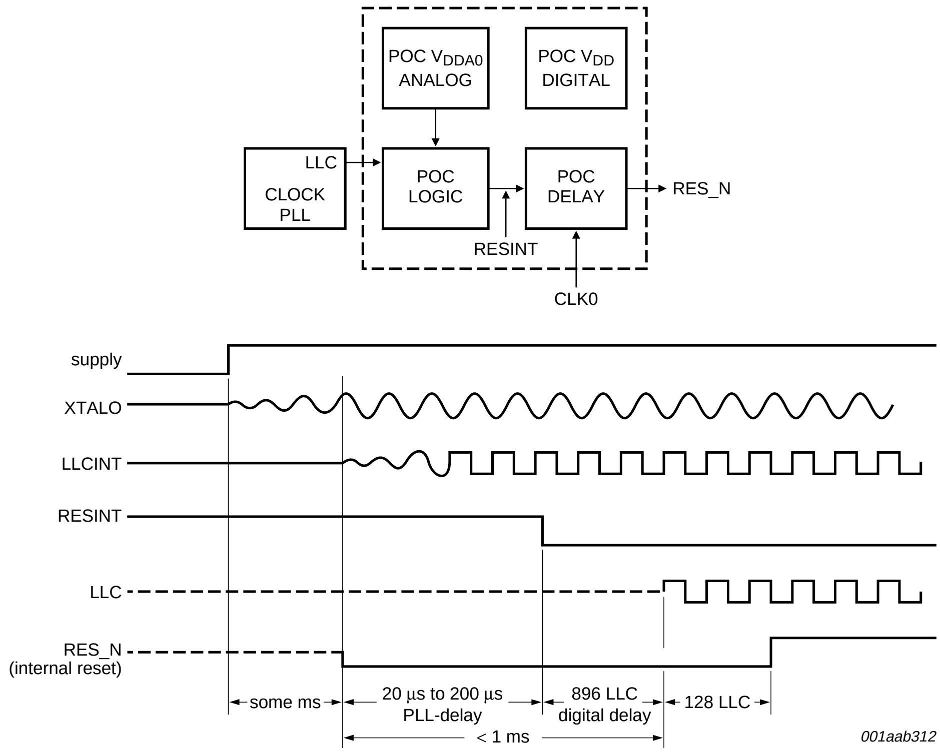


Fig 18. Block diagram of clock generation circuit.

8.7 Power-on reset

A missing clock, insufficient digital or analog V_{DDA0} supply voltages will start the reset sequence; all outputs are forced to 3-state; see Figure 19.

After sufficient power supply voltage, the outputs LLC and SDA return from 3-state to active.



POC = Power-on control.

XTALO = crystal oscillator output.

LLCINT = internal system clock.

RESINT = internal reset.

LLC = line-locked clock output.

RES_N = delayed internal reset.

Fig 19. Power-on control circuit.

Table 5: Power-on control sequence

Internal power-on control sequence	Pin output status	Remarks
Directly after power-on asynchronous reset	VPO7 to VPO0, SDA and LLC are in high-impedance state	direct switching to high-impedance for 20 ms to 200 ms
Synchronous reset sequence	LLC and SDA become active; VPO7 to VPO0, are held in high-impedance state	internal reset sequence
Status after power-on control sequence	VPO7 to VPO0, are held in high-impedance state	after power-on (reset sequence) a complete I^2C-bus transmission is required

8.8 Multistandard VBI data slicer

The multistandard data slicer is a Vertical Blanking Interval (VBI) and Full Field (FF) video data acquisition block. In combination with software modules the slicer acquires most existing formats of broadcast VBI and FF data.

The implementation and programming model is in accordance with the VBI data slicer built into the multimedia video data acquisition circuit SAA5284.

The circuitry recovers the actual clock phase during the clock run-in period, slices the data bits with the selected data rate, and groups them into bytes. The clock frequency, signal source, field frequency and accepted error count must be defined via the I^2C-bus in subaddress 40h, bits 7 to 4.

Several standards can be selected per VBI line. The supported VBI data standards are described in Table 6.

The programming of the desired standards is done via I^2C-bus subaddresses 41h to 57h (LCR2[7:0] to LCR24[7:0]); see detailed description in Section 8.10. To adjust the slicers processing to the signals source, there are offsets in horizontal and vertical direction available via the I^2C-bus in subaddresses 5Bh (bits 2 to 0), 59h (HOFF10 to HOFF0) and 5Bh (bit 4), 5Ah (VOFF8 to VOFF0). The formatting of the decoded VBI data is done within the output interface to the VPO-bus. For a detailed description of the sliced data format see Table 20.

Table 6: Supported VBI standards

Standard type	Data rate (Mbit/s)	Framing code	FC window	Hamming check
Teletext EuroWST, CCST	6.9375	27h	WST625	always
European closed caption	0.500	001	CC625	
VPS	5	9951h	VPS	
Wide screen signalling bits	5	1E3C1Fh	WSS	
US teletext (WST)	5.7272	27h	WST525	always
US closed caption (line 21)	0.503	001	CC525	
Teletext	6.9375	programmable	general text	optional
VITC/EBU time codes (Europe)	1.8125	programmable	VITC625	
VITC/SMPTE time codes (USA)	1.7898	programmable	VITC625	
US NABTS	5.7272	programmable	NABTS	optional
MOJI (Japanese)	5.7272	programmable (A7h)	Japtext	
Japanese format switch (L20/22)	5	programmable		

8.9 VBI-raw data bypass

For a 27 MHz VBI-raw data bypass the digitized CVBS signal is upsampled after analog-to-digital conversion. Suppressing of the back folded CVBS frequency components after upsampling is achieved by an interpolation filter; see Figure 20.

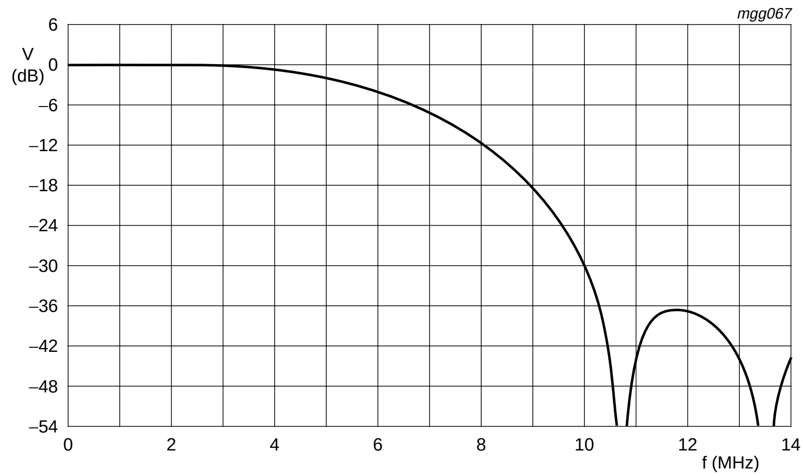


Fig 20. Interpolation filter for the upsampled CVBS signal.

8.10 Digital output port

The 8-bit VPO-bus can carry 16 data types in three different formats, selectable by the control registers LCR2 to LCR24 (see also Section 9, subaddresses 41h to 57h). OEYC (output enable $Y\text{-}C_B\text{-}C_R$) bit (subaddress 11h, bit 3) in I^2C-bus register needs to be set to logic 1 to enable the VPO-bus.

Table 7: VPO-bus data formats and types [1]

Data type number	Data format	Data type	Name	Number of valid bytes sent per line
0	sliced	teletext EuroWST, CCST	WST625	88
1	sliced	European closed caption	CC625	8
2	sliced	VPS	VPS	56
3	sliced	wide screen signalling bits	WSS	32
4	sliced	US teletext (WST)	WST525	72
5	sliced	US closed caption (line 21)	CC525	8
6	$Y\text{-}C_B\text{-}C_R$ 4 : 2 : 2	video component signal, VBI region	test line	1440
7	raw	oversampled CVBS data	Intercast™	programmable
8	sliced	teletext	general text	88
9	sliced	VITC/EBU time codes (Europe)	VITC625	26
10	sliced	VITC/SMPTE time codes (USA)	VITC625	26
11	reserved	reserved	-	-
12	sliced	US NABTS	NABTS	72
13	sliced	MOJI (Japanese)	Japtext	74
14	sliced	Japanese format switch (L20/22)	JFS	56
15	$Y\text{-}C_B\text{-}C_R$ 4 : 2 : 2	video component signal, active video region	active video	1440

[1] The number of valid bytes per line can be less for the sliced data format if standard not recognized (wrong standard or poor input signal).

For each LCR value from 2 to 23 the data type can be programmed individually. LCR2 to LCR23 refer to line numbers. The selection in LCR24 values is valid for the rest of the corresponding field. The upper nibble contains the value for field 1 (odd), the lower nibble for field 2 (even). The relationship between LCR values and line numbers can be adjusted via VOFF8 to VOFF0 (located in subaddresses 5Bh, bit 4 and 5Ah, bits 7 to 0). The recommended values are 07h for 50 Hz sources and 0Ah for 60 Hz sources, to accommodate line number conventions as used for PAL, SECAM and NTSC standards; see Table 11 to Table 14.

Some details about data types:

- **Active video** (data type 15) component Y-C_B-C_R 4 : 2 : 2 signal, 720 active pixels per line. Format and nominal levels are given in Figure 21 and Table 16.
- **Test line** (data type 6), is similar to decoded Y-C_B-C_R data as in active video, with two exceptions:
  – vertical filter (chrominance comb filter for NTSC standards, PAL-phase-error correction) within the chrominance processing is disabled
  – peaking and chrominance trap are bypassed within the luminance processing, if I^2C-bus bit VBLB is set. This data type is defined for future enhancements; it could be activated for lines containing standard test signals within the vertical blanking period; currently the most sources do not contain test lines.

  This data type is available only in lines with VREF = 0, see I^2C-bus detail section, Table 41. Format and nominal levels are given in Figure 21 and Table 16.
- **Raw samples** (data type 7) oversampled CVBS-signal for Intercast™ applications; the data rate is 27 MHz. The horizontal range is programmable via HSB7 to HSB0, HSS7 to HSS0 and HDEL1 to HDEL0; see Section 9.3.6, Section 9.3.7 and Section 9.3.16 and Table 30, Table 31 and Table 40. Format and nominal levels are given in Figure 22 and Table 18.
- **Sliced data** (various standards, data types 0 to 5 and 8 to 14). The format is given in Table 20.

The data type selections by LCR are overruled by setting VIPB (subaddress 11h bit 1) to logic 1. This setting is mainly intended for device production tests. The VPO-bus carries the upper or lower 8 bits of the ADC depending on the ADLSB (subaddress 13h bit 7) setting. The output configuration is done via MODE3 to MODE0 settings (subaddress 02h bits 3 to 0; see Table 27).

The SAV/EAV timing reference codes define start and end of valid data regions.

Table 8: SAV/EAV format

Bit	Symbol	Description
7		logic 1
6	F	field bit
		1st field: F = 0
		2nd field: F = 1
		for vertical timing see Table 9 and Table 10
5	V	vertical blanking bit
		VBI: V = 1
		active video: V = 0
		for vertical timing see Table 9 and Table 10
4	H	H = 0 in SAV; H = 1 in EAV
3 to 0	P[3:0]	reserved; evaluation not recommended (protection bits according to ITU-R BT 656)

The generation of the H-bit and consequently the timing of SAV/EAV corresponds to the selected data format. H = 0 during active data region. For all data formats excluding data type 7 (raw data), the length of the active data region is 1440 LLC. For the $Y\text{-}C_B\text{-}C_R$ 4 : 2 : 2 formats (data types 15 and 6) every clock cycle within this range contains valid data; see Table 16.

The sliced data stream (various standards, data types 0 to 5 and 8 to 14; see Table 20) contains also invalid cycles marked as 00h.

The length of the raw data region (data type 7) is programmable via HSB7 to HSB0 and HSS7 to HSS0 (subaddresses 06h and 07h; see Figure 22).

During horizontal blanking period between EAV and SAV the ITU-blanking code sequence '-80-10-80-10-...' is transmitted.

The position of the F-bit is constant according to ITU-R BT 656; see Table 9 and Table 10.

The V-bit can be generated in four different ways (see Table 9 and Table 10) controlled via OFTS1 and OFTS0 (subaddress 10h, bits 7 and 6), VRLN (subaddress 10h, bit 3) and LCR2 to LCR24 (subaddresses 41h to 57h).

F and V bits change synchronously with the EAV code.

Table 9: 525 lines/60 Hz vertical timing

Line number	F (ITU-R BT 656)	V			
		OFTS1 = 0; OFTS0 = 0 (ITU-R BT 656)	OFTS1 = 0; OFTS0 = 1		OFTS1 = 1; OFTS0 = 0
			VRLN = 0	VRLN = 1	
1 to 3	1	1	1	1	according to selected data type via LCR2 to LCR24 (subaddresses 41h to 57h): data types 0 to 14: V = 1; data type 15: V = 0
4 to 19	0	1	1	1	
20	0	0	1	1	
21	0	0	1	0	
22 to 261	0	0	0	0	
262	0	0	1	0	
263	0	0	1	1	
264 and 265	0	1	1	1	
266 to 282	1	1	1	1	
283	1	0	1	1	
284	1	0	1	0	
285 to 524	1	0	0	0	
525	1	0	1	0	

Table 10: 625 lines/50 Hz vertical timing

Line number	F (ITU-R BT 656)	V			
		OFTS1 = 0; OFTS0 = 0 (ITU-R BT 656)	OFTS1 = 0; OFTS0 = 1		OFTS1 = 1; OFTS0 = 0
			VRLN = 0	VRLN = 1	
1 to 22	0	1	1	1	according to selected data type via LCR2 to LCR24 (subaddresses 41h to 57h): data types 0 to 14: V = 1; data type 15: V = 0
23	0	0	1	0	
24 to 309	0	0	0	0	
310	0	0	1	0	
311 and 312	0	1	1	1	
313 to 335	1	1	1	1	
336	1	0	1	0	
337 to 622	1	0	0	0	
623	1	0	1	0	
624 and 625	1	1	1	1	

Table 11: Relationship of LCR to line numbers in 525 lines/60 Hz systems (part 1)

Vertical line offset VOFF8 to VOFF0 = 00Ah; horizontal pixel offset HOFF10 to HOFF0 = 354h, FOFF = 1, FISET = 1																
Line number (1st field)	519	520	521	522	523	524	525	1	2	3	4	5	6	7	8	9
	active video							equalization pulses			serration pulses			equalization pulses		
Line number (2nd field)	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272
	active video						equalization pulses			serration pulses			equalization pulses			
LCR (VOFF = 00Ah; HOFF = 354h; FOFF = 1; FISET = 1)	24								2	3	4	5	6	7	8	9

Table 12: Relationship of LCR to line numbers in 525 lines/60 Hz systems (part 2)

Vertical line offset VOFF8 to VOFF0 = 00Ah; horizontal pixel offset HOFF10 to HOFF0 = 354h, FOFF = 1, FISET = 1														
Line number (1st field)	10	11	12	13	14	15	16	17	18	19	20	21	22	23
	nominal VBI-lines F1												active video	
Line number (2nd field)	273	274	275	276	277	278	279	280	281	282	283	284	285	286
	nominal VBI-lines F2												active video	
LCR (VOFF = 00Ah; HOFF = 354h; FOFF = 1; FISET = 1)	10	11	12	13	14	15	16	17	18	19	20	21	22	23

Table 13: Relationship of LCR to line numbers in 625 lines/50 Hz systems (part 1)

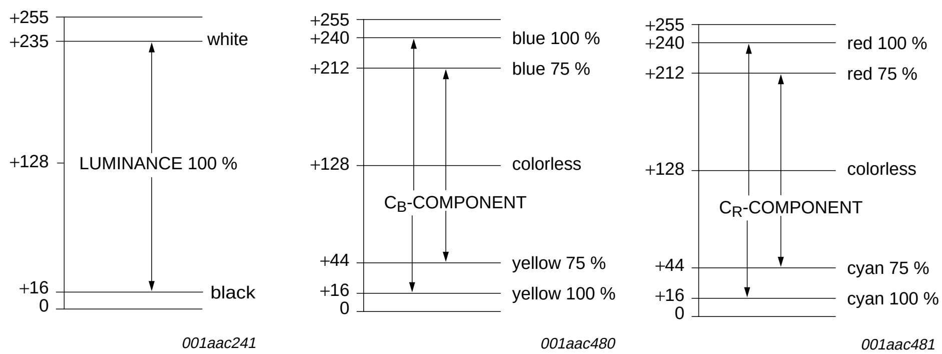
Vertical line offset VOFF8 to VOFF0 = 007h; horizontal pixel offset HOFF10 to HOFF0 = 354h, FOFF = 1, FISET = 0										
Line number (1st field)	621	622	623	624	625	1	2	3	4	5
	active video		equalization pulses			serration pulses		equalization pulses		
Line number (2nd field)	309	310	311	312	313	314	315	316	317	318
	active video		equalization pulses		serration pulses			equalization pulses		
LCR (VOFF = 007h; HOFF = 354h; FOFF = 1; FISET = 0)	24						2	3	4	5

Table 14: Relationship of LCR to line numbers in 625 lines/50 Hz systems (part 2)

Vertical line offset VOFF8 to VOFF0 = 007h; horizontal pixel offset HOFF10 to HOFF0 = 354h, FOFF = 1, FISET = 0																				
Line number (1st field)	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
	nominal VBI-lines F1																		active video	
Line number (2nd field)	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338
	nominal VBI-lines F2																	active video		
LCR (VOFF = 007h; HOFF = 354h; FOFF = 1; FISET = 0)	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	

Table 15: Location of related programming registers

Name	Subaddress bits
VOFF[8:0]	5Bh[4] and 5Ah[7:0]
HOFF[10:0]	5Bh[2:0] and 59h[7:0]
FOFF	5Bh[7]
FISET	40h[7]



Equations for modification to the Y-C_B-C_R levels via BCS control I²C-bus bytes BRIG, CONT and SATN.

Luminance:

$$Y_{OUT} = \mathrm{Int}\left[\frac{CONT}{71} \times (Y - 128)\right] + BRIG$$

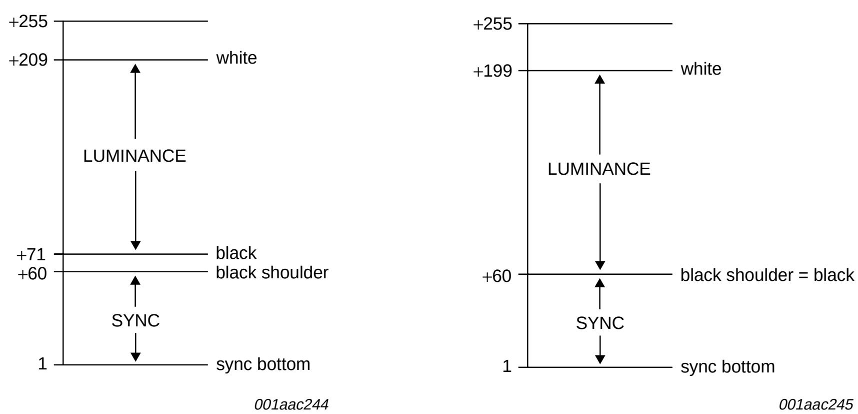
Chrominance:

$$UV_{OUT} = \mathrm{Int}\left[\frac{SATN}{64} \times (C_R, C_B - 128)\right] + 128$$

It should be noted that the resulting levels are limited to 1 to 254 in accordance with ITU-R BT 601/656 standard.

a. Y output range. b. C_B output range. c. C_R output range.

Fig 21. Y-C_B-C_R 4 : 2 : 2 levels on the 8-bit VPO-bus (data types 6 and 15).



VBI data levels are **not** dependent on BCS settings.

a. For sources containing 7.5 IRE black level offset (e.g. NTSC M). b. For sources not containing black level offset.

Fig 22. Raw data levels on the 8-bit VPO-bus (data type 8).

Table 16: Y-C_B-C_R data format on the 8-bit VPO-bus (data types 6 and 15)

Blanking period		Timing reference code				720 pixels Y-C_B-C_R 4 : 2 : 2 data									Timing reference code				Blanking period		
...	80	10	FF	00	00	SAV	C_B0	Y0	C_R0	Y1	C_B2	Y2	...	C_R718	Y719	FF	00	00	EAV	80	10	...

Table 17: Explanation to Table 16

Name	Explanation
SAV	start of active video range; see Table 8 to Table 10
C_Bn	U (B – Y) color difference component, pixel number n = 0, 2, 4 to 718
Yn	Y (luminance) component, pixel number n = 0, 1, 2, 3 to 719
C_Rn	V (R – Y) color difference component, pixel number n = 0, 2, 4 to 718
EAV	end of active video range; see Table 8 to Table 10

Table 18: Raw data format on the 8-bit VPO-bus (data type 8)

Blanking period			Timing reference code				Oversampled CVBS samples									Timing reference code				Blanking period		
...	80	10	FF	00	00	SAV	Y0	Y1	Y2	Y3	Y4	Y5	...	Yn – 1	Yn	FF	00	00	EAV	80	10	...

Table 19: Explanation to Table 18

Name	Explanation
SAV	start of raw sample range; see Table 8 to Table 10
Yi	oversampled raw sample stream (CVBS signal), n = 0, 1, 2, 3 to n; n is programmable via HSB and HSS; see Section 9.3.6 and Section 9.3.7
EAV	end of raw sample range; see Table 8 to Table 10

Table 20: Sliced data format on the 8-bit VPO-bus (data types 0 to 5 and 8 to 14)

Blanking period			Timing reference code				Internal header				Sliced data					Timing reference code				Blanking period		
...	80	10	FF	00	00	SAV	SDID	DC	IDI1	IDI2	DLN1	DHN1	...	DLNn	DHNn	FF	00	00	EAV	80	10	...

Table 21: Explanation to Table 20

Name	Explanation
SAV	start of active data; see Table 8 to Table 10
SDID	sliced data identification: NEP [1], EP [2], SDID5 to SDID0, freely programmable via I²C-bus subaddress 5Eh[5:0], e.g. to be used as source identifier
DC	Dword count: NEP [1], EP [2], DC5 to DC0; DC is inserted for software compatibility with old encoder devices, but does not represent any relevant information for SAA7144HL applications. DC describes the number of succeeding 32-bit words: DC = $\frac{1}{4}$(C + n), where C = 2 (the two data identification bytes IDI1 and IDI2) and n = number of decoded bytes according to the chosen text standard. As the sliced data are transmitted nibble wise, the maximum number of bytes transmitted (NBT) starting at IDI1 results to: NBS = (DC $\times$ 8) – 2 DC can vary between 1 and 11, depending on the selected data type. Note that the number of bytes actually transmitted can be less than NBT for two reasons: 1. result of DC would result to a non-integer value (DC is always rounded up) 2. standard not recognized (wrong standard or poor input signal)
IDI1	internal data identification 1: OP [3], FID (field 1 = 0, field 2 = 1), LineNumber8 to LineNumber3

Table 21: Explanation to Table 20 *...continued*

Name	Explanation
IDI2	internal data identification 2: OP [3], LineNumber2 to LineNumber0, DataType3 to DataType0; see Table 7
DLNn	sliced data LOW nibble, format: NEP [1], EP [2], bits 3 to 0, 1, 1
DLHn	sliced data HIGH nibble, format: NEP [1], EP [2], bits 7 to 4, 1, 1
EAV	end of active data; see Table 8 to Table 10

[1] Inverted EP (bit 7); for EP see Table note 2.

[2] Even parity (bit 6) of bits 5 to 0.

[3] Odd parity (bit 7) of bits 6 to 0.

9. I²C-bus description

9.1 I²C-bus format

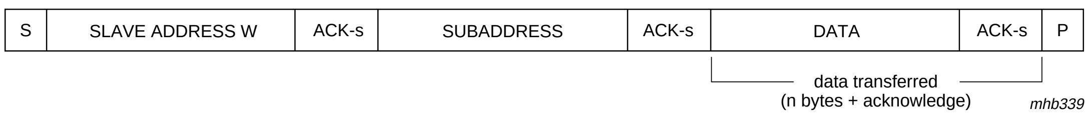


Fig 23. Write procedure.

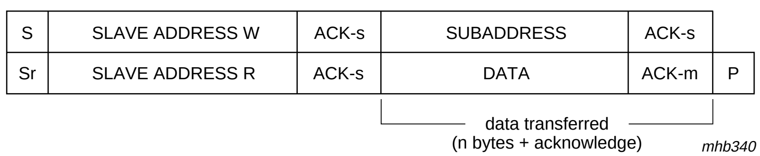


Fig 24. Read procedure (combined format).

Table 22: Description of I²C-bus format [1]

Code	Description
S	START condition
Sr	repeated START condition
Slave address W	0100 1010 (= 4Ah) for decoder cores B and D
	0100 1000 (= 48h) for decoder cores A and C
Slave address R	0100 1011 (= 4Bh) for decoder cores B and D
	0100 1001 (= 49h) for decoder cores A and C
ACK-s	acknowledge generated by the slave
ACK-m	acknowledge generated by the master
Subaddress	subaddress byte; see Table 24
Data	data byte; see Table 24 and Table note 2
P	STOP condition
X = LSB slave address	read/write control bit; X = 0, order to write (the circuit is slave receiver); X = 1, order to read (the circuit is slave transmitter)

[1] The SAA7144HL supports the fast mode I²C-bus specification extension (data rate up to 400 kbit/s).

[2] If more than one byte DATA is transmitted the subaddress pointer is automatically incremented.

9.2 I²C-bus register description

Table 23: Register subaddresses map

Subaddress	Description	Access	Reference
00h	chip version	read only	Section 9.3.1
01h to 04h	front-end part	read and write	Section 9.3.2 to Section 9.3.5
05h	reserved	-	-
06h to 11h	decoder part	read and write	Section 9.3.6 to Section 9.3.17
12h	reserved	-	-
13h	decoder part	read and write	Section 9.3.18
14h to 1Eh	reserved	-	-
1Fh	video decoder status byte	read only	Section 9.3.19
20h to 3Fh	reserved	-	-
40h to 5Bh	general purpose data slicer	read and write	Section 9.3.20 to Section 9.3.25
5Ch	for testability	-	-
5Dh	reserved	-	-
5Eh	sliced data identification code	read and write	Section 9.3.26
5Fh	reserved	-	-
60h to 62h	general purpose data slicer status	read only	Section 9.3.27 and Section 9.3.28
63h to FFh	reserved	-	-

Table 24: I²C-bus receiver/transmitter overview

Register function	Subaddress	7	6	5	4	3	2	1	0
Chip version (read only)	00h	ID07	ID06	ID05	ID04	-	-	-	-
Increment delay	01h	[1]	[1]	[1]	[1]	IDEL3	IDEL2	IDEL1	IDEL0
Analog control 1	02h	FUSE1	FUSE0	GUDL1	GUDL0	MODE3	MODE2	MODE1	MODE0
Analog control 2	03h	[1]	HLNRS	VBSL	WPOFF	HOLDG	GAFIX	[1]	GAI18
Analog control 3	04h	GAI17	GAI16	GAI15	GAI14	GAI13	GAI12	GAI11	GAI10
Reserved	05h	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Horizontal sync begin	06h	HSB7	HSB6	HSB5	HSB4	HSB3	HSB2	HSB1	HSB0
Horizontal sync stop	07h	HSS7	HSS6	HSS5	HSS4	HSS3	HSS2	HSS1	HSS0
Sync control	08h	AUFD	FSEL	FOET	HTC1	HTC0	HPLL	VNOI1	VNOI0
Luminance control	09h	BYPS	PREF	BPSS1	BPSS0	VBLB	UPTCV	APER1	APER0
Luminance brightness	0Ah	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0
Luminance contrast	0Bh	CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
Chrominance saturation	0Ch	SATN7	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0
Chrominance hue control	0Dh	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
Chrominance control	0Eh	[1]	CSTD2	CSTD1	CSTD0	DCCF	FCTC	CHBW1	CHBW0
Chrominance gain control	0Fh	ACGC	CGAIN6	CGAIN5	CGAIN4	CGAIN3	CGAIN2	CGAIN1	CGAIN0
Format/delay control	10h	OFTS1	OFTS0	HDEL1	HDEL0	VRLN	YDEL2	YDEL1	YDEL0
Output control 1	11h	[1]	[1]	[1]	[1]	OEYC	[1]	VIPB	COLO
Reserved	12h	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Output control 3	13h	ADLSB	[1]	[1]	OLDSB	[1]	[1]	[1]	[1]
Reserved	14h to 1Eh	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Decoder status byte (read only, OLDSB = 0)	1Fh	INTL	HLVLN	FIDT	GLIMT	GLIMB	WIPA	COPRO	RDCAP
Decoder status byte (read only, OLDSB = 1)	1Fh	INTL	HLCK	FIDT	GLIMT	GLIMB	WIPA	SLTCA	CODE
Reserved	20h to 3Fh	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Slicer control	40h	FISET	HAM_N	FCE	HUNT_N	[1]	CLKSEL1	CLKSEL0	[1]
Line control register 2	41h	LCR02_7	LCR02_6	LCR02_5	LCR02_4	LCR02_3	LCR02_2	LCR02_1	LCR02_0
Line control register 3 to 23	42h to 56h	LCRN_7	LCRN_6	LCRN_5	LCRN_4	LCRN_3	LCRN_2	LCRN_1	LCRN_0
Line control register 24	57h	LCR24_7	LCR24_6	LCR24_5	LCR24_4	LCR24_3	LCR24_2	LCR24_1	LCR24_0
Framing code	58h	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0

Table 24: I²C-bus receiver/transmitter overview *…continued*

Register function	Subaddress	7	6	5	4	3	2	1	0
Horizontal offset	59h	HOFF7	HOFF6	HOFF5	HOFF4	HOFF3	HOFF2	HOFF1	HOFF0
Vertical offset	5Ah	VOFF7	VOFF6	VOFF5	VOFF4	VOFF3	VOFF2	VOFF1	VOFF0
Horizontal offset (MSBs), vertical offset (MSB) and field offset	5Bh	FOFF	[1]	[1]	VOFF8	[1]	HOFF10	HOFF9	HOFF8
For testability	5Ch	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Reserved	5Dh	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Sliced data identification code	5Eh	[1]	[1]	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0
Reserved	5Fh	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Slicer status 1 (read only)	60h	-	FC8V	FC7V	VPSV	PPV	CCV	-	-
Slicer status 2 (read only)	61h	-	-	F21_N	LN8	LN7	LN6	LN5	LN4
Slicer status 3 (read only)	62h	LN3	LN2	LN1	LN0	DT3	DT2	DT1	DT0
Reserved	63h to FFh	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]

[1] All unused control bits must be programmed with logic 0 to ensure compatibility to future enhancements.

9.3 I²C-bus detail

The I²C-bus receiver slave address is 48h/49h and 4Ah/4Bh. Subaddresses 05h, 12h, 14h to 1Eh, 20h to 3Fh, 5Ch, 5Dh, 5Fh and 63h to FFh are reserved.

9.3.1 Subaddress 00h (read only register)

Table 25: Chip version

Function	Logic levels			
	ID07	ID06	ID05	ID04
Chip Version (CV)	CV3	CV2	CV1	CV0

9.3.2 Subaddress 01h

Table 26: Horizontal increment delay

Function	IDEL3	IDEL2	IDEL1	IDEL0
No update	1	1	1	1
Minimum delay	1	1	1	0
Recommended position	**1**	**0**	**0**	**0**
Maximum delay	0	0	0	0

The programming of the horizontal increment delay is used to match internal processing delays to the delay of the ADC. Use recommended position only.

9.3.3 Subaddress 02h

Table 27: Analog control 1 - bit description

Bit	Symbol	Description
7 and 6	FUSE[1:0]	analog function select; see Figure 6
		00 = amplifier plus anti-alias filter bypassed
		01 = amplifier plus anti-alias filter bypassed
		10 = amplifier active
		11 = amplifier plus anti-alias filter active
5 and 4	GUDL[1:0]	update hysteresis for 9-bit gain; see Figure 7
		00 = off
		01 = ±1 LSB
		10 = ±2 LSB
		11 = ±3 LSB
3 to 0	MODE[3:0]	channel input selector
		0000 = select CVBS (automatic gain) from AI11; see Figure 25
		0001 = select CVBS (automatic gain) from AI12; see Figure 25
		XXXX = reserved; see Table note 1

[1] X = don't care.

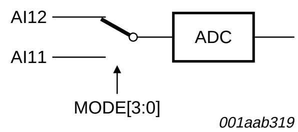


Fig 25. Mode switch for video inputs AI11 or AI12.

9.3.4 Subaddress 03h

Table 28: Analog control 2 - bit description

Bit	Symbol	Description
7	-	not used; has to be set to logic 0
6	HLNRS	HL not reference select
		0 = normal clamping if decoder is in unlocked state
		1 = reference select if decoder is in unlocked state
5	VBSL	AGC hold during vertical blanking period
		0 = short vertical blanking (AGC disabled during equalization and serration pulses)
		1 = long vertical blanking (AGC disabled from start of pre-equalization pulses until start of active video (line 22 for 60 Hz, line 24 for 50 Hz)
4	WPOFF	white peak off
		0 = white peak control active
		1 = white peak off
3	HOLDG	automatic gain control integration
		0 = AGC active
		1 = AGC integration hold (freeze)
2	GAFIX	gain control fix
		0 = automatic gain controlled by MODE[3:0]
		1 = gain is user programmable via GAI1
1	-	not used; has to be set to logic 0
0	GAI18	sign bit of gain control; see Table 29

9397 750 14454

9.3.5 Subaddress 04h

Table 29: Analog control 3; static gain control

Decimal value	Gain (dB)	Sign bit	Control bits 7 to 0							
		GAI18	GAI17	GAI16	GAI15	GAI14	GAI13	GAI12	GAI11	GAI10
0...	≈–3	0	0	0	0	0	0	0	0	0
...117...	≈0	0	0	1	1	1	0	1	0	1
...511	≈6	1	1	1	1	1	1	1	1	1

9.3.6 Subaddress 06h

Table 30: Horizontal sync begin

Delay time (step size = 8/LLC)	Control bits 7 to 0							
	HSB7	HSB6	HSB5	HSB4	HSB3	HSB2	HSB1	HSB0
–128...–109 (50 Hz)	forbidden (outside available central counter range)							
–128...–108 (60 Hz)								
–108 (50 Hz)...	1	0	0	1	0	1	0	0
–107 (60 Hz)...	1	0	0	1	0	1	0	1
...108 (50 Hz)	0	1	1	0	1	1	0	0
...107 (60 Hz)	0	1	1	0	1	0	1	1
109...127 (50 Hz)	forbidden (outside available central counter range)							
108...127 (60 Hz)								
Recommended value for raw data type; see Figure 22	**1**	**1**	**1**	**0**	**1**	**0**	**0**	**1**

9.3.7 Subaddress 07h

Table 31: Horizontal sync stop

Delay time (step size = 8/LLC)	Control bits 7 to 0							
	HSS7	HSS6	HSS5	HSS4	HSS3	HSS2	HSS1	HSS0
–128...–109 (50 Hz)	forbidden (outside available central counter range)							
–128...–108 (60 Hz)								
–108 (50 Hz)...	1	0	0	1	0	1	0	0
–107 (60 Hz)...	1	0	0	1	0	1	0	1
...108 (50 Hz)	0	1	1	0	1	1	0	0
...107 (60 Hz)	0	1	1	0	1	0	1	1
109...127 (50 Hz)	forbidden (outside available central counter range)							
108...127 (60 Hz)								
Recommended value for raw data type; see Figure 22	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**1**

9.3.8 Subaddress 08h

Table 32: Sync control - bit description

Bit	Symbol	Description
7	AUFD	automatic field detection
		0 = field state directly controlled via FSEL
		1 = automatic field detection
6	FSEL	field selection
		0 = 50 Hz, 625 lines
		1 = 60 Hz, 525 lines
5	FOET	forced ODD/EVEN toggle
		0 = ODD/EVEN signal toggles only with interlaced source
		1 = ODD/EVEN signal toggles fieldwise even if source is non-interlaced
4 and 3	HTC[1:0]	horizontal time constant selection
		00 = TV mode (recommended for poor quality TV signals only; do not use for new applications)
		01 = VTR mode (recommended if a deflection control circuit is directly connected to SAA7144HL)
		10 = reserved
		11 = fast locking mode (**recommended setting**)
2	HPLL	horizontal PLL
		0 = PLL closed
		1 = PLL open; horizontal frequency fixed
1 and 0	VNOI[1:0]	vertical noise reduction
		00 = normal mode (**recommended setting**)
		01 = fast mode [applicable for stable sources only; automatic field detection (AUFD) **must** be disabled]
		10 = free running mode
		11 = vertical noise reduction bypassed

9.3.9 Subaddress 09h

Table 33: Luminance control - bit description

Bit	Symbol	Description
7	BYPS	chrominance trap bypass
		0 = chrominance trap active; default for CVBS mode
		1 = chrominance trap bypassed
6	PREF	prefilter active; see Figure 11 to Figure 16
		0 = bypassed
		1 = active
5 and 4	BPSS[1:0]	aperture band-pass (center frequency)
		00 = center frequency is 4.1 MHz
		01 = center frequency is 3.8 MHz; see Table note 1
		10 = center frequency is 2.6 MHz; see Table note 1
		11 = center frequency is 2.9 MHz; see Table note 1

Table 33: Luminance control - bit description *...continued*

Bit	Symbol	Description
3	VBLB	vertical blanking luminance bypass
		0 = active luminance processing
		1 = chrominance trap and peaking stage are disabled during VBI lines determined by VREF = 0; see Table 41
2	UPTCV	update time interval for analog AGC value
		0 = horizontal update (once per line)
		1 = vertical update (once per field)
1 and 0	APER[1:0]	aperture factor; see Figure 11 to Figure 16
		00 = aperture factor is 0
		01 = aperture factor is 0.25
		10 = aperture factor is 0.5
		11 = aperture factor is 1.0

[1] Not to be used with bypassed chrominance trap.

9.3.10 Subaddress 0Ah

Table 34: Luminance brightness control

Offset	Control bits 7 to 0							
	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0
255 (bright)	1	1	1	1	1	1	1	1
128 (CCIR level)	1	0	0	0	0	0	0	0
0 (dark)	0	0	0	0	0	0	0	0

9.3.11 Subaddress 0Bh

Table 35: Luminance contrast control

Gain	Control bits 7 to 0							
	CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
1.999 (maximum)	0	1	1	1	1	1	1	1
1.109 (CCIR level)	0	1	0	0	0	1	1	1
1.0	0	1	0	0	0	0	0	0
0 (luminance off)	0	0	0	0	0	0	0	0
–1 (inverse luminance)	1	1	0	0	0	0	0	0
–2 (inverse luminance)	1	0	0	0	0	0	0	0

9.3.12 Subaddress 0Ch

Table 36: Chrominance saturation control

Gain	Control bits 7 to 0							
	SATN7	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0
1.999 (maximum)	0	1	1	1	1	1	1	1
1.0 (CCIR level)	0	1	0	0	0	0	0	0
0 (color off)	0	0	0	0	0	0	0	0
−1 (inverse chrominance)	1	1	0	0	0	0	0	0
−2 (inverse chrominance)	1	0	0	0	0	0	0	0

9.3.13 Subaddress 0Dh

Table 37: Chrominance hue control

Hue phase (deg)	Control bits 7 to 0							
	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
+178.6...	0	1	1	1	1	1	1	1
...0...	0	0	0	0	0	0	0	0
...−180	1	0	0	0	0	0	0	0

9.3.14 Subaddress 0Eh

Table 38: Chrominance control - bit description

Bit	Symbol	Description	
		50 Hz	60 Hz
7	-	not used; has to be set to logic 0	
6 to 4	CSTD[2:0]	color standard selection	
		000 = PAL BGHIN	NTSC M (or NTSC-Japan with special level adjustment: brightness subaddress 0Ah = 95h; contrast subaddress 0Bh = 48h)
		001 = NTSC 4.43 (50 Hz)	PAL 4.43 (60 Hz)
		010 = combination-PAL N	NTSC 4.43 (60 Hz)
		011 = NTSC N	PAL M
		100 = reserved; do not use	
		101 = SECAM	reserved
		110 = reserved; do not use	
		111 = reserved; do not use	
3	DCCF	disable chrominance comb filter	
		0 = chrominance comb filter on (during lines determined by VREF = 1; see Table 41)	
		1 = chrominance comb filter permanently off	
2	FCTC	fast color time constant	
		0 = nominal time constant	
		1 = fast time constant	

Table 38: Chrominance control - bit description *…continued*

Bit	Symbol	Description	
		50 Hz	60 Hz
1 and 0	CHBW[1:0]	chrominance bandwidth	
		00 = small bandwidth (≈ 620 kHz)	
		01 = nominal bandwidth (≈ 800 kHz)	
		10 = medium bandwidth (≈ 920 kHz)	
		11 = wide bandwidth (≈ 1000 kHz)	

9.3.15 Subaddress 0Fh

Table 39: Chrominance gain control - bit description

Bit	Symbol	Description
7	ACGC	automatic chrominance gain control
		0 = on
		1 = programmable gain via CGAIN[6:0]
6 to 0	CGAIN[6:0]	chrominance gain value (if AGC is set to logic 1)
		0000000 = minimum gain (0.5)
		0100100 = nominal gain (1.125)
		1111111 = maximum gain (7.5)

9.3.16 Subaddress 10h

Table 40: Format/delay control - bit description

Bit	Symbol	Description
7 and 6	OFTS[1:0]	output format selection; V-flag generation in SAV/EAV codes; see Table 9 and Table 10
		00 = standard ITU-R BT 656 format
		01 = V-flag in SAV/EAV is generated by VREF
		10 = V-flag in SAV/EAV is generated by data type
		11 = reserved
5 and 4	HDEL[1:0]	fine position of HS
		00 = 0 × 2/LLC
		01 = 1 × 2/LLC
		10 = 2 × 2/LLC
		11 = 3 × 2/LLC
3	VRLN	VREF pulse position and length; see Table 41
2 to 0	YDEL[2:0]	luminance delay compensation (steps in 2/LLC)
		100 = –4... × 2/LLC
		000 = ...0... × 2/LLC
		011 = ...3 × 2/LLC

Table 41: VREF pulse position and length VRLN SA 10 (bit 3)

VRLN	VREF at 60 Hz 525 lines				VREF at 50 Hz 625 lines			
	0		1		0		1	
Length	240		242		286		288	
Line number	first	last	first	last	first	last	first	last
Field 1 [1]	19 (22)	258 (261)	18 (21)	259 (262)	24	309	23	310
Field 2 [1]	282 (285)	521 (524)	281 (284)	522 (525)	337	622	336	623

[1] The numbers given in parenthesis refer to ITU line counting.

9.3.17 Subaddress 11h

Table 42: Output control 1 - bit description

Bit	Symbol	Description
7 to 4	-	not used; have to be set to logic 0
3	OEYC	output enable Y-C_B-C_R data
		0 = VPO-bus high-impedance
		1 = output VPO-bus active
2	-	not used; has to be set to logic 0
1	VIPB	Y-C_B-C_R decoder bypassed
		0 = processed data to VPO output
		1 = ADC data to VPO output; dependent on mode settings
0	COLO	color on
		0 = automatic color killer
		1 = color forced on

9.3.18 Subaddress 13h

Table 43: Output control 3 - bit description

Bit	Symbol	Description
7	ADLSB	analog-to-digital converter output bits on VPO7 to VPO0 in bypass mode (VIPB = 1, used for test purposes); see Table note 1
		0 = AD8 to AD1 (MSBs) on VPO7 to VPO0
		1 = AD7 to AD0 (LSBs) on VPO7 to VPO0
6 and 5	-	not used; have to be set to logic 0
4	OLDSB	selection bit for status byte functionality
		0 = default status information; see Table 44
		1 = old status information, for compatibility reasons; see Table 44
3 to 0	-	not used; have to be set to logic 0

[1] Video input selection via MODE[3:0] (subaddress 02h; see Figure 25).

9.3.19 Subaddress 1Fh (read only register)

Table 44: Status byte - bit description

Bit	Symbol	Description
7	INTL	status bit for interlace detection
		0 = non-interlaced
		1 = interlaced
6	HLCK	status bit for locked horizontal frequency (OLDSB = 1)
		0 = locked
		1 = unlocked
	HLVLN	status bit for horizontal/vertical loop (OLDSB = 0)
		0 = locked
		1 = unlocked
5	FIDT	identification bit for detected field frequency
		0 = 50 Hz
		1 = 60 Hz
4	GLIMT	gain value for active luminance channel is limited [max (top)]; active HIGH
3	GLIMB	gain value for active luminance channel is limited [min (bottom)]; active HIGH
2	WIPA	white peak loop is activated; active HIGH
1	SLTCA	slow time constant active in WIPA mode; active HIGH (OLDSB = 1)
	COPRO	Macrovision® copy protection detection according to *Macrovision® detect specification revision 7.01* (OLDSB = 0).
0	CODE	color signal in accordance with selected standard has been detected; active HIGH (OLDSB = 1)
	RDCAP	ready for capture (all internal loops locked); active HIGH (OLDSB = 0)

9.3.20 Subaddress 40h

Table 45: Slicer control - bit description

Bit	Symbol	Description
7	FISET	field size select
		0 = 50 Hz field rate
		1 = 60 Hz field rate
6	HAM_N	hamming check
		0 = **hamming check for 2 bytes after framing code, dependent on data type (default)**
		1 = no hamming check
5	FCE	framing code error
		0 = one framing code error allowed
		1 = no framing code errors allowed
4	HUNT_N	amplitude searching
		0 = **amplitude searching active (default)**
		1 = amplitude searching stopped
3	-	not used; has to be set to logic 0

Table 45: Slicer control - bit description *…continued*

Bit	Symbol	Description
2 and 1	CLKSEL[1:0]	data slicer clock selection
		00 = reserved
		01 = **13.5 MHz (default)**
		10 = reserved
		11 = reserved
0	-	not used; has to be set to logic 0

9.3.21 Subaddresses 41h to 57h

Table 46: LCR register 2 to 24; see Table 7

LCR register 2 to 24 (41h to 57h)		Framing code	Bit 7 to 4 DT3 to DT0 [1]	Bit 3 to 0 DT3 to DT0 [1]
WST625	teletext EuroWST, CCST	27h	0000	0000
CC625	European closed caption	001	0001	0001
VPS	video programming service	9951h	0010	0010
WSS	wide screen signalling bits	1E3C1Fh	0011	0011
WST525	US teletext (WST)	27h	0100	0100
CC525	US closed caption (line 21)	001	0101	0101
Test line	video component signal, VBI region	-	0110	0110
Intercast™	oversampled CVBS data	-	0111	0111
General text	teletext	programmable	1000	1000
VITC625	VITC/EBU time codes (Europe)	programmable	1001	1001
	VITC/SMPTE time codes (USA)	programmable	1010	1010
Reserved	reserved	-	1011	1011
NABTS	US NABTS	-	1100	1100
Japtext	MOJI (Japanese)	programmable (A7h)	1101	1101
JFS	Japanese format switch (L20/22)	programmable	1110	1110
Active video	**video component signal, active video region (default)**	-	1111	1111

[1] The assignment of the upper and lower nibbles to the corresponding field depends on the setting of FOFF (subaddress 5Bh, bit 7); see Table 47.

Table 47: Setting of FOFF (subaddress 5Bh, bit 7)

FOFF	Bit 7 to 4	Bit 3 to 0
0	field 1	field 2
1	field 2	field 1

9.3.22 Subaddress 58h

Table 48: Framing code - bit description

Bit	Symbol	Description
7 to 0	FC[7:0]	framing code for programmable data types; **40h (default)**

9.3.23 Subaddresses 59h and 5Bh

Table 49: Horizontal offset - bit description

Bit	Symbol	Description
Subaddress 5Bh		
2 to 0	HOFF[10:8]	horizontal offset; recommended value: 03h
Subaddress 59h		
7 to 0	HOFF[7:0]	horizontal offset; recommended value: 54h

9.3.24 Subaddresses 5Ah and 5Bh

Table 50: Vertical offset - bit description

Bit	Symbol	Description
Subaddress 5Bh		
4	VOFF8	vertical offset
Subaddress 5Ah		
7 to 0	VOFF[7:0]	vertical offset
		00h = minimum value 0, if VOFF8 = 0
		38h = maximum value 312, if VOFF8 = 1
		07h = value for 50 Hz 625 lines input, if VOFF8 = 0
		0Ah = value for 60 Hz 525 lines input, if VOFF8 = 0

9.3.25 Subaddress 5Bh

Table 51: Field offset, MSBs for vertical and horizontal offsets - bit description

Bit	Symbol	Description
7	FOFF	field offset
		0 = no modification of internal field indicator
		1 = **invert field indicator (even/odd; default)**
6 and 5	-	not used; have to be set to logic 0
4	VOFF8	vertical offset; see Table 50
3	-	not used; has to be set to logic 0
2 to 0	HOFF[10:8]	horizontal offset; see Table 49

9.3.26 Subaddress 5Eh

Table 52: Sliced data identification code - bit description

Bit	Symbol	Description
7 and 6	-	not used; have to be set to logic 0
5 to 0	SDID[5:0]	sliced data identification code; **SDID[5:0] = 000000 (default)**

9.3.27 Subaddress 60h (read only register)

Table 53: Slicer status 1 - bit description

Bit	Symbol	Description
7	-	not used; has to be set to logic 0
6 and 5	FC8V and FC7V	framing code valid
		00 = no framing code in the last frame
		01 = framing code with 1 error detected in the last frame
		1X [1] = framing code without errors detected in the last frame
4	VPSV	VPS valid
		0 = no VPS in the last frame
		1 = VPS detected
3	PPV	PALplus valid
		0 = no PALplus in the last frame
		1 = PALplus detected
2	CCV	closed caption valid
		0 = no closed caption in the last frame
		1 = closed caption detected
1 and 0	-	not used; have to be set to logic 0

[1] X = don’t care.

9.3.28 Subaddresses 61h and 62h (read only register)

Table 54: Slicer status 2 and 3 - bit description

Bit	Symbol	Description
Subaddress 61h		
7 and 6	-	not used; have to be set to logic 0
5	F21_N	internal used slicer status bit
4 to 0	LN[8:4]	line number
Subaddress 62h		
7 to 4	LN[3:0]	line number
3 to 0	DT[3:0]	data type according to Table 7

10. I²C-bus start set-up

The given values force the following behavior of the SAA7144HL:

- The analog input AI11 expects a signal in CVBS format; analog anti-alias filter and AGC active
- Automatic field detection enabled, PAL BDGHI or NTSC M standard expected
- Standard ITU-R BT 656 output format enabled, VBI data slicer disabled; see Table 55 Table note 2
- Contrast, brightness and saturation control in accordance with ITU standards
- Chrominance processing with nominal bandwidth (800 kHz).

Table 55: I²C-bus start set-up values

Subaddress (hexadecimal)	Function	Name [1]	Values (binary) 7	6	5	4	3	2	1	0	Start (hexadecimal)
00	chip version	ID07 to ID04	read only								
01	increment delay	X, X, X, X, IDEL[3:0]	0	0	0	0	1	0	0	0	08
02	analog control 1	FUSE[1:0], GUDL[1:0], MODE[3:0]	1	0	0	0	0	0	0	0	80
03	analog control 2	X, HLNRS, VBSL, WPOFF, HOLDG, GAFIX, X, GAI18	0	0	1	1	0	0	0	1	31
04	analog control 3	GAI1[7:0]	0	0	0	0	0	0	0	0	00
05	reserved		0	0	0	0	0	0	0	0	00
06	horizontal sync begin	HSB[7:0]	1	1	1	0	1	0	0	1	E9
07	horizontal sync stop	HSS[7:0]	0	0	0	0	1	1	0	1	0D
08	sync control	AUFD, FSEL, FOET, HTC[1:0], HPLL, VNOI[1:0]	1	0	0	1	1	0	0	0	98
09	luminance control	BYPS, PREF, BPSS[1:0], VBLB, UPTCV, APER[1:0]	0	0	0	0	0	0	0	1	01
0A	luminance brightness	BRIG[7:0]	1	0	0	0	0	0	0	0	80
0B	luminance contrast	CONT[7:0]	0	1	0	0	0	1	1	1	47
0C	chrominance saturation	SATN[7:0]	0	1	0	0	0	0	0	0	40
0D	chrominance hue control	HUEC[7:0]	0	0	0	0	0	0	0	0	00
0E	chrominance control	X, CSTD[2:0], DCCF, FCTC, CHBW[1:0]	0	0	0	0	0	0	0	1	01
0F	chrominance gain control	ACGC, CGAIN[6:0]	0	0	1	0	1	0	1	0	2A
10	format/delay control	OFTS[1:0], HDEL[1:0], VRLN, YDEL[2:0]	0	0	0	0	0	0	0	0	00
11	output control 1	X, X, X, X, OEYC, X, VIPB, COLO	0	0	0	0	1	0	0	0	0C
12	reserved		0	0	0	0	0	0	0	1	01
13	output control 3	ADLSB, X, X, OLDSB, X, X, X, X	0	0	0	0	0	0	0	0	00
14 to 1E	reserved		0	0	0	0	0	0	0	0	00
1F	decoder status byte	INTL, HLVLN, FIDT, GLIMT, GLIMB, WIPA, COPRO, RDCAP	read only								
20 to 3F	reserved		0	0	0	0	0	0	0	0	00
40	slicer control	FISET, HAM_N, FCE, HUNT_N, X, CLKSEL[1:0], X	0	0	0	0	0	0	1	0	02 [2]
41 to 57	line control register 2 to 24	LCRn[7:0]	1	1	1	1	1	1	1	1	FF [2]
58	programmable framing code	FC[7:0]	0	0	0	0	0	0	0	0	00
59	horizontal offset for slicer	HOFF[7:0]	0	1	0	1	0	1	0	0	54 [2]
5A	vertical offset for slicer	VOFF[7:0]	0	0	0	0	0	1	1	1	07 [2]
5B	field offset and MSBs for horizontal and vertical offset	FOFF, X, X, VOFF8, X, HOFF[10:8]	1	0	0	0	0	0	1	1	83 [2]
5C and 5D	reserved		0	0	0	0	0	0	0	0	00
5E	sliced data identification code	X, X, SDID[5:0]	0	0	0	0	0	0	0	0	00
5F	reserved		0	0	0	0	0	0	0	0	00

Table 55: I^2C-bus start set-up values *…continued*

Subaddress (hexadecimal)	Function	Name [1]	Values (binary)								Start (hexadecimal)
			7	6	5	4	3	2	1	0	
60	slicer status 1	-, FC8V, FC7V, VPSV, PPV, CCV, -, -	read only								
61	slicer status 2	-, -, F21_N, LN[8:4]	read only								
62	slicer status 3	LN[3:0], DT[3:0]	read only								
63 to FF	reserved		0	0	0	0	0	0	0	0	00

[1] All X values must be set to logic 0. For SECAM decoding set register 0Eh to 50h.

[2] For proper data slicer programming refer to Table 11 to Table 14 and Table 7.

11. Limiting values

Table 56: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All ground pins connected together and all supply pins connected together.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDD}	digital supply voltage			–0.5	+4.6	V
V_{DDA}	analog supply voltage			–0.5	+4.6	V
$V_{i(a)}$	analog input voltage			–0.5	V_{DDA} + 0.5 (4.6 max)	V
$V_{o(a)}$	analog output voltage			–0.5	V_{DDA} + 0.5	V
$V_{i(d)}$	digital input voltage	outputs in 3-state		–0.5	+5.5	V
$V_{o(d)}$	digital output voltage	outputs active		–0.5	V_{DDD} + 0.5	V
ΔV_{SS}	voltage difference between $V_{SSA(all)}$ and $V_{SS(all)}$			-	100	mV
T_{stg}	storage temperature			–65	+150	°C
T_{amb}	ambient temperature			0	70	°C
$T_{amb(bias)}$	ambient temperature under bias			–10	+80	°C
V_{esd}	electrostatic discharge voltage	human body model	[1]	-	±2000	V
		machine model	[2]	-	±200	V

[1] Class 2 according to JESD22-A114-B.

[2] Class B according to EIA/JESD22-A115-A.

12. Thermal characteristics

Table 57: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	30	K/W

13. Characteristics

Table 58: Characteristics

V_{DDD} = 3.0 V to 3.6 V; V_{DDA} = 3.1 V to 3.5 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
I_{DDD}	digital supply current (I_{DDDI} + I_{DDDE})	all outputs unloaded	-	125	165	mA
V_{DDA}	analog supply voltage		3.1	3.3	3.5	V
I_{DDA}	analog supply current (I_{DDA0} + I_{DDA1})		-	210	250	mA
P_{A+D}	analog and digital power		-	1.1	-	W
Analog part						
I_{clamp}	clamping current	V_I = 0.9 V DC	-	±8	-	µA

Table 58: Characteristics *...continued*

V_{DDD} = 3.0 V to 3.6 V; V_{DDA} = 3.1 V to 3.5 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(p-p)}$	input voltage (peak-to-peak value)	for normal video levels 1 V (p-p), termination 18/56 Ω and AC coupling required; coupling capacitor = 47 nF	0.5	0.7	1.4	V
$\lvert Z_i \rvert$	input impedance	clamping current off	200	-	-	kΩ
C_i	input capacitance		-	-	10	pF
α_{cs}	channel crosstalk between inputs of one instance AI11_x and AI12_x (e.g. AI11_A to AI12_A)	f_i = 5 MHz	-	-	–50	dB
$\alpha_{instance}$	crosstalk between two decoder instances	CVBS inputs with different line frequencies	-	–40	-	dB
9-bit analog-to-digital converter						
B	bandwidth	at –3 dB	-	7	-	MHz
ϕ_{diff}	differential phase (amplifier plus anti-alias filter bypassed)		-	2	-	deg
G_{diff}	differential gain (amplifier plus anti-alias filter bypassed)		-	2	-	%
$f_{clk(ADC)}$	ADC clock frequency		12.8	-	14.3	MHz
DLE	DC differential linearity error		-	0.7	-	LSB
ILE	DC integral linearity error		-	1	-	LSB
Digital inputs						
$V_{IL(SCL,SDA)}$	LOW-level input voltage pins SDA and SCL		–0.5	-	$+0.3V_{DDD}$	V
$V_{IH(SCL,SDA)}$	HIGH-level input voltage pins SDA and SCL		$0.7V_{DDD}$	-	V_{DDD} + 0.5	V
$V_{IL(n)}$	LOW-level input voltage all other inputs		–0.3	-	+0.8	V
$V_{IH(n)}$	HIGH-level input voltage all other inputs		2.0	-	5.5	V
I_{LI}	input leakage current		-	-	1	µA
$I_{LI/O}$	I/O leakage current		-	-	10	µA
C_i	input capacitance	outputs at 3-state	-	-	8	pF
$C_{i(n)}$	input capacitance all other inputs		-	-	5	pF
Digital outputs						
$V_{OL(SCL,SDA)}$	LOW-level output voltage pins SDA and SCL	SDA/SCL at 3 mA sink current	-	-	0.4	V
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	–0.5	-	+0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –2 mA	2.4	-	V_{DDD} + 0.5	V

Table 58: Characteristics *...continued*

V_{DDD} = 3.0 V to 3.6 V; V_{DDA} = 3.1 V to 3.5 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OL(clk)}$	LOW-level output voltage for LLC clock	I_{OL} = 2 mA	–0.5	-	+0.6	V
$V_{OH(clk)}$	HIGH-level output voltage for LLC clock	I_{OH} = –2 mA	2.4	-	V_{DDD} + 0.5	V
Data and control output timing; see Figure 26 [1]						
C_L	output load capacitance		15	-	40	pF
$t_{OHD;DAT}$	output hold time	C_L = 15 pF	4	-	-	ns
t_{PD}	propagation delay	C_L = 25 pF	-	-	22	ns
t_{PDZ}	propagation delay to 3-state		-	-	22	ns
Clock output timing (LLC); see Figure 26						
$C_{L(LLC)}$	output load capacitance		15	-	40	pF
T_{cy}	cycle time	LLC	35	-	39	ns
δ_{LLC}	duty factors for t_{LLCH}/t_{LLC}	C_L = 25 pF	40	-	60	%
t_r	rise time LLC		-	-	5	ns
t_f	fall time LLC		-	-	5	ns
Clock input timing (XTALI)						
δ_{XTALI}	duty factor for t_{XTALIH}/t_{XTALI}	nominal frequency	40	-	60	%
Horizontal PLL						
f_{Hn}	nominal line frequency	50 Hz field	-	15625	-	Hz
		60 Hz field	-	15734	-	Hz
$\Delta f_H/f_{Hn}$	permissible static deviation		-	-	5.7	%
Subcarrier PLL						
f_{SCn}	nominal subcarrier frequency	PAL BGHIN	-	4433619	-	Hz
		NTSC M; NTSC Japan	-	3579545	-	Hz
		PAL M	-	3575612	-	Hz
		combination-PAL N	-	3582056	-	Hz
Δf_{SC}	lock-in range		±400	-	-	Hz
Crystal oscillator						
f_n	nominal frequency	3rd harmonic	-	24.576	-	MHz
$\Delta f/f_n$	permissible nominal frequency deviation		-	-	±50	10^{-6}
$\Delta Tf/f_{n(T)}$	permissible nominal frequency deviation with temperature		-	-	±20	10^{-6}
Crystal specification (X1)						
$T_{amb(X1)}$	operating ambient temperature		0	-	70	°C
C_L	load capacitance		8	-	-	pF

Table 58: Characteristics *…continued*

V_{DDD} = 3.0 V to 3.6 V; V_{DDA} = 3.1 V to 3.5 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_s	series resonance resistor		-	40	80	Ω
C_1	motional capacitance		-	1.5 ± 20 %	-	fF
C_0	parallel capacitance		-	3.5 ± 20 %	-	pF

[1] The effects of rise and fall times are included in the calculation of $t_{OHD;DAT}$, t_{PD} and t_{PDZ}. Timings and levels refer to drawings and conditions illustrated in Figure 26.

Table 59: Processing delay

Function	Typical analog delay AI22 –> ADC(in) (ns)	Digital delay ADC(in) –> VPO (LLC CLOCKS); YDEL2 to YDEL0 = 0
Without amplifier or anti-alias filter	15	157
With amplifier, without anti-alias filter	25	
With amplifier and anti-alias filter	75	

14. Timing diagrams

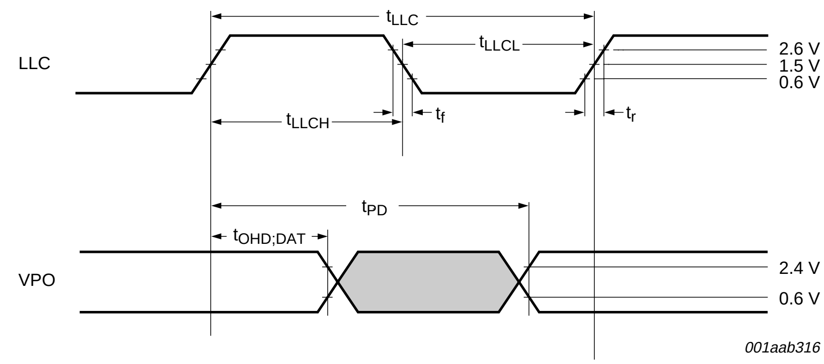
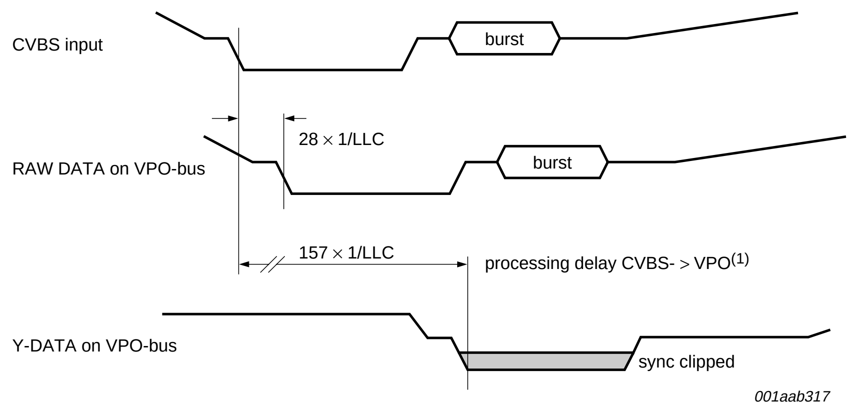


Fig 26. Clock/data output timing.



(1) See Table 59.

Fig 27. Horizontal timing diagram.

15. Application information

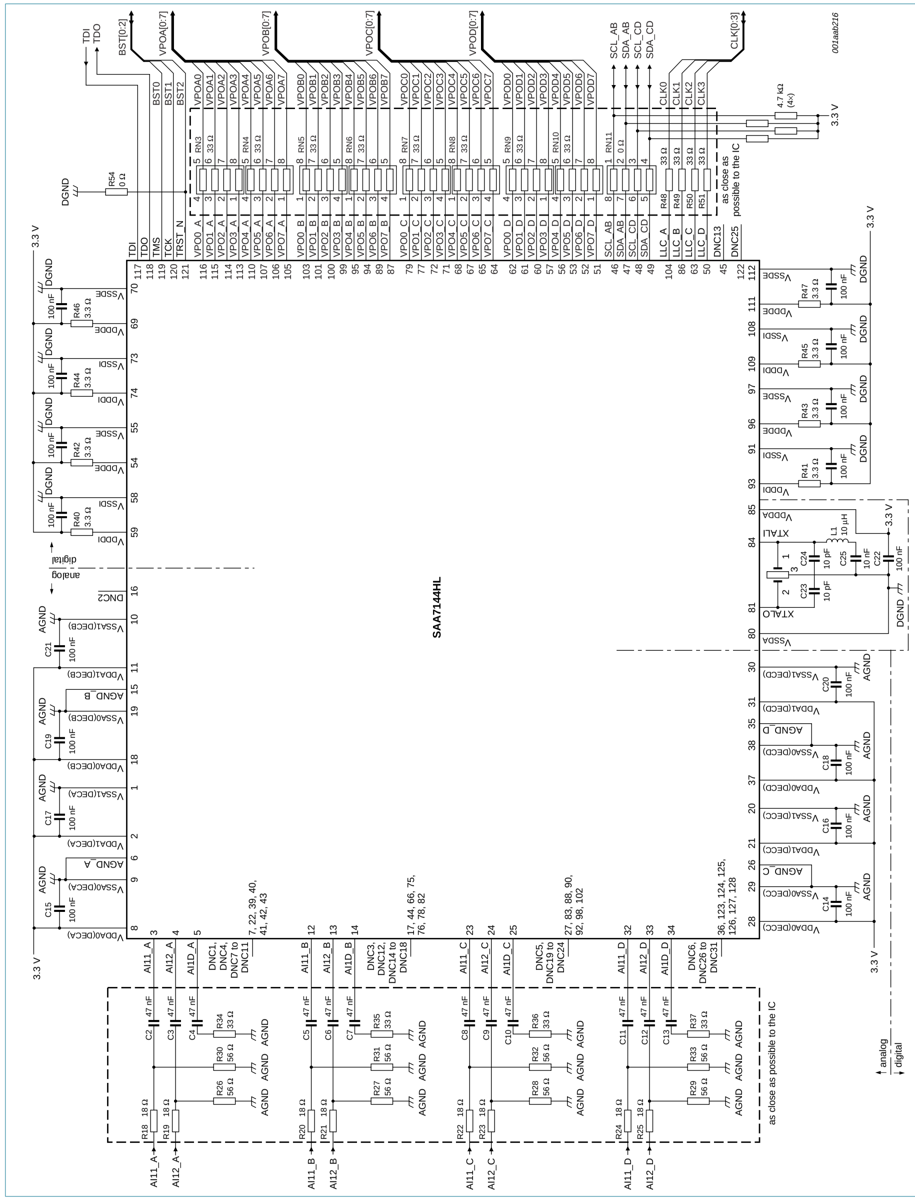


Fig 28. Application diagram of SAA7144HL.

15.1 Recommended printed-circuit board layout

The SAA7144HL consists of analog and digital areas. Due to this special care needs to be taken for design of layout regarding crosstalk by analog and digital supply interaction.

It is recommended to use four layer Printed-Circuit Board (PCB). Top and bottom layer for signal wires, one for ground plane and one for supply plane. Split of analog and digital supply layer areas shows best video performance.

The ground and supply plane need to be close to each other to achieve capacitive behavior. Due to this size, distance and also material is responsible for layer capacitor value. Additional decoupling isles are required.

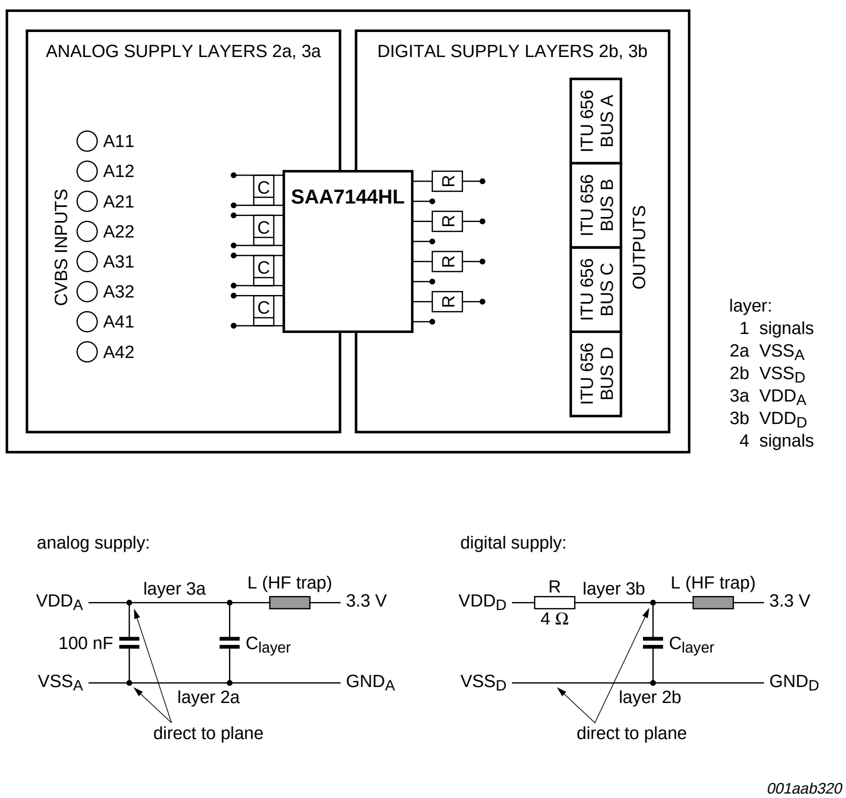


Fig 29. Supply method.

16. Test information

16.1 Boundary scan test

The SAA7144HL has built-in logic and five dedicated pins to support boundary scan testing which allows board testing without special hardware (nails). The SAA7144HL follows the *“IEEE Std. 1149.1 - Standard Test Access Port and Boundary - Scan Architecture”* set by the Joint Test Action Group (JTAG) chaired by Philips.

The 5 special pins are: Test Mode Select (TMS), Test Clock (TCK), Test Reset (TRST_N), Test Data Input (TDI) and Test Data Output (TDO).

The Boundary Scan Test (BST) functions BYPASS, EXTEST, INTEST, SAMPLE, CLAMP and IDCODE are all supported (see Table 60). Details about the JTAG BST-test can be found in the specification *“IEEE Std. 1149.1”*.

Table 60: BST instructions supported by the SAA7144HL

Instruction	Description
BYPASS	This mandatory instruction provides a minimum length serial path (1 bit) between pins TDI and TDO when no test operation of the component is required.
EXTEST	This mandatory instruction allows testing of off-chip circuitry and board level interconnections.
INTEST	This optional instruction allows testing of the internal logic (no support for customers available).
SAMPLE	This mandatory instruction can be used to take a sample of the inputs during normal operation of the component. It can also be used to preload data values into the latched outputs of the boundary scan register.
CLAMP	This optional instruction is useful for testing when not all ICs have BST. This instruction addresses the bypass register while the boundary scan register is in external test mode.
IDCODE	This optional instruction will provide information on the components manufacturer, part number and version number.

16.1.1 Initialization of boundary scan circuit

The Test Access Port (TAP) controller of an IC should be in the reset state (TEST_LOGIC_RESET) when the IC is in the functional mode. This reset state also forces the instruction register into a functional instruction such as IDCODE or BYPASS.

To solve the power-up reset, the standard specifies that the TAP controller will be forced asynchronously to the TEST_LOGIC_RESET state by setting the TRST_N pin LOW.

16.1.2 Device identification codes

A device identification register is specified in *"IEEE Std. 1149.1b-1994"*. It is a 32-bit register which contains fields for the specification of the IC manufacturer, the IC part number and the IC version number. Its biggest advantage is the possibility to check for the correct ICs mounted after production and determination of the version number of ICs during field service.

When the IDCODE instruction is loaded into the BST instruction register, the identification register will be connected internally between pins TDI and TDO of the IC. The identification register will load a component specific code during the CAPTURE_DATA_REGISTER state of the TAP controller and this code can subsequently be shifted out. At board level, this code can be used to verify component manufacturer, type and version number. The device identification register contains 32 bits, numbered 31 to 0, where bit 31 is the most significant bit (nearest to TDI) and bit 0 is the least significant bit (nearest to TDO); see Figure 30.

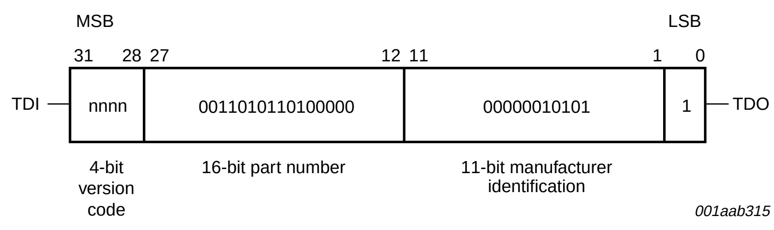
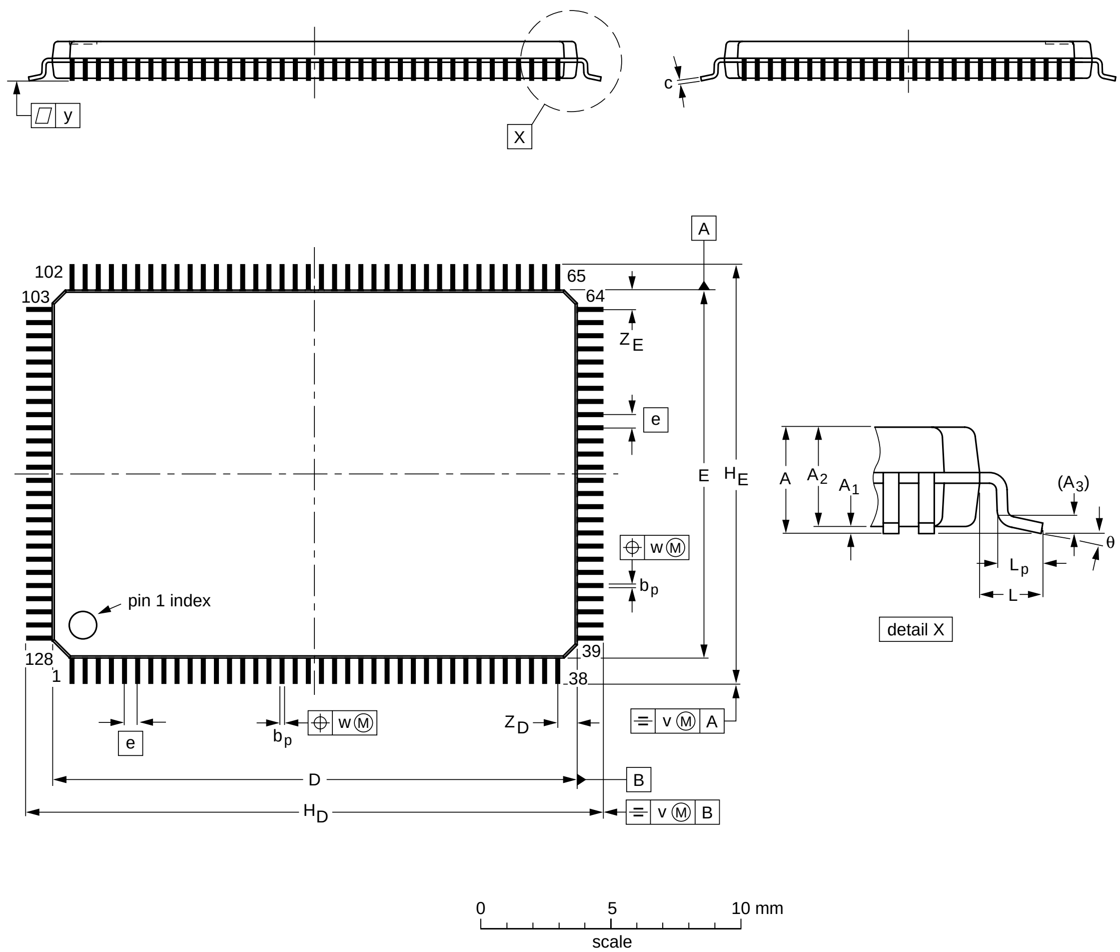


Fig 30. 32 bits of identification code.

17. Package outline

LQFP128: plastic low profile quad flat package; 128 leads; body 14 x 20 x 1.4 mm **SOT425-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	14.1 13.9	0.5	22.15 21.85	16.15 15.85	1	0.75 0.45	0.2	0.12	0.1	0.81 0.59	0.81 0.59	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT425-1	136E28	MS-026				~~00-01-19~~ 03-02-20

Fig 31. Package outline SOT425-1 (LQFP128).

18. Soldering

18.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

18.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

18.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

18.5 Package related soldering information

Table 61: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

19. Revision history

Table 62: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
SAA7144HL_1	20050421	Product data sheet	-	9397 750 14454	-

20. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

21. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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25. Contents

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