# ST-NXP Wireless

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ST-NXP Wireless

# STn8810S12

## STn8810 mobile multimedia application processor with 1-Gbit NAND-Flash and 512-Mbit DDR mobile RAM

Data Brief

*Nomadik is a registered trademark of STMicroelectronics*

## Features

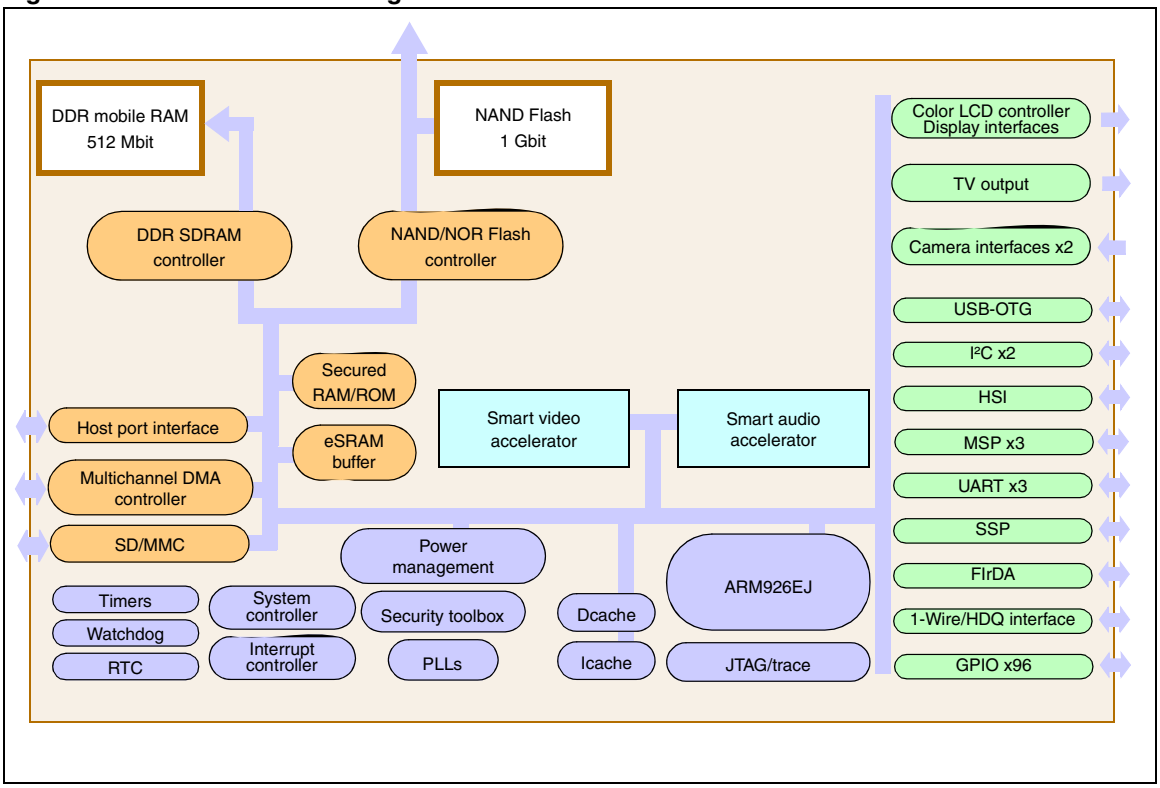
- Unique combination of SOC and memories in a single package
- Complete and memory-autonomous application system
  - STn8810 multimedia application processor
  - 1-Gbit NAND Flash
  - 512-Mbit DDR mobile RAM
- Important area saving and PCB simplification: complete system in 388 (288 + 36 + 64) balls LFGBA 14 mm x 14 mm x 1.4 mm
- Ultra low-power solution

## Description

The STn8810S12 is a culmination of breakthroughs in video coding efficiency, inventive algorithms, chip implementation schemes and enhanced packaging techniques.

The STn8810S12 system-in-package enables multimedia mobile phones and multimedia portable consumer applications.

**Figure 1. Functional block diagram**



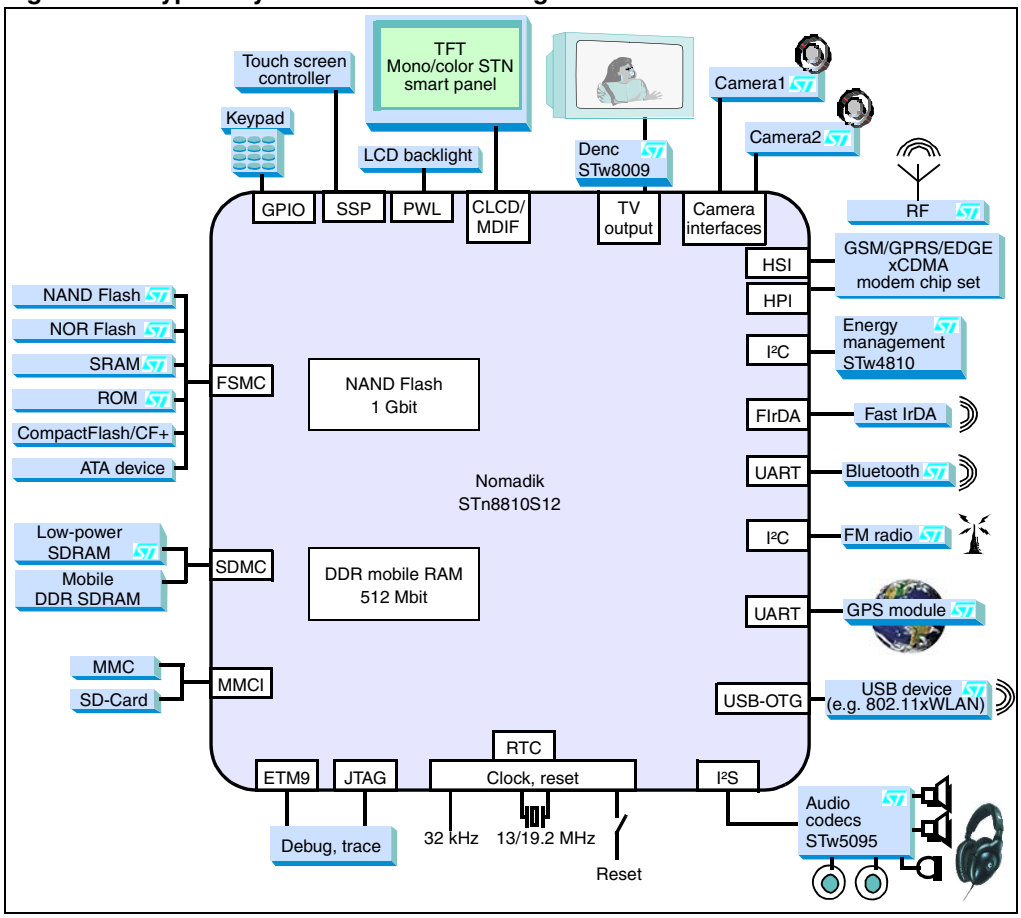
# Contents

# 1 STn8810S12 general description

The STn8810S12 system from STMicroelectronics is a culmination of breakthroughs in video coding efficiency, inventive algorithms, chip implementation schemes and enhanced packaging techniques. The processor and memory package enables multimedia mobile phones and multimedia portable consumer applications.

The STn8810S12 focuses on the essential features of mobile products and services: a high-performance multimedia capability coupled with low power consumption, based on an open platform strategy.

**Figure 2. Typical system architecture using the STn8810S12**



## 1.1 Key benefits

The STn8810S12 brings the following key benefits to mobile manufacturers and consumers:

- Unsurpassed audio and video quality,
- Ultra-low power consumption for longer battery operation,
- Easier application development for shorter time-to-market,
- Scalability for multiple market segments and future multimedia applications,
- Ultra-integrated system package.

## 1.2 Main features

The STn8810S12 system-in-package enables compelling multimedia applications by means of its unique distributed-processing architecture. The application processor features low-power smart accelerators which handle all audio and video functions. These free the main CPU for control and program flow tasks, or allow the CPU to enter power-saving modes to prolong battery life. The smart accelerators operate independently and concurrently to ensure the lowest absolute system power and deterministic high-performance. The STn8810S12 incorporates additional memory in a much reduced area using advanced packaging processes.

The main features of the system are:

- A smart video accelerator for VGA video encoding and decoding, with camera interfaces,
- A smart audio accelerator containing a comprehensive set of digital audio decoders and encoders, and offering a large number of 3-D surround effects,
- A power management unit which offers a number of power saving modes,
- The ARM926EJ processor, a powerful industry-standard CPU,
- Self-contained memory resources:
  - Processor on-chip ROM and SRAM memory devices,
  - 1-Gbit NAND Flash memory,
  - 512-Mbit DDR mobile RAM.
- Advanced security framework for authentication and digital rights management,
- Multichannel DMA controller for efficient data transfer without CPU intervention,
- A multi-layer AMBA crossbar interconnect for optimized data transfers between the CPU, accelerators, memory devices and peripherals,
- A wide range of peripheral interfaces (GPIO, USB-OTG, UART, I²C, FIrDA, SD/MMC, serial ports, color LCD and camera interfaces),
- Minimal support for high-level operating system such as Symbian™, Linux and WinCE® operating systems.

## 1.3 Low power consumption

The new multimedia functionality of mobile products brings with it an increase in power consumption that is outpacing advances in battery technology. The STn8810S12 saves on power by avoiding the need for high clock speeds wherever possible, but its extremely low power consumption results from a systematic effort at all design levels to reduce power requirements. These include:

- The use of smart accelerators and distributed processing to off load from the CPU,
- Efficient code execution by means of innovative algorithms, energy-efficient instruction set architectures and Java acceleration,
- The efficient use of bandwidth for on-chip data transport, achieved by data compression, buffering and image scaling,
- Aggressive power management which includes turning off inactive parts of the chip and keeping the CPU in power-saving modes as much as possible,
- Low-power SDRAM.

## 1.4 Open platform strategy

The STn8810S12 is based around the MIPI™ software and hardware interface standard. This open platform strategy provides manufacturers with roadmap flexibility, allowing them to avoid becoming locked into a proprietary CPU architecture or vendor technology. This approach is facilitated by the following design points.

- The STn8810S12 employs the third-party ARM® processor which is the standard CPU for mobile devices, with industry-wide application support.
- Open, standard APIs are provided for the development of application code on a level which is abstracted from the physical hardware. This allows the development of multimedia plug-ins that are portable between products and which can be reused on future products without modification.
- The STn8810S12 offers a rich set of peripherals and the capability of adding new smart accelerators when required.
- The STn8810S12 enables best-in-class algorithm development on its smart accelerators.

## 1.5 STn8810 processor features

- Smart video accelerator
  - Real-time MPEG4 or H.263 encoding or decoding, up to VGA 30 fps
  - H.264 encode/decode support
  - JPEG encode or decode, up to 4080 x 4080 pixels
  - Ultra low-power implementation
- Smart audio accelerator
  - Extensive digital-audio software library
  - Ultra low-power implementation
- WM9/VC-1 encode/decode support
- Camera interfaces
  - Supports high-resolution sensors up to 4 Megapixels
  - Serial interface up to 416 Mbit/s (MIPI legacy CSI)
  - Parallel camera CCIR-656 interface up to 66 MHz (MIPI legacy CPI)
- TV output
- Advanced power management unit
  - Run, idle, doze and sleep modes
  - CPU clock with programmable frequency
  - Embedded 1.2 V logic supply switch
- ARM926EJ 32-bit RISC CPU, at 264 MHz
  - 32-Kbyte instruction cache, 16-Kbyte data cache
  - 3 instruction sets: 32-bit for high performance, 16-bit (Thumb) for efficient code density, byte Java mode (Jazelle™) for direct execution of Java code
  - Embedded medium trace module (ETM Medium+)
- On-chip SRAM: 40 Kbytes + 16 Kbytes with secured access + 1 Kbyte backup
- On-chip ROM: 32 Kbytes for boot + 64 Kbytes with secured access
- Advanced security
  - Comprehensive security framework
  - Protected access to secured ROM and RAM
- 16-bit DDR/SDR-SDRAM memory controller
- NOR Flash/NAND Flash/CompactFlash/CF+ controller
- MultiMediaCard/SD Card host controller
- Color LCD controller for STN or TFT panels or display interface for display module
  - 24-bpp true color
  - MIPI legacy DBI and DPI
- USB On-The-Go interface up to 12 Mbit/s
- Host port interface

- I/O peripherals
  - 3 autobaud UARTs (one with modem control signals) up to 3.692 Mbit/s
  - One IrDA (SIR/MIR/FIR) interface up to 4 Mbit/s
  - One synchronous serial port (SSP) up to 24 Mbit/s
  - 3 multichannel serial ports (MSP) up to 48 Mbit/s
  - Two I²C multi-master/slave interfaces
  - One 8-channel, full-duplex high-speed serial interface, 108 Mbit/s
  - 1-Wire®/HDQ interface [a]
- 96 general-purpose I/Os (muxed with peripheral I/Os)
- System and peripheral controller
  - Multichannel DMA controller
  - 32-source interrupt controller
  - Eight 32-bit timers/counters
  - Real-time clock (RTC)
  - Real-time timer (RTT)
  - Watchdog timer
- Programmable PLL for CPU and system clocks
- 13/19.2 MHz crystal oscillator
- JTAG IEEE 1149.1 boundary scan
- Supply voltages
  - 1.2 V logic; 1.8 V to 2.5 V I/O, PLL analog; 2.5 V OTP

a.1-Wire is a registered trademark of Dallas Semiconductor

## 1.6 Additional memory devices

### 1.6.1 1-Gbit NAND Flash memory features

- NAND interface
  - x16 bus width
  - Multiplexed address/data
  - Pinout compatibility for all densities
- Page size
  - (1 K + 32 spare) words
- Block size
  - (64 K + 2 K spare) words
- Page read/program
  - Random access: 12 µs (max)
  - Sequential access: 50 ns (min)
  - Page program time: 200 µs (typ)
- Copy back program mode
  - Fast page copy without external buffering
- Fast block erase
  - Block erase time: 2 ms (typ)
- Status register
- Data integrity
  - 100,000 program/erase cycles
  - 10 years data retention

### 1.6.2 512-Mbit DDR mobile RAM features

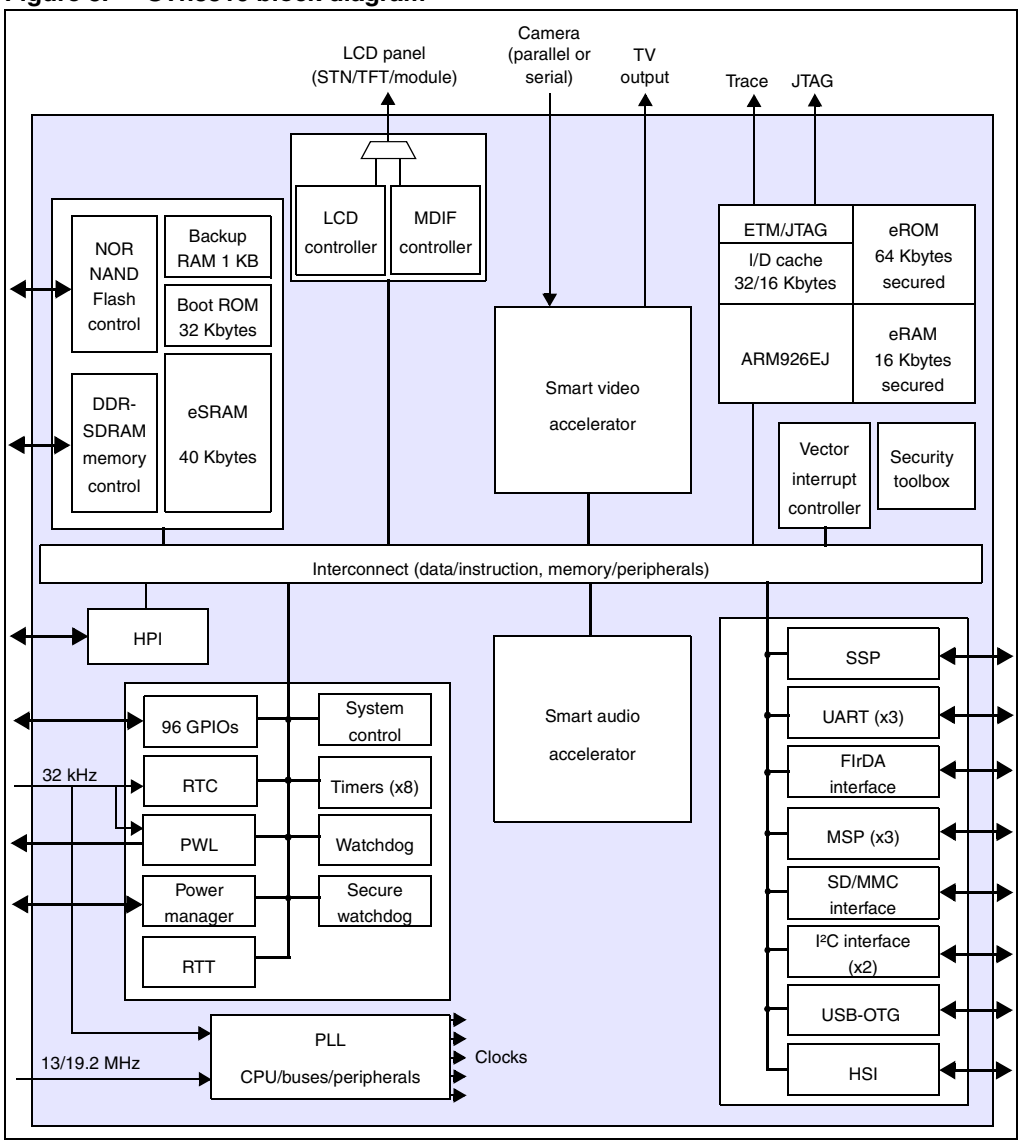
- Programmable partial array self refresh
- Programmable driver strength
- Auto temperature compensated self refresh by built-in temperature sensor
- Deep power down mode
- Data rate: 266 Mbit/s/IO (max)
- 16-bit data bus
- Double data rate architecture: two data transfers per clock cycle
- Bi-directional, data strobe (DQS) is transmitted/received with data, used in capturing data at the receiver
- Command and address signals refer to a positive clock edge
- Quad internal banks controlled by BA0 and BA1
- Data mask (DM) for write data
- Wrap sequence: sequential/ interleave
- Programmable burst length (BL): 2, 4, 8
- Automatic precharge and controlled precharge
- Auto refresh and self refresh
- 8,192 refresh cycles/64 ms (7.8 µs maximum average periodic refresh interval)
- Burst termination by burst stop command and precharge command

# 2 STn8810 architecture overview

The STn8810 platform comprises an industry-standard ARM CPU supported by smart audio and video accelerators, on-chip memory and controllers, a rich set of peripheral interfaces, and a power management system. The processors, controllers, memory and peripheral interfaces are connected by a multi-layer advanced microcontroller bus architecture (AMBA) for efficient data transport between the components.

The overall STn8810 architecture is illustrated in *Figure 3*.

**Figure 3. STn8810 block diagram**

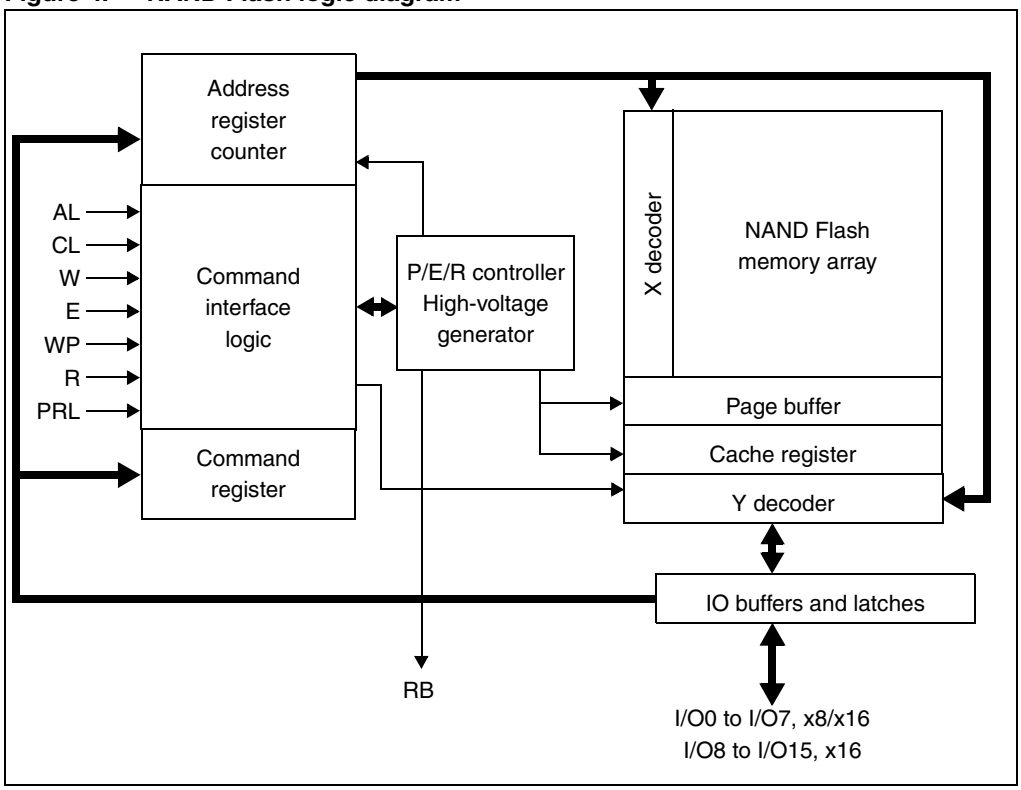


# 3 Additional memory devices

## 3.1 NAND Flash device

The STn8810S12 contains a 1-Gbit NAND Flash memory (large page). For detailed information on how to use the devices, see the NAND01G-B datasheet which is available from the Internet site *http:// www.st.com* or from your local STMicroelectronics distributor.

**Figure 4. NAND Flash logic diagram**



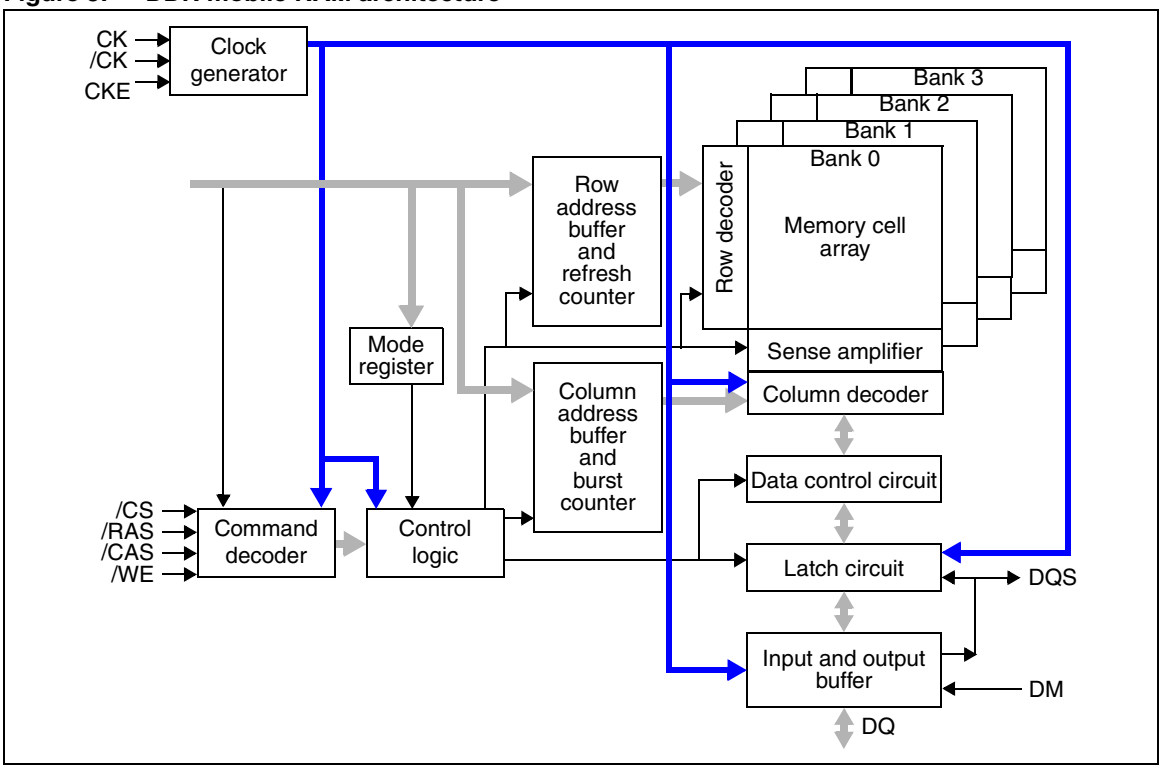
## 3.2 DDR mobile RAM device

The 512-Mbit DDR mobile RAM is organized as 8,388,608 × 16 bits × 4 banks. It achieves low power consumption and high-speed data transfer using a 2-bit prefetch pipeline architecture.

Command and address inputs are synchronized with the positive edge of the clock. Data inputs and outputs are synchronized with both edges of DQS (data strobe). DLL is not implemented.

The device architecture is illustrated in *Figure 5*.

**Figure 5. DDR mobile RAM architecture**




## 3.3 External memory support

- One chip-select available for external NAND Flash connection.

# 4 Package mechanical data

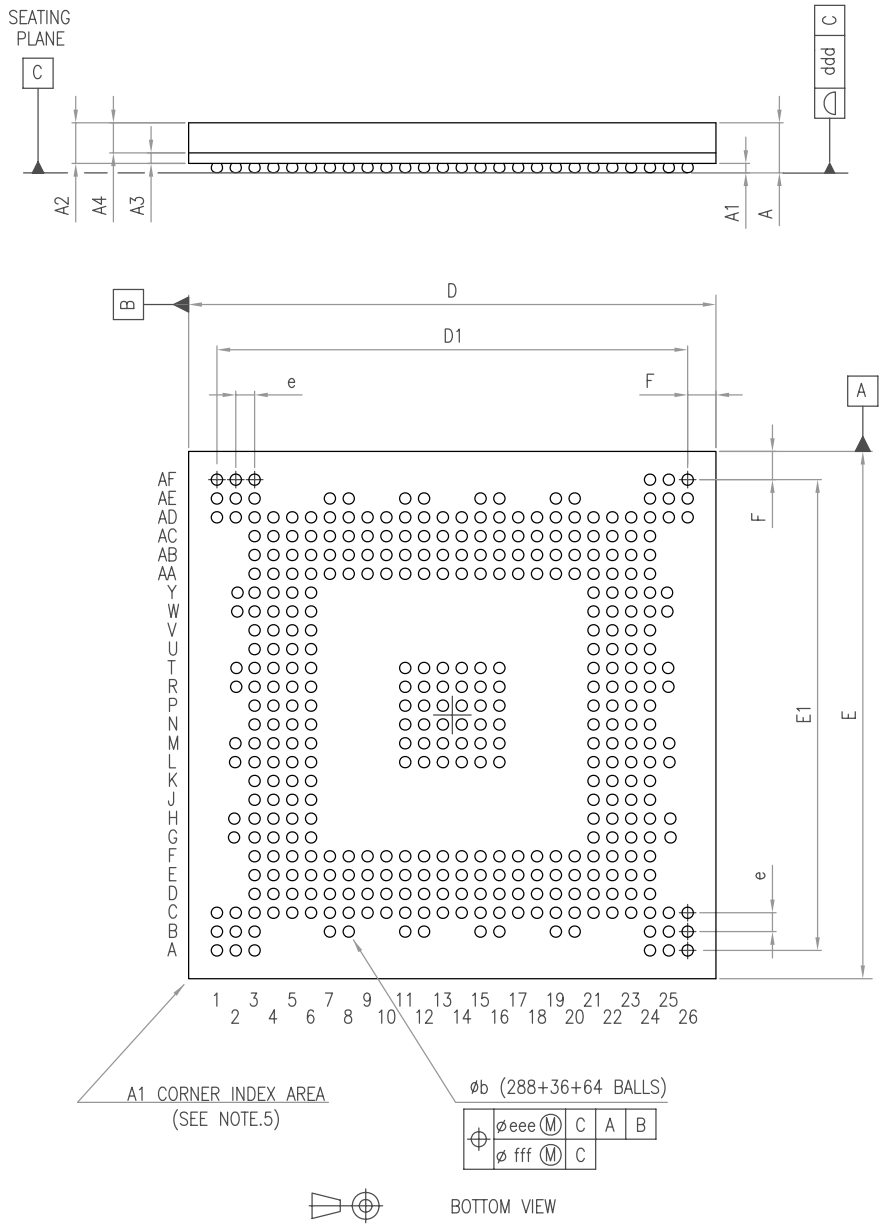
In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

**Table 1. Package dimensions**

| | Databook (mm) | | | Drawing (mm) | | |
|---|---|---|---|---|---|---|
| **Ref.** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** |
| A (1) | | | 1.40 | | | 1.34 |
| A1 | 0.15 | | | 0.16 | 0.21 | 0.26 |
| A2 | | 1.08 | | 1.01 | 1.065 | 1.12 |
| A3 | | 0.28 | | 0.24 | 0.28 | 0.32 |
| A4 | | | 0.80 | 0.77 | 0.785 | 0.80 |
| b (2) | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 |
| D | 13.85 | 14.00 | 14.15 | 13.90 | 14.00 | 14.10 |
| D1 | | 12.50 | | | 12.50 | |
| E | 13.85 | 14.00 | 14.15 | 13.90 | 14.00 | 14.10 |
| E1 | | 12.50 | | | 12.50 | |
| e | | 0.50 | | | 0.50 | |
| F | | 0.75 | | | 0.75 | |
| ddd | | | 0.08 | | | 0.10 |
| eee (3) | | | 0.15 | | | 0.15 |
| fff (4) | | | 0.05 | | | 0.05 |

1. LFBGA stands for low profile fine pitch ball grid array.
   - Thin profile: The total profile height (Dim A) is measured from the seating plane to the top of the component.
   - Low profile 1.20 <= A < 1.70 mm
   - Fine pitch: e < 1.00mm pitch.
2. The typical ball diameter before mounting is 0.30mm.
3. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
4. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

**Figure 6. LFBGA 14 x 14 x 1.4 mm - 288 + 36 +64 - pitch 0.5 package outline**




*Note: The terminal A1 corner is identified on the top surface by using a corner chamfer, ink or metallized markings.*

# 5 Ordering information

**Table 2. Ordering information**

| Order code | Package | Packing |
|---|---|---|
| STN8810BDS12HPBE | TFBGA 12x12x1.2 288+36 4R22 0.5 | Tray |

# 6 Revision history

**Table 3. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 19-Jan-2007 | 1 | Initial release. |
| 08-Feb-2008 | 2 | Removed all references to SDIO card. |

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