

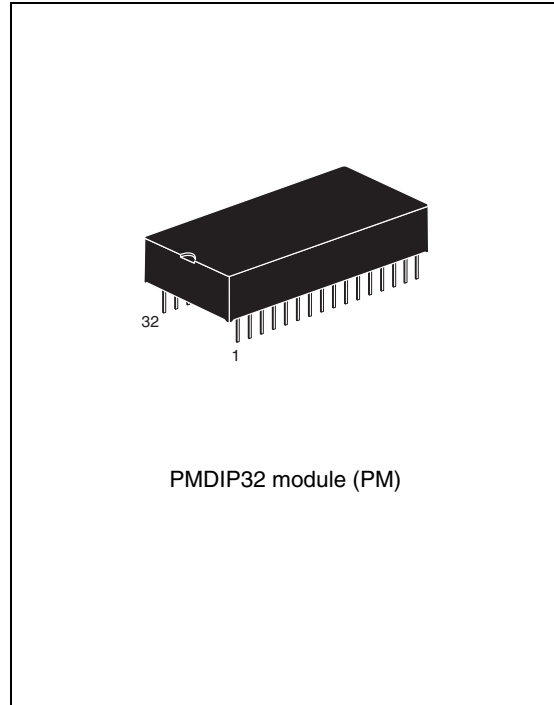


M48Z128 M48Z128Y, M48Z128V

5.0 V or 3.3 V, 1 Mbit (128 Kbit x 8) ZEROPOWER[®] SRAM

Features

- Integrated, ultra low power SRAM, power-fail control circuit, and battery
- Conventional SRAM operation; unlimited WRITE cycles
- 10 years of data retention in the absence of power
- Battery internally isolated until power is first applied
- Automatic power-fail chip deselect and WRITE protection
- WRITE protect voltages:
(V_{PFD} = power-fail deselect voltage)
 - M48Z128: $V_{CC} = 4.75$ to 5.5 V
 4.5 V $\leq V_{PFD} \leq 4.75$ V
 - M48Z128Y: $V_{CC} = 4.5$ to 5.5 V
 4.2 V $\leq V_{PFD} \leq 4.5$ V
 - M48Z128V: $V_{CC} = 3.0$ to 3.6 V
 2.8 V $\leq V_{PFD} \leq 3.0$ V
(contact ST sales office for availability)
- Pin and function compatible with JEDEC standard 128 K x 8 SRAMs
- RoHS compliant
 - Lead-free second level interconnect



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1 Description

The M48Z128/Y/V ZEROPOWER[®] RAM is a 128 Kbit x 8 non-volatile static RAM organized as 131,072 words by 8 bits. The device combines an internal lithium battery, a CMOS SRAM and a control circuit in a plastic, 32-pin DIP module to provide a highly integrated battery-backed memory solution.

The M48Z128/Y/V is a non-volatile pin and function equivalent to any JEDEC standard 128 K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special WRITE timing or limitations on the number of WRITES that can be performed. The 32-pin, 600 mil DIP module houses the M48Z128/Y/V silicon with a long-life lithium button cell in a single package.

Figure 1. Logic diagram

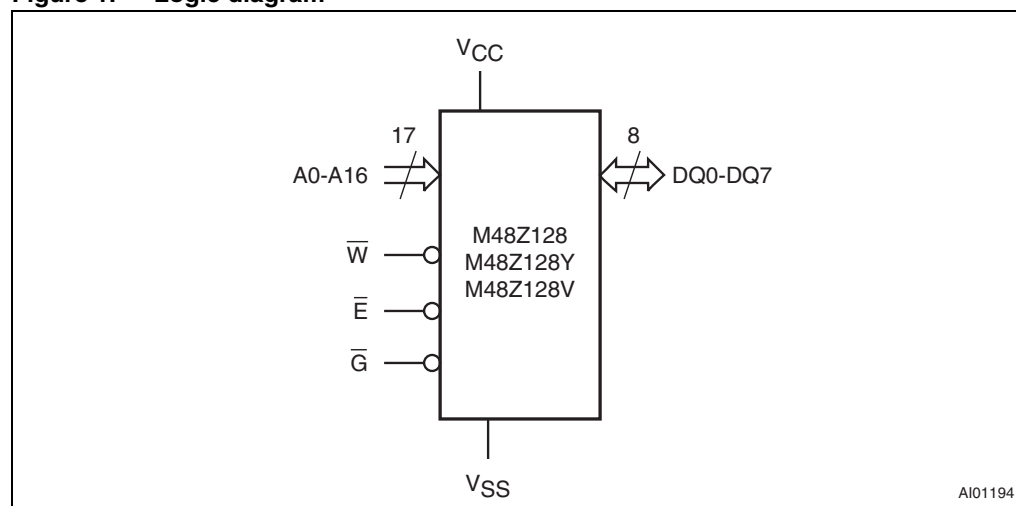


Table 1. Signal names

| | |
|-----------|--------------------------|
| A0-A16 | Address inputs |
| DQ0-DQ7 | Data inputs / outputs |
| \bar{E} | Chip enable input |
| \bar{G} | Output enable input |
| \bar{W} | WRITE enable input |
| V_{CC} | Supply voltage |
| V_{SS} | Ground |
| NC | Not connected internally |

Figure 2. DIP connections

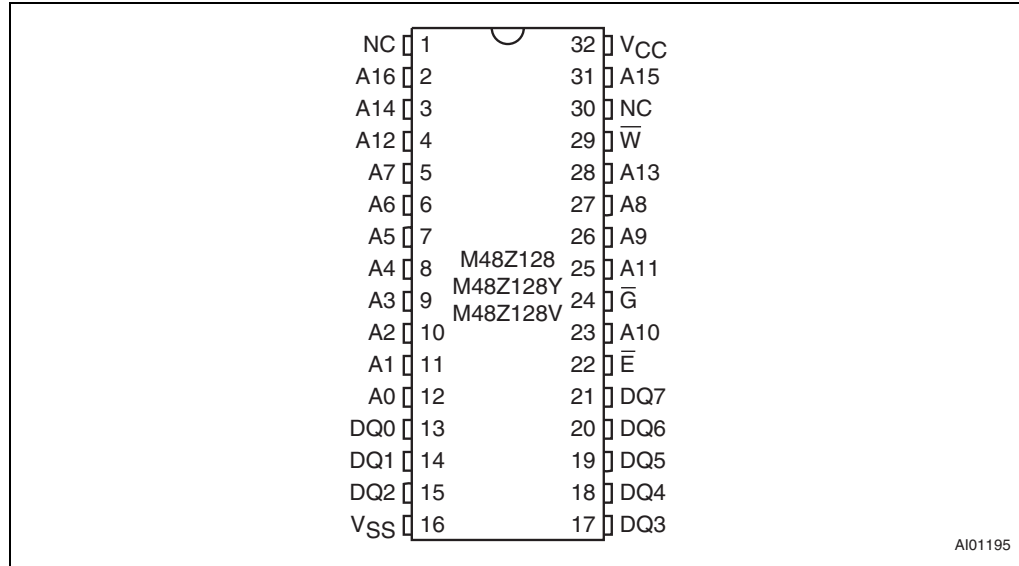
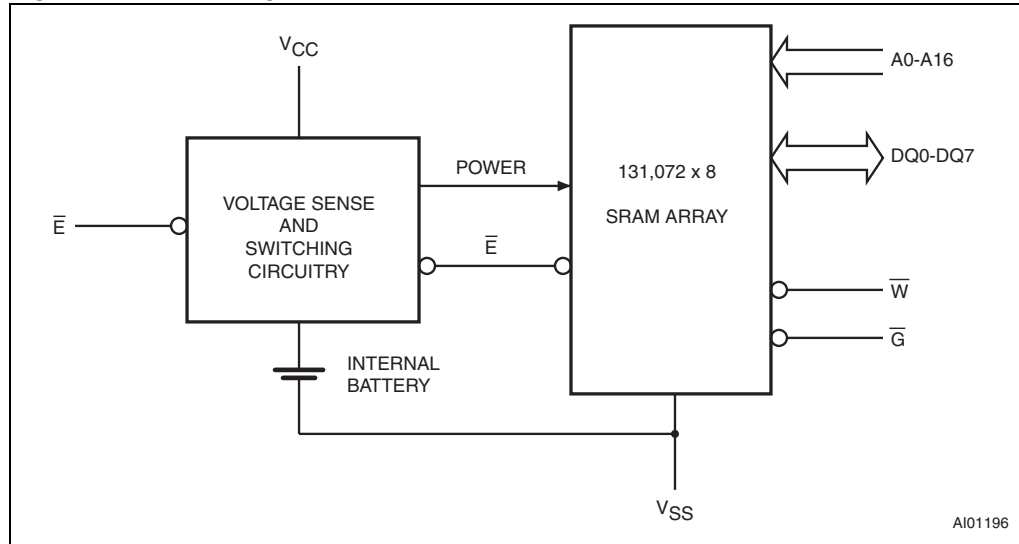


Figure 3. Block diagram



2 Operating modes

The M48Z128/Y/V also has its own power-fail detect circuit. The control circuitry constantly monitors the single V_{CC} supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC} . As V_{CC} falls below the switchover voltage (V_{SO}), the control circuitry connects the battery which maintains data until valid power returns.

Table 2. Operating modes

| Mode | V_{CC} | \bar{E} | \bar{G} | \bar{W} | DQ0-DQ7 | Power |
|----------|--|-----------|-----------|-----------|-----------|---------------------|
| Deselect | 4.75 to 5.5 V | V_{IH} | X | X | High Z | Standby |
| WRITE | or | V_{IL} | X | V_{IL} | D_{IN} | Active |
| READ | 4.5 to 5.5 V | V_{IL} | V_{IL} | V_{IH} | D_{OUT} | Active |
| READ | or | V_{IL} | V_{IH} | V_{IH} | High Z | Active |
| | 3.0 to 3.6 V | V_{IL} | V_{IH} | V_{IH} | High Z | Active |
| Deselect | V_{SO} to V_{PFD} (min) ⁽¹⁾ | X | X | X | High Z | CMOS standby |
| Deselect | $\leq V_{SO}$ ⁽¹⁾ | X | X | X | High Z | Battery backup mode |

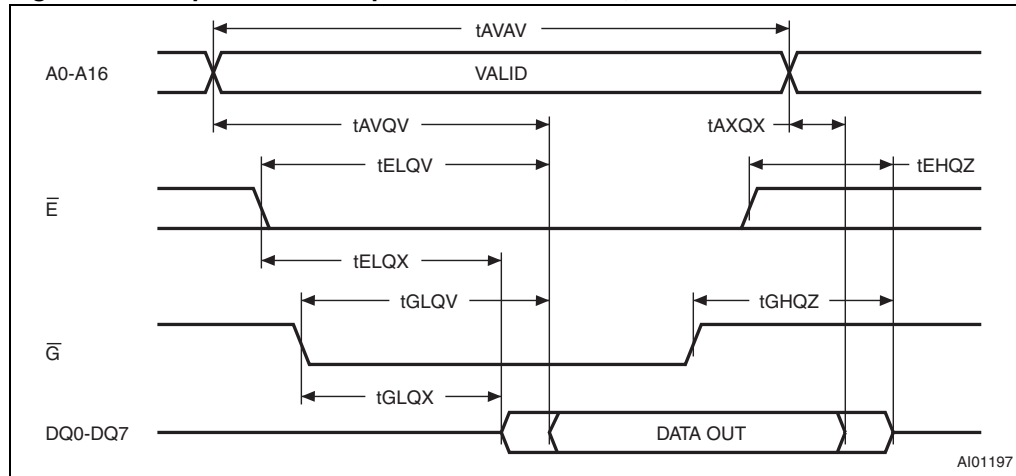
1. See [Table 10 on page 15](#) for details.

Note: $X = V_{IH}$ or V_{IL} ; V_{SO} = battery backup switchover voltage.

2.1 READ mode

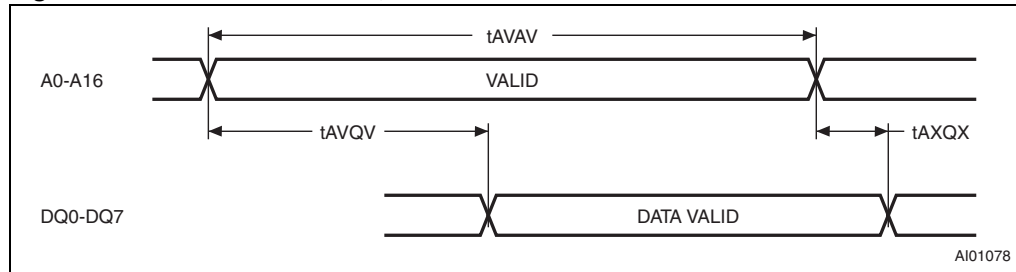
The M48Z128/Y/V is in the READ mode whenever \bar{W} (WRITE enable) is high and \bar{E} (chip enable) is low. The device architecture allows ripple-through access of data from eight of 1,048,576 locations in the static storage array. Thus, the unique address specified by the 17 address inputs defines which one of the 131,072 bytes of data is to be accessed. Valid data will be available at the data I/O pins within address access time (t_{AVQV}) after the last address input signal is stable, providing that the \bar{E} and \bar{G} (output enable) access times are also satisfied. If the \bar{E} and \bar{G} access times are not met, valid data will be available after the later of chip enable access time (t_{ELQV}) or output enable access time (t_{GLQV}). The state of the eight three-state data I/O signals is controlled by \bar{E} and \bar{G} . If the outputs are activated before t_{AVQV} , the data lines will be driven to an indeterminate state until t_{AVQV} . If the address inputs are changed while \bar{E} and \bar{G} remain low, output data will remain valid for output data hold time (t_{AXQX}) but will go indeterminate until the next address access.

Figure 4. Chip enable or output enable controlled, READ mode AC waveforms



Note: WRITE enable (\bar{W}) = high.

Figure 5. Address controlled, READ mode AC waveforms



Note: Chip enable (\bar{E}) and output enable (\bar{G}) = low, WRITE enable (\bar{W}) = high.

Table 3. READ mode AC characteristics

| Symbol | Parameter ⁽¹⁾ | M48Z128/Y | | M48Z128/Y/V | | M48Z128/Y/V | | Unit |
|------------------|---|-----------|-----|-------------|-----|-------------|-----|------|
| | | -70 | | -85 | | -120 | | |
| | | Min | Max | Min | Max | Min | Max | |
| t_{AVAV} | READ cycle time | 70 | | 85 | | 120 | | ns |
| t_{AVQV} | Address valid to output valid | | 70 | | 85 | | 120 | ns |
| t_{ELQV} | Chip enable low to output valid | | 70 | | 85 | | 120 | ns |
| t_{GLQV} | Output enable low to output valid | | 35 | | 45 | | 60 | ns |
| $t_{ELQX}^{(2)}$ | Chip enable low to output transition | 5 | | 5 | | 5 | | ns |
| $t_{GLQX}^{(2)}$ | Output enable low to output transition | 3 | | 3 | | 3 | | ns |
| $t_{EHQZ}^{(2)}$ | Chip enable high to output Hi-Z | | 30 | | 35 | | 45 | ns |
| $t_{GHQZ}^{(2)}$ | Output enable high to output Hi-Z | | 20 | | 25 | | 35 | ns |
| t_{AXQX} | Address transition to output transition | 5 | | 5 | | 10 | | ns |

1. Valid for ambient operating temperature: $T_A = 0$ to 70 °C; $V_{CC} = 4.75$ to 5.5 V, 4.5 to 5.5 V, or 3.0 to 3.6 V (except where noted).

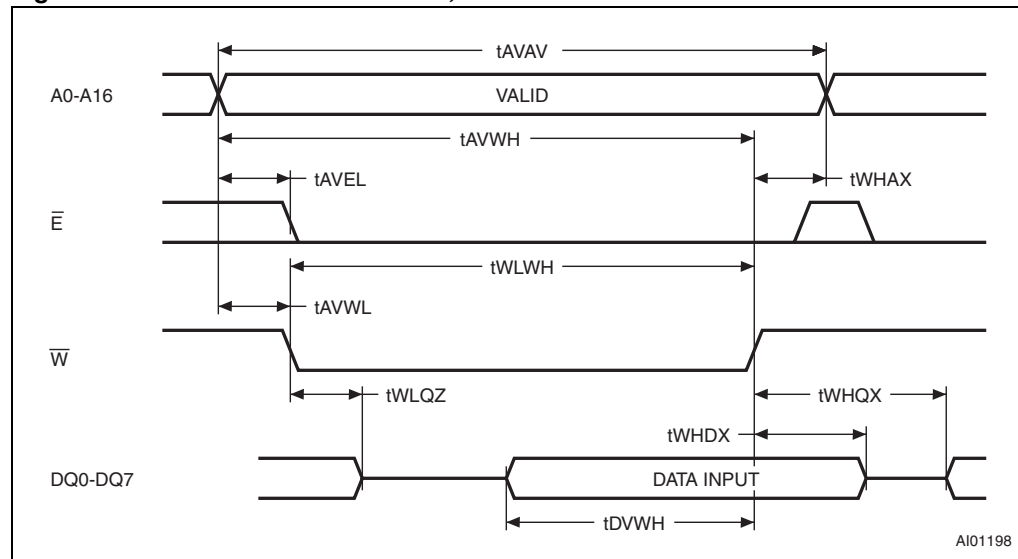
2. $C_L = 5$ pF.

2.2 WRITE mode

The M48Z128/Y/V is in the WRITE mode whenever \overline{W} and \overline{E} are active. The start of a WRITE is referenced from the latter occurring falling edge of \overline{W} or \overline{E} . A WRITE is terminated by the earlier rising edge of \overline{W} or \overline{E} .

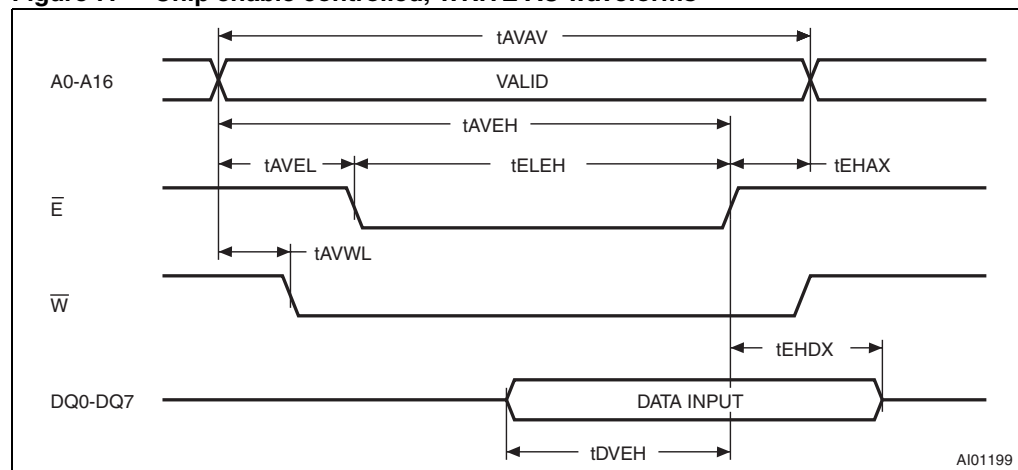
The addresses must be held valid throughout the cycle. \overline{E} or \overline{W} must return high for minimum of t_{EHAX} from \overline{E} or t_{WHAX} from \overline{W} prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} or t_{EHDX} afterward. \overline{G} should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on \overline{E} and \overline{G} , a low on \overline{W} will disable the outputs t_{WLQZ} after \overline{W} falls.

Figure 6. WRITE enable controlled, WRITE AC waveforms



Note: Output enable (\overline{G}) = high.

Figure 7. Chip enable controlled, WRITE AC waveforms



Note: Output enable (\overline{G}) = high.

Table 4. WRITE mode AC characteristics

| Symbol | Parameter ⁽¹⁾ | M48Z128/Y | | M48Z128/Y/V | | M48Z128/Y/V | | Unit |
|---------------------|---|-----------|-----|-------------|-----|-------------|-----|------|
| | | -70 | | -85 | | -120 | | |
| | | Min | Max | Min | Max | Min | Max | |
| t_{AVAV} | WRITE cycle time | 70 | | 85 | | 120 | | ns |
| t_{AVWL} | Address valid to WRITE enable Low | 0 | | 0 | | 0 | | ns |
| t_{AVEL} | Address valid to chip enable low | 0 | | 0 | | 0 | | ns |
| t_{WLWH} | WRITE enable pulse width | 55 | | 65 | | 85 | | ns |
| t_{ELEH} | Chip enable low to chip enable high | 55 | | 75 | | 100 | | ns |
| t_{WHAX} | WRITE enable high to address transition | 5 | | 5 | | 5 | | ns |
| t_{EHAX} | Chip enable high to address transition | 15 | | 15 | | 15 | | ns |
| t_{DVWH} | Input valid to WRITE enable high | 30 | | 35 | | 45 | | ns |
| t_{DVEH} | Input valid to chip enable high | 30 | | 35 | | 45 | | ns |
| t_{WHDX} | WRITE enable high to input transition | 0 | | 0 | | 0 | | ns |
| t_{EHDX} | Chip enable high to input transition | 10 | | 10 | | 10 | | ns |
| $t_{WLQZ}^{(2)(3)}$ | WRITE enable low to output Hi-Z | | 25 | | 30 | | 40 | ns |
| t_{AVWH} | Address valid to WRITE enable high | 65 | | 75 | | 100 | | ns |
| t_{AVEH} | Address valid to chip enable high | 65 | | 75 | | 100 | | ns |
| $t_{WHQX}^{(2)(3)}$ | WRITE enable high to output transition | 5 | | 5 | | 5 | | ns |

- Valid for ambient operating temperature: $T_A = 0$ to 70 °C; $V_{CC} = 4.75$ to 5.5 V, 4.5 to 5.5 V or 3.0 to 3.6 V (except where noted).
- $C_L = 5$ pF.
- If \bar{E} goes low simultaneously with \bar{W} going low, the outputs remain in the high impedance state.

2.3 Data retention mode

With valid V_{CC} applied, the M48Z128/Y/V operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD} . All outputs become high impedance, and all inputs are treated as “Don't care.”

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP} write protection takes place. When V_{CC} drops below V_{SO} , the control circuit switches power to the internal energy source which preserves data.

The internal coin cell will maintain data in the M48Z128/Y/V after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO} . As system power returns and V_{CC} rises above V_{SO} , the battery is disconnected, and the power supply is switched to external V_{CC} . Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER} , normal RAM operation can resume.

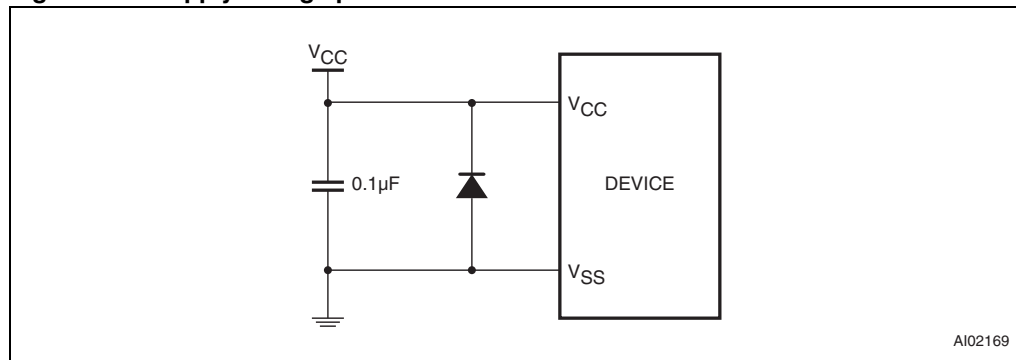
For more information on battery storage life refer to the application note AN1012.

2.4 V_{CC} noise and negative going transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of $0.1 \mu\text{F}$ (see [Figure 8](#)) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, ST recommends connecting a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC} , anode to V_{SS}). (Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface-mount).

Figure 8. Supply voltage protection



3 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

| Symbol | Parameter | Value | Unit | |
|-----------------|---|-----------|-------------|---|
| T_A | Ambient operating temperature | 0 to 70 | °C | |
| T_{STG} | Storage temperature (V_{CC} off, oscillator off) | -40 to 85 | °C | |
| T_{BIAS} | Temperature under bias | -10 to 70 | °C | |
| $T_{SLD}^{(1)}$ | Lead solder temperature for 10 seconds | 260 | °C | |
| V_{IO} | Input or output voltages | -0.3 to 7 | V | |
| V_{CC} | Supply voltage | M48Z128/Y | -0.3 to 7.0 | V |
| | | M48Z128V | -0.3 to 4.6 | V |
| I_O | Output current | 20 | mA | |
| P_D | Power dissipation | 1 | W | |

1. Soldering temperature of the IC leads is to not exceed 260 °C for 10 seconds. In order to protect the lithium battery, preheat temperatures must be limited such that the battery temperature does not exceed +85 °C. Furthermore, the devices shall not be exposed to IR reflow.

Caution: *Negative undershoots below -0.3 V are not allowed on any pin while in the battery backup mode.*

4 DC and AC parameters

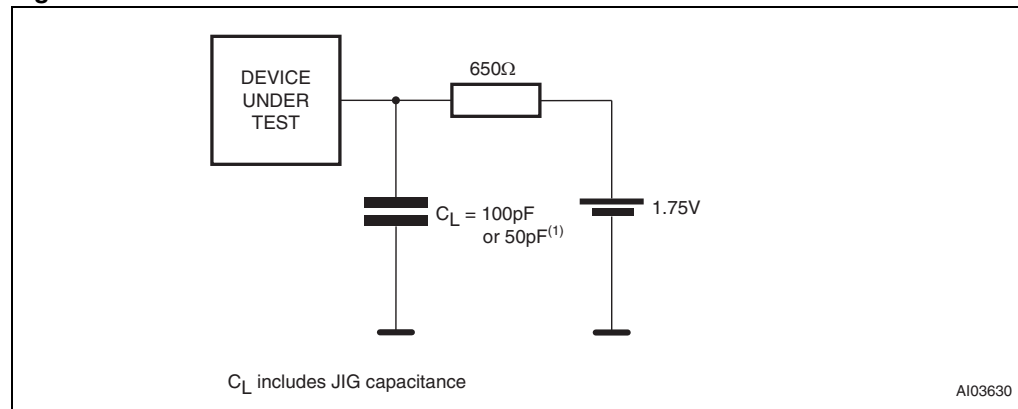
This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 6. Operating and AC measurement conditions

| Parameter | M48Z128/Y | M48Z128V | Unit |
|---|-----------------------------|------------|------|
| Supply voltage (V_{CC}) | 4.75 to 5.5 V or 4.5 to 5.5 | 3.0 to 3.6 | V |
| Ambient operating temperature (T_A) | 0 to 70 | 0 to 70 | °C |
| Load capacitance (C_L) | 100 | 50 | pF |
| Input rise and fall times | ≤ 5 | ≤ 5 | ns |
| Input pulse voltages | 0 to 3 | 0 to 3 | V |
| Input and output timing ref. voltages | 1.5 | 1.5 | V |

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 9. AC measurement load circuit



1. 50 pF for M48Z128V (3.3 V).

Table 7. Capacitance

| Symbol | Parameter ⁽¹⁾⁽²⁾ | Min | Max | Unit |
|----------------|-----------------------------|-----|-----|------|
| C_{IN} | Input capacitance | - | 10 | pF |
| $C_{IO}^{(3)}$ | Input / output capacitance | - | 10 | pF |

1. Effective capacitance measured with power supply at 5 V (M48Z128/Y) or 3.3 V (M48Z128V); sampled only, not 100% tested.
2. At 25 °C, $f = 1$ MHz.
3. Outputs deselected.

Table 8. DC characteristics

| Sym | Parameter | Test condition ⁽¹⁾ | M48Z128/Y | | M48Z128V | | Unit |
|----------------|-------------------------------|---------------------------------------|------------------|----------------|------------|----------------|---------------|
| | | | -70 / -85 / -120 | | -85 / -120 | | |
| | | | Min | Max | Min | Max | |
| I_{LI} | Input leakage current | $0\text{ V} \leq V_{IN} \leq V_{CC}$ | | ± 1 | | ± 1 | μA |
| $I_{LO}^{(2)}$ | Output leakage current | $0\text{ V} \leq V_{OUT} \leq V_{CC}$ | | ± 1 | | ± 1 | μA |
| I_{CC} | Supply current | $\bar{E} = V_{IL}$ Outputs open | | 105 | | 50 | mA |
| I_{CC1} | Supply current (standby) TTL | $\bar{E} = V_{IH}$ | | 7 | | 4 | mA |
| I_{CC2} | Supply current (standby) CMOS | $\bar{E} = V_{CC} - 0.2\text{ V}$ | | 4 | | 3 | mA |
| V_{IL} | Input low voltage | | -0.3 | 0.8 | -0.3 | 0.6 | V |
| V_{IH} | Input high voltage | | 2.2 | $V_{CC} + 0.3$ | 2.2 | $V_{CC} + 0.3$ | V |
| V_{OL} | Output low voltage | $I_{OL} = 2.1\text{ mA}$ | | 0.4 | | 0.4 | V |
| V_{OH} | Output high voltage | $I_{OH} = -1\text{ mA}$ | 2.4 | | 2.2 | | V |

- Valid for ambient operating temperature: $T_A = 0$ to $70\text{ }^\circ\text{C}$; $V_{CC} = 4.75$ to 5.5 V , 4.5 to 5.5 V , or 3.0 to 3.6 V (except where noted).
- Outputs deselected.

Figure 10. Power down/up mode AC waveforms

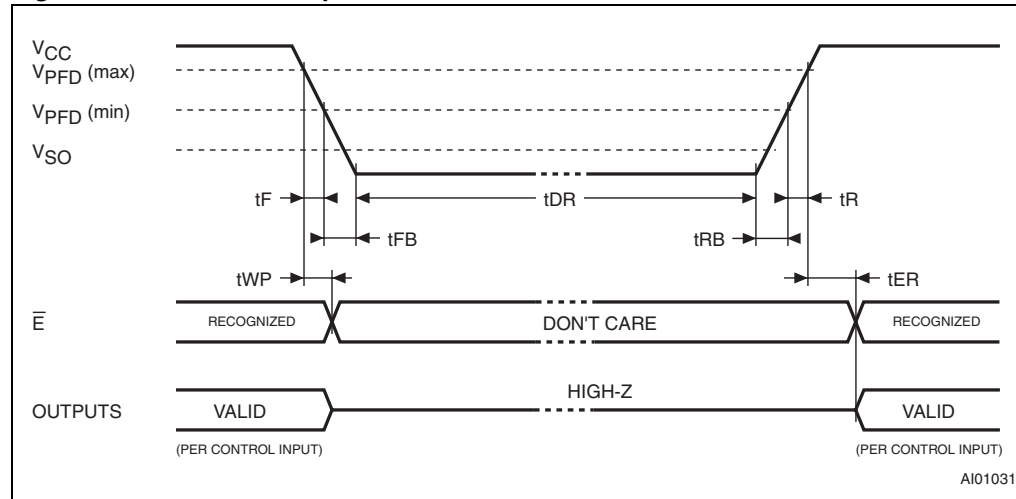


Table 9. Power down/up AC characteristics

| Symbol | Parameter ⁽¹⁾ | Min | Max | Unit | |
|----------------|---|-----------|-----|---------------|---------------|
| $t_F^{(2)}$ | $V_{PFD}(\text{max})$ to $V_{PFD}(\text{min})$ V_{CC} fall time | 300 | | μs | |
| $t_{FB}^{(3)}$ | $V_{PFD}(\text{min})$ to V_{SS} V_{CC} fall time | M48Z128/Y | 10 | μs | |
| | | M48Z128V | 150 | | |
| t_R | $V_{PFD}(\text{min})$ to $V_{PFD}(\text{max})$ V_{CC} rise time | 10 | | μs | |
| t_{RB} | V_{SS} to $V_{PFD}(\text{min})$ V_{CC} rise time | 1 | | μs | |
| t_{WP} | Write protect time | M48Z128/Y | 40 | 150 | μs |
| | | M48Z128V | 40 | 250 | |
| t_{ER} | \bar{E} recovery time | 40 | 120 | ms | |

- Valid for ambient operating temperature: $T_A = 0$ to 70 °C; $V_{CC} = 4.75$ to 5.5 V, 4.5 to 5.5 V, or 3.0 to 3.6 V (except where noted).
- $V_{PFD}(\text{max})$ to $V_{PFD}(\text{min})$ fall time of less than t_F may result in deselection/write protection not occurring until 200 μs after V_{CC} passes $V_{PFD}(\text{min})$.
- $V_{PFD}(\text{min})$ to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.

Table 10. Power down/up trip points DC characteristics

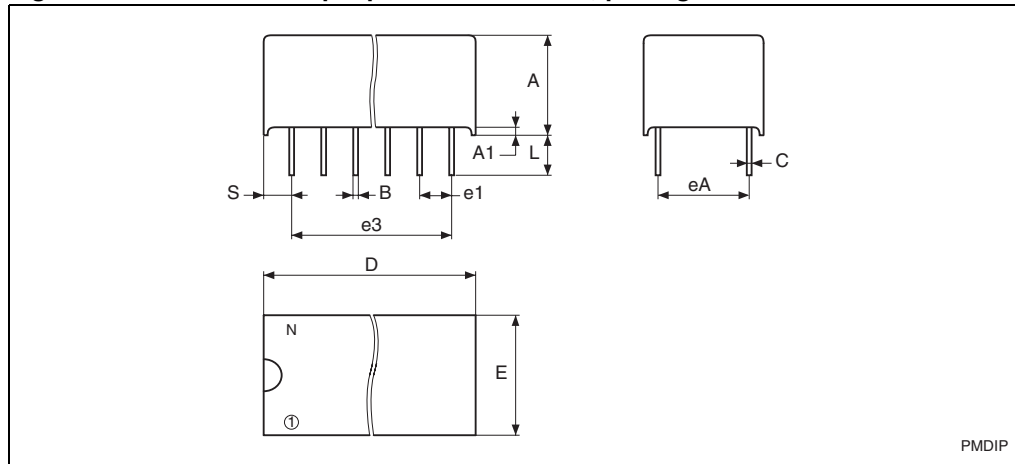
| Symbol | Parameter ⁽¹⁾⁽²⁾ | Min | Typ | Max | Unit | |
|----------------|-----------------------------------|-----------|-----|-----|-------|---|
| V_{PFD} | Power-fail deselect voltage | M48Z128 | 4.5 | 4.6 | 4.75 | V |
| | | M48Z128Y | 4.2 | 4.3 | 4.5 | V |
| | | M48Z128V | 2.8 | 2.9 | 3.0 | V |
| V_{SO} | Battery backup switchover voltage | M48Z128/Y | | 3.0 | | V |
| | | M48Z128V | | 2.5 | | V |
| $t_{DR}^{(3)}$ | Expected data retention time | 10 | | | YEARS | |

- All voltages referenced to V_{SS} .
- Valid for ambient operating temperature: $T_A = 0$ to 70 °C; $V_{CC} = 4.75$ to 5.5 V, 4.5 to 5.5 V, or 3.0 to 3.6 V (except where noted).
- At 25 °C; $V_{CC} = 0$ V.

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 11. PMDIP32 – 32-pin plastic DIP module, package outline



Note: Drawing is not to scale.

Table 11. PMDIP32 – 32-pin plastic DIP module, package mechanical data

| Symb | mm | | | inches | | |
|------|------|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | 9.27 | 9.52 | | 0.365 | 0.375 |
| A1 | | 0.38 | – | | 0.015 | – |
| B | | 0.43 | 0.59 | | 0.017 | 0.023 |
| C | | 0.20 | 0.33 | | 0.008 | 0.013 |
| D | | 42.42 | 43.18 | | 1.670 | 1.700 |
| E | | 18.03 | 18.80 | | 0.710 | 0.740 |
| e1 | | 2.29 | 2.79 | | 0.090 | 0.110 |
| e3 | 38.1 | | | 1.5 | | |
| eA | | 14.99 | 16.00 | | 0.590 | 0.630 |
| L | | 3.05 | 3.81 | | 0.120 | 0.150 |
| S | | 1.91 | 2.79 | | 0.075 | 0.110 |
| N | | 32 | | | 32 | |

6 Part numbering

Table 12. Ordering information scheme

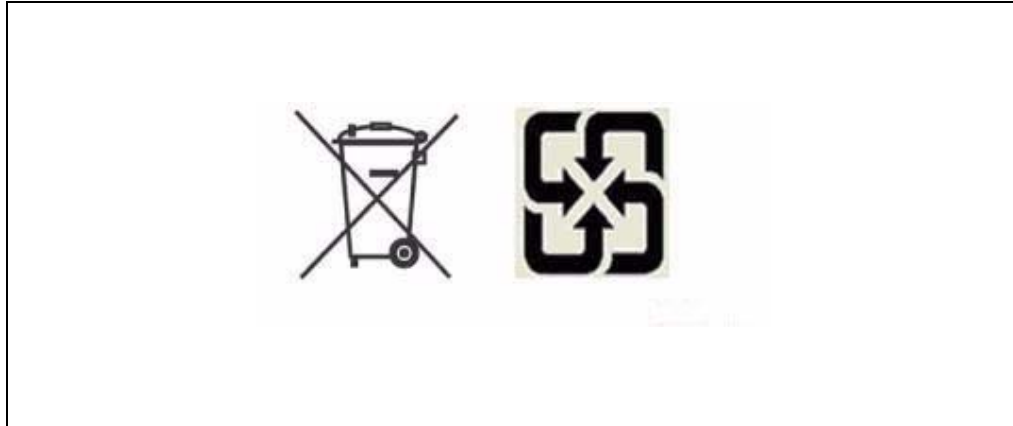
| Example: | M48Z | 128Y | -70 | PM | 1 |
|---|------|------|-----|----|---|
| Device type | | | | | |
| M48Z | | | | | |
| Supply voltage and write protect voltage | | | | | |
| 128 = $V_{CC} = 4.75$ to 5.5 V; $V_{PFD} = 4.5$ to 4.75 V | | | | | |
| 128Y = $V_{CC} = 4.5$ to 5.5 V; $V_{PFD} = 4.2$ to 4.5 V | | | | | |
| 128V ⁽¹⁾ = $V_{CC} = 3.0$ to 3.6 V; $V_{PFD} = 2.8$ to 3.0 V | | | | | |
| Speed | | | | | |
| -70 = 70 ns (for M48Z128/Y) | | | | | |
| -85 = 85 ns (for M48Z128/Y/V) | | | | | |
| -120 = 120 ns (for M48Z128/Y/V) | | | | | |
| Package | | | | | |
| PM = PMDIP32 | | | | | |
| Temperature range | | | | | |
| 1 = 0 to 70 °C | | | | | |
| Shipping method | | | | | |
| blank = ECOPACK [®] package, tubes | | | | | |

1. Contact local ST sales office for availability

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

7 Environmental information

Figure 12. Recycling symbols



This product contains a non-rechargeable lithium (lithium carbon monofluoride chemistry) button cell battery fully encapsulated in the final product.

Recycle or dispose of batteries in accordance with the battery manufacturer's instructions and local/national disposal and recycling regulations.

Please refer to the following web site address for additional information regarding compliance statements and waste recycling.

Go to www.st.com/nvram, then select "Lithium Battery Recycling" from "Related Topics".

8 Revision history

Table 13. Revision history

| Date | Revision | Changes |
|-------------|----------|---|
| May-1999 | 1 | First issue |
| 13-Apr-2000 | 2 | Document layout changed; surface-mount chip set solution added |
| 20-Jun-2000 | 2.1 | t _{GLQX} changed (Table 3) |
| 19-Jul-2000 | 2.2 | M48Z128V added |
| 14-Sep-2001 | 3 | Reformatted; added temperature information (Table 7 , 8 , 3 , 4 , 9 , 10) |
| 07-Nov-2001 | 3.1 | Remove chipset option from ordering Information (Table 12) |
| 20-May-2002 | 3.2 | Modify reflow time and temperature footnotes (Table 5) |
| 18-Nov-2002 | 3.3 | Modifying SMT solution text (Figure 2, 4 ; Table 2) |
| 17-Sep-2003 | 3.4 | Remove references to M68ZXXX (obsolete) parts (Figure 4 ; Table 2); update disclaimer |
| 22-Feb-2005 | 4 | Reformatted; IR reflow, SO package updates (Table 5) |
| 20-Jul-2010 | 5 | Reformatted document; updated Features, Section 3: Maximum ratings, Table 11, 12 ; added ECOPACK [®] text to Section 5 ; added Section 7: Environmental information ; removed SOH28, SNAPHAT [®] housing and all references from datasheet. |

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