# STK11C68-M

## CMOS nvSRAM
## High Performance
## 8K x 8 Nonvolatile Static RAM
## MIL-STD-883/SMD # 5962-92324

### FEATURES

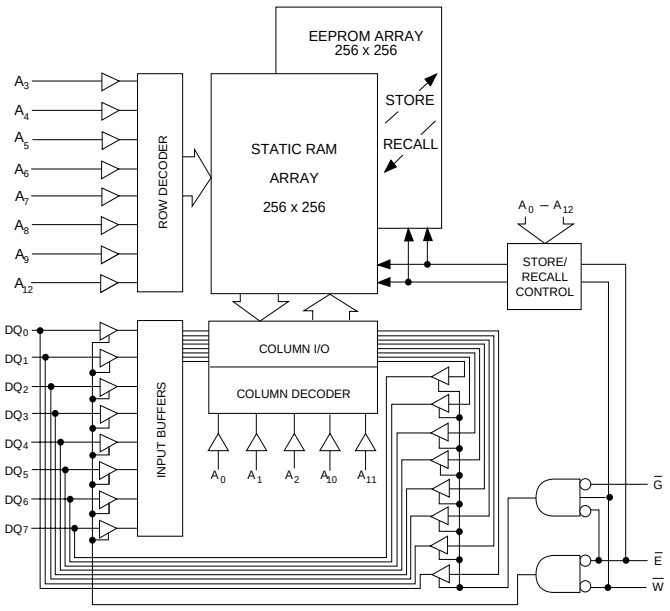
- **35, 45 and 55ns Access Times**
- **17, 20 and 25ns Output Enable Access**
- **Unlimited Read and Write to SRAM**
- **Software *STORE* Initiation**
- **Automatic *STORE* Timing**
- **100,000 *STORE* cycles to EEPROM**
- **10 year data retention in EEPROM**
- **Automatic *RECALL* on Power Up**
- **Software *RECALL* Initiation**
- **Unlimited *RECALL* cycles from EEPROM**
- **Single 5V ± 10% Operation**
- **Available in multiple standard packages**

### DESCRIPTION

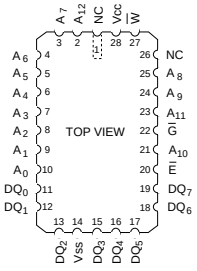
The Simtek STK11C68-M is a fast static RAM (35, 45 and 55ns), with a nonvolatile electrically-erasable PROM (EEPROM) element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (*STORE*), or from the EEPROM to the SRAM (*RECALL*) are initiated through software sequences. It combines the high performance and ease of use of a fast SRAM with nonvolatile data integrity.

The STK11C68-M is pin compatible with industry standard SRAMs and is available in a 28-pin 300 mil ceramic DIP or 28-pad LCC package. Commercial and industrial devices are also available.

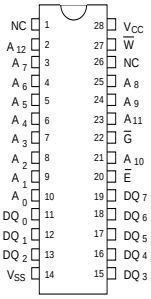
### LOGIC BLOCK DIAGRAM




### PIN CONFIGURATIONS




28 - LCC




28 - 300 C-DIP

### PIN NAMES

| | |
|---|---|
| $A_0$ - $A_{12}$ | Address Inputs |
| $\overline{W}$ | Write Enable |
| $DQ_0$ - $DQ_7$ | Data In/Out |
| $\overline{E}$ | Chip Enable |
| $\overline{G}$ | Output Enable |
| $V_{CC}$ | Power (+5V) |
| $V_{SS}$ | Ground |

## ABSOLUTE MAXIMUM RATINGS[a]

Voltage on typical input relative to $V_{SS}$. . . . . –0.6V to 7.0V
Voltage on $DQ_{0-7}$ and $\overline{G}$. . . . . .–0.5V to ($V_{CC}$+0.5V)
Temperature under bias . . . . . –55°C to 125°C
Storage temperature. . . . . –65°C to 150°C
Power dissipation. . . . . .1W
DC output current . . . . . .15mA
(One output at a time, one second duration)

**Note a:** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC CHARACTERISTICS

($V_{CC}$ = 5.0V ± 10%)

| SYMBOL | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $I_{CC_1}$[b] | Average $V_{CC}$ Current | | 90 | mA | $t_{AVAV}$ = 35ns |
| | | | 85 | mA | $t_{AVAV}$ = 45ns |
| | | | 80 | mA | $t_{AVAV}$ = 55ns |
| $I_{CC_2}$[d] | Average $V_{CC}$ Current during STORE cycle | | 50 | mA | $\overline{E} \geq (V_{CC} - 0.2V)$ all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$ |
| $I_{SB_1}$[c] | Average $V_{CC}$ Current (Standby, Cycling TTL Input Levels) | | 27 | mA | $t_{AVAV}$ = 35ns |
| | | | 23 | mA | $t_{AVAV}$ = 45ns |
| | | | 20 | mA | $t_{AVAV}$ = 55ns $\overline{E} \geq V_{IH}$; all others cycling |
| $I_{SB_2}$[c] | Average $V_{CC}$ Current (Standby, Stable CMOS Input Levels) | | 2 | mA | $\overline{E} \geq (V_{CC} - 0.2V)$ all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$ |
| $I_{ILK}$ | Input Leakage Current (Any Input) | | ±1 | µA | $V_{CC}$ = max $V_{IN} = V_{SS}$ to $V_{CC}$ |
| $I_{OLK}$ | Off State Output Leakage Current | | ±5 | µA | $V_{CC}$ = max $V_{IN} = V_{SS}$ to $V_{CC}$ |
| $V_{IH}$ | Input Logic "1" Voltage | 2.2 | $V_{CC}$+.5 | V | All Inputs |
| $V_{IL}$ | Input Logic "0" Voltage | $V_{SS}$–.5 | 0.8 | V | All Inputs |
| $V_{OH}$ | Output Logic "1" Voltage | 2.4 | | V | $I_{OUT}$ = –4mA |
| $V_{OL}$ | Output Logic "0" Voltage | | 0.4 | V | $I_{OUT}$ = 8mA |
| $T_A$ | Operating Temperature | –55 | 125 | °C | |

Note b: $I_{CC_1}$ is dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: Bringing $\overline{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.
Note d: $I_{CC_2}$ is the average current required for the duration of the store cycle ($t_{STORE}$) after the sequence ($t_{WC}$) that initiates the cycle.

## AC TEST CONDITIONS

Input Pulse Levels. . . . . $V_{SS}$ to 3V
Input Rise and Fall Times. . . . . ≤ 5ns
Input and Output Timing Reference Levels. . . . . 1.5V
Output Load. . . . . See Figure 1

## CAPACITANCE[e] ($T_A$=25°C, f=1.0MHz)

| SYMBOL | PARAMETER | MAX | UNITS | CONDITIONS |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 5 | pF | ΔV = 0 to 3V |
| $C_{OUT}$ | Output Capacitance | 7 | pF | ΔV = 0 to 3V |

Note e: These parameters are guaranteed but not tested.

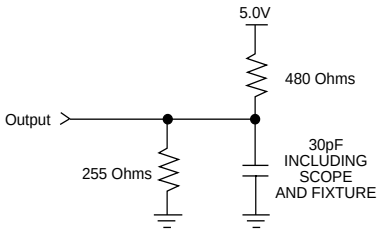



Figure 1: AC Output Loading

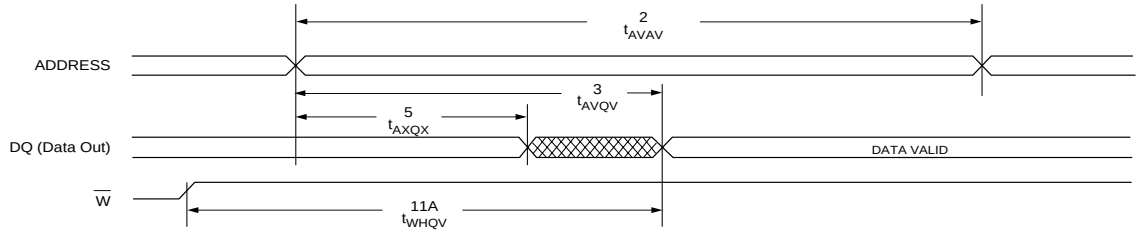
## READ CYCLES #1 & #2

($V_{CC}$ = 5.0V ± 10%)

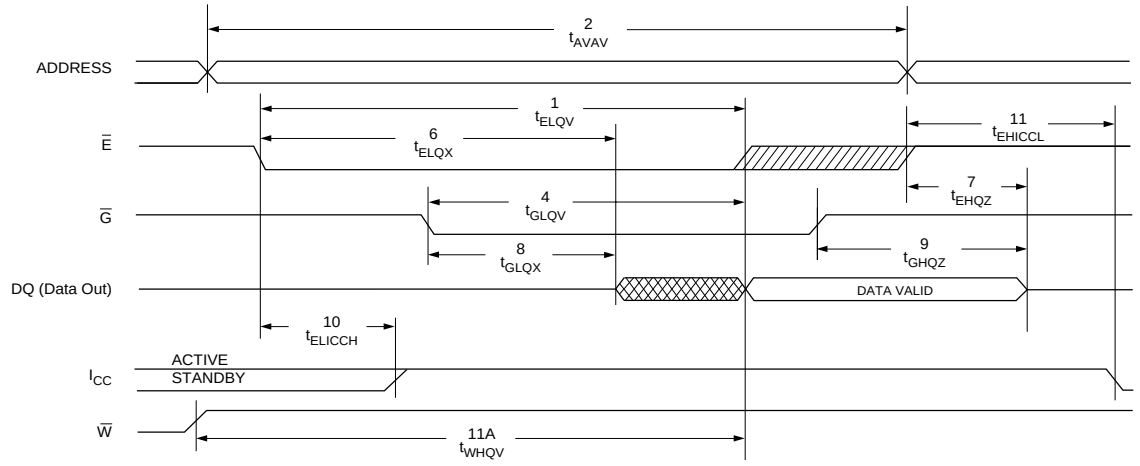
| NO. | SYMBOLS | | PARAMETER | STK11C68-35M | | STK11C68-45M | | STK11C68-55M | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | #1, #2 | Alt. | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{ELQV}$ | $t_{ACS}$ | Chip Enable Access Time | | 35 | | 45 | | 55 | ns |
| 2 | $t_{AVAV}$[g] | $t_{RC}$ | Read Cycle Time | 35 | | 45 | | 55 | | ns |
| 3 | $t_{AVQV}$[h] | $t_{AA}$ | Address Access Time | | 35 | | 45 | | 55 | ns |
| 4 | $t_{GLQV}$ | $t_{OE}$ | Output Enable to Data Valid | | 20 | | 25 | | 25 | ns |
| 5 | $t_{AXQX}$ | $t_{OH}$ | Output Hold After Address Change | 5 | | 5 | | 5 | | ns |
| 6 | $t_{ELQX}$ | $t_{LZ}$ | Chip Enable to Output Active | 5 | | 5 | | 5 | | ns |
| 7 | $t_{EHQZ}$[i] | $t_{HZ}$ | Chip Disable to Output Inactive | | 17 | | 20 | | 25 | ns |
| 8 | $t_{GLQX}$ | $t_{OLZ}$ | Output Enable to Output Active | 0 | | 0 | | 0 | | ns |
| 9 | $t_{GHQZ}$[i] | $t_{OHZ}$ | Output Disable to Output Inactive | | 17 | | 20 | | 25 | ns |
| 10 | $t_{ELICCH}$[e] | $t_{PA}$ | Chip Enable to Power Active | 0 | | 0 | | 0 | | ns |
| 11 | $t_{EHICCL}$[c,e] | $t_{PS}$ | Chip Disable to Power Standby | | 35 | | 45 | | 55 | ns |
| 11A | $t_{WHQV}$ | $t_{WR}$ | Write Recovery Time | | 45 | | 55 | | 65 | ns |

Note c: Bringing $\overline{E}$ high will not produce standby currents until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.
Note e: Parameter guaranteed but not tested.
Note g: For READ CYCLE #1 and #2, $\overline{W}$ must be high for entire cycle.
Note h: Device is continuously selected with $\overline{E}$ low and $\overline{G}$ low.
Note i: Measured ± 200mV from steady state output voltage.

## READ CYCLE #1 [g,h]




## READ CYCLE #2 [g]



## WRITE CYCLES #1 & #2; $\overline{G}$ high

($V_{CC}$ = 5.0V ± 10%)

| NO. | SYMBOLS | | | PARAMETER | STK11C68-35M | | STK11C68-45M | | STK11C68-55M | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | #1 | #2 | Alt. | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 12 | $t_{AVAV}$ | $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time | 35 | | 45 | | 55 | | ns |
| 13 | $t_{WLWH}$ | $t_{WLEH}$ | $t_{WP}$ | Write Pulse Width | 30 | | 35 | | 45 | | ns |
| 14 | $t_{ELWH}$ | $t_{ELEH}$ | $t_{CW}$ | Chip Enable to End of Write | 30 | | 35 | | 45 | | ns |
| 15 | $t_{DVWH}$ | $t_{DVEH}$ | $t_{DW}$ | Data Set-up to End of Write | 18 | | 20 | | 30 | | ns |
| 16 | $t_{WHDX}$ | $t_{EHDX}$ | $t_{DH}$ | Data Hold After End of Write | 0 | | 0 | | 0 | | ns |
| 17 | $t_{AVWH}$ | $t_{AVEH}$ | $t_{AW}$ | Address Set-up to End of Write | 30 | | 35 | | 45 | | ns |
| 18 | $t_{AVWL}$ | $t_{AVEL}$ | $t_{AS}$ | Address Set-up to Start of Write | 0 | | 0 | | 0 | | ns |
| 19 | $t_{WHAX}$ | $t_{EHAX}$ | $t_{WR}$ | Address Hold After End of Write | 0 | | 0 | | 0 | | ns |

## WRITE CYCLES #1 & #2; $\overline{G}$ low

($V_{CC}$ = 5.0V ± 10%)

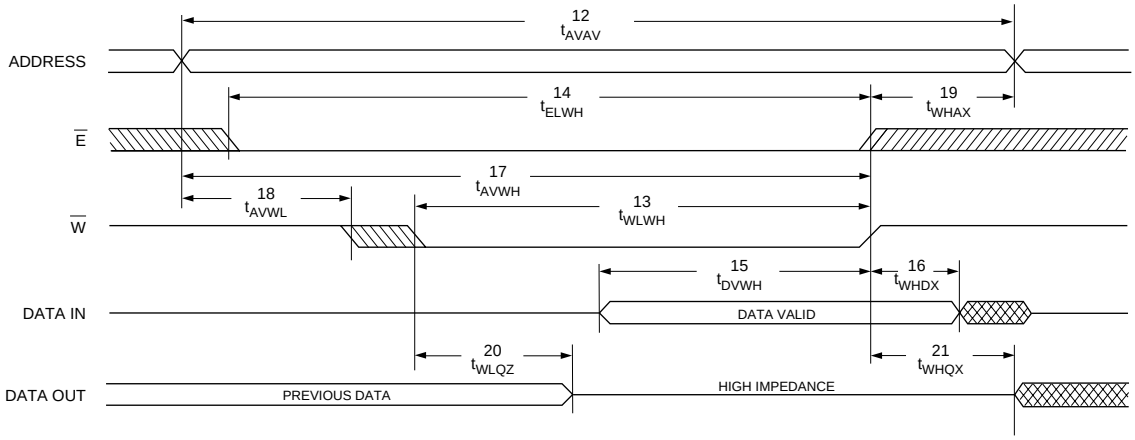
| NO. | SYMBOLS | | | PARAMETER | STK11C68-35M | | STK11C68-45M | | STK11C68-55M | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | #1 | #2 | Alt. | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 12 | $t_{AVAV}$ | $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time | 45 | | 45 | | 55 | | ns |
| 13 | $t_{WLWH}$ | $t_{WLEH}$ | $t_{WP}$ | Write Pulse Width | 35 | | 35 | | 45 | | ns |
| 14 | $t_{ELWH}$ | $t_{ELEH}$ | $t_{CW}$ | Chip Enable to End of Write | 35 | | 35 | | 45 | | ns |
| 15 | $t_{DVWH}$ | $t_{DVEH}$ | $t_{DW}$ | Data Set-up to End of Write | 30 | | 30 | | 30 | | ns |
| 16 | $t_{WHDX}$ | $t_{EHDX}$ | $t_{DH}$ | Data Hold After End of Write | 0 | | 0 | | 0 | | ns |
| 17 | $t_{AVWH}$ | $t_{AVEH}$ | $t_{AW}$ | Address Set-up to End of Write | 35 | | 35 | | 45 | | ns |
| 18 | $t_{AVWL}$ | $t_{AVEL}$ | $t_{AS}$ | Address Set-up to Start of Write | 0 | | 0 | | 0 | | ns |
| 19 | $t_{WHAX}$ | $t_{EHAX}$ | $t_{WR}$ | Address Hold After End of Write | 0 | | 0 | | 0 | | ns |
| 20 | $t_{WLQZ}^{i,m}$ | | $t_{WZ}$ | Write Enable to Output Disable | | 35 | | 35 | | 35 | ns |
| 21 | $t_{WHQX}$ | | $t_{OW}$ | Output Active After End of Write | 5 | | 5 | | 5 | | ns |

Note i: Measured ± 200mV from steady state output voltage.

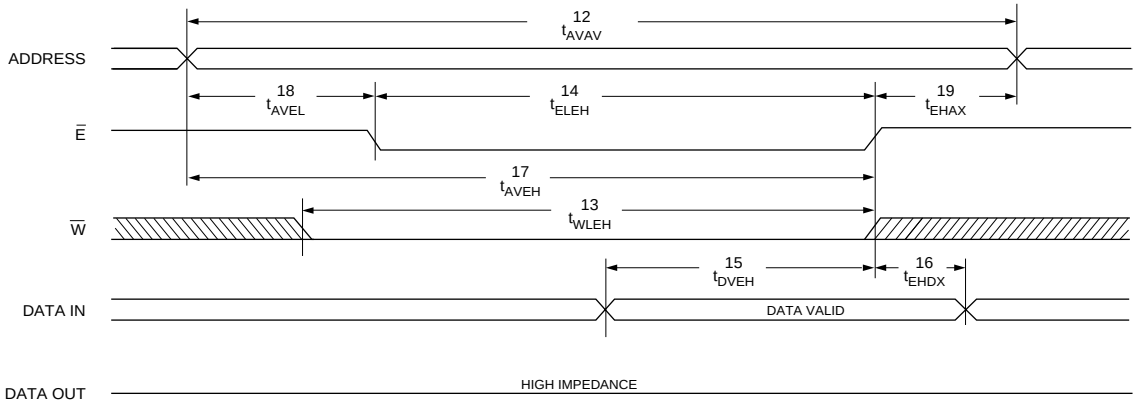
Note k: $\overline{E}$ or $\overline{W}$ must be ≥ $V_{IH}$ during address transitions.

Note m: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.

## WRITE CYCLE #1: $\overline{W}$ CONTROLLED[k]




## WRITE CYCLE #2: $\overline{E}$ CONTROLLED[k]



# NONVOLATILE MEMORY OPERATION

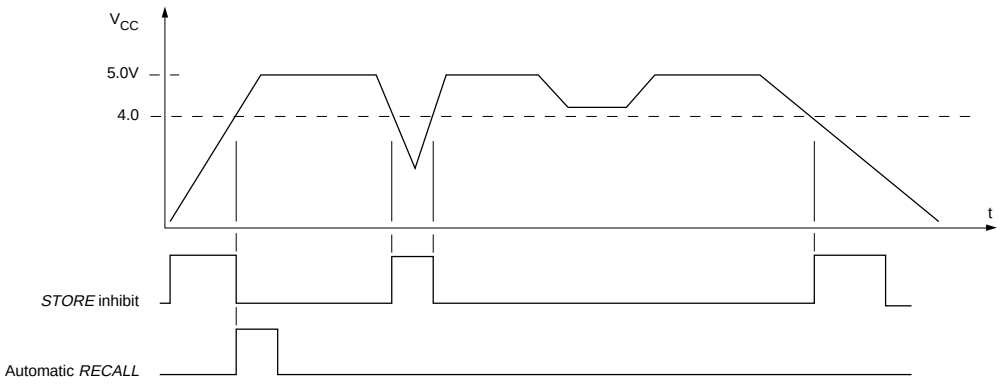
## MODE SELECTION

| $\overline{E}$ | $\overline{W}$ | $A_{12}$ - $A_0$(hex) | MODE | I/O | POWER | NOTES |
|---|---|---|---|---|---|---|
| H | X | X | Not Selected | Output High Z | Standby | |
| L | H | X | Read SRAM | Output Data | Active | o |
| L | L | X | Write SRAM | Input Data | Active | |
| L | H | 0000 | Read SRAM | Output Data | Active | n,o |
| | | 1555 | Read SRAM | Output Data | | n,o |
| | | 0AAA | Read SRAM | Output Data | | n,o |
| | | 1FFF | Read SRAM | Output Data | | n,o |
| | | 10F0 | Read SRAM | Output Data | | n,o |
| | | 0F0F | Nonvolatile *STORE* | Output High Z | $I_{CC2}$ | n |
| L | H | 0000 | Read SRAM | Output Data | Active | n,o |
| | | 1555 | Read SRAM | Output Data | | n,o |
| | | 0AAA | Read SRAM | Output Data | | n,o |
| | | 1FFF | Read SRAM | Output Data | | n,o |
| | | 10F0 | Read SRAM | Output Data | | n,o |
| | | 0F0E | Nonvolatile *RECALL* | Output High Z | | n |

Note n: The six consecutive addresses must be in order listed - (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a *STORE* cycle or (0000, 1555, 0AAA,1FFF, 10F0, 0F0E) for a *RECALL* cycle. $\overline{W}$ must be high during all six consecutive cycles. See *STORE* cycle and *RECALL* cycle tables and diagrams for further details.

Note o: I/O state assumes that $\overline{G} \leq V_{IL}$. Initiation and operation of nonvolatile cycles does not depend on the state of $\overline{G}$.

## *STORE* CYCLE INHIBIT and AUTOMATIC POWER-UP *RECALL*



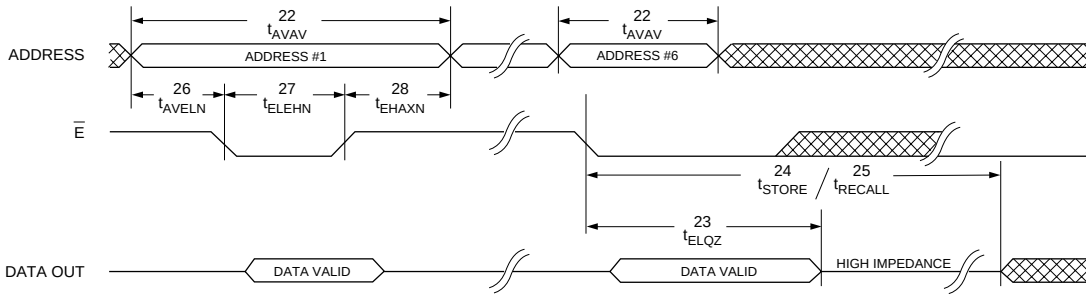
## STORE/RECALL CYCLE

($V_{CC}$ = 5.0V ± 10%)

| NO. | SYMBOLS | | PARAMETER | STK11C68-35M | | STK11C68-45M | | STK11C68-55M | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | #1 | Alt. | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 22 | $t_{AVAV}$ | $t_{RC}$ | *STORE/RECALL* Initiation Cycle Time | 35 | | 45 | | 55 | | ns |
| 23 | $t_{ELQZ}$[p] | | Chip Enable to Output Inactive | | 75 | | 75 | | 85 | ns |
| 24 | $t_{ELQXS}$ | $t_{STORE}$[q] | *STORE* Cycle Time | | 10 | | 10 | | 10 | ms |
| 25 | $t_{ELQXR}$ | $t_{RECALL}$[r] | *RECALL* Cycle Time | | 20 | | 20 | | 20 | µs |
| 26 | $t_{AVELN}$[s] | $t_{AE}$ | Address Set-up to Chip Enable | 0 | | 0 | | 0 | | ns |
| 27 | $t_{ELEHN}$[s,t] | $t_{EP}$ | Chip Enable Pulse Width | 25 | | 35 | | 45 | | ns |
| 28 | $t_{EHAXN}$[s] | $t_{EA}$ | Chip Disable to Address Change | 0 | | 0 | | 0 | | ns |

Note p: Once the software *STORE* or *RECALL* cycle is initiated, it completes automatically, ignoring all inputs.
Note q: Note that *STORE* cycles (but not *RECALL*s) are aborted by $V_{CC}$ < 4.0V (STORE inhibit).
Note r: A *RECALL* cycle is initiated automatically at power up when $V_{CC}$ exceeds 4.0V. $t_{RECALL}$ is measured from the point at which $V_{CC}$ exceeds 4.5V.
Note s: Noise on the $\overline{E}$ pin may trigger multiple read cycles from the same address and abort the address sequence.
Note t: If the Chip Enable Pulse Width is less than $t_{ELQV}$ (see READ CYCLE #2) but greater than or equal to $t_{ELEHN}$, then the data may not be valid at the end of the low pulse, however the *STORE* or *RECALL* will still be initiated.
Note u: $\overline{W}$ must be HIGH when $\overline{E}$ is LOW during the address sequence in order to initiate a nonvolatile cycle. $\overline{G}$ may be either HIGH or LOW throughout. Addresses #1 through #6 are found in the MODE SELECTION table. Address #6 determines whether the STK11C68-M performs a *STORE* or *RECALL*.
Note v: $\overline{E}$ must be used to clock in the address sequence for the Software *STORE* and *RECALL* cycles.

## STORE/RECALL CYCLE [u,v]



# DEVICE OPERATION

The STK11C68-M has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as an ordinary static RAM. In nonvolatile operation, data is transferred from SRAM to EEPROM or from EEPROM to SRAM. In this mode SRAM functions are disabled.

## SRAM READ

The STK11C68-M performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are LOW while $\overline{W}$ is HIGH. The address specified on pins $A_{0-12}$ determines which of the 8192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of $t_{AVQV}$ (READ CYCLE #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at $t_{ELQV}$ or at $t_{GLQV}$, whichever is later (READ CYCLE #2). The data outputs will repeatedly respond to address changes within the $t_{AVQV}$ access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought HIGH or $\overline{W}$ is brought LOW.

The STK11C68-M is a high speed memory and therefore must have a high frequency bypass capacitor of approximately 0.1µF connected between DUT $V_{CC}$ and $V_{SS}$ using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

## SRAM WRITE

A write cycle is performed whenever $\overline{E}$ and $\overline{W}$ are LOW. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ go HIGH at the end of the cycle. The data on pins $DQ_{0-7}$ will be written into the memory if it is valid $t_{DVWH}$ before the end of a $\overline{W}$ controlled WRITE or $t_{DVEH}$ before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept HIGH during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{G}$ is left LOW, internal circuitry will turn off the output buffers $t_{WLQZ}$ after $\overline{W}$ goes LOW.

## NONVOLATILE STORE

The STK11C68-M *STORE* cycle is initiated by executing sequential READ cycles from six specific address locations. By relying on READ cycles only, the STK11C68-M implements nonvolatile operation while remaining pin-for-pin compatible with standard 8Kx8 SRAMs. During the *STORE* cycle, an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile elements. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for *STORE* initiation, it is important that no other read or write accesses intervene in the sequence or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To initiate the *STORE* cycle the following READ sequence must be performed:

| | | | |
|---|---|---|---|
| 1. | Read address | 0000 (hex) | Valid READ |
| 2. | Read address | 1555 (hex) | Valid READ |
| 3. | Read address | 0AAA (hex) | Valid READ |
| 4. | Read address | 1FFF (hex) | Valid READ |
| 5. | Read address | 10F0 (hex) | Valid READ |
| 6. | Read address | 0F0F (hex) | Initiate *STORE* Cycle |

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{G}$ be LOW for the sequence to be valid. After the $t_{STORE}$ cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

## HARDWARE PROTECT

The STK11C68-M offers hardware protection against inadvertent *STORE* cycles through $V_{CC}$ Sense. A *STORE* cycle will not be initiated, and one in progress will discontinue, if $V_{CC}$ goes below 4.0V. 4.0V is a typical, characterized value. The datasheet specifications are guaranteed only for $V_{CC}$ = 5.0 ±10%.

## NONVOLATILE RECALL

A *RECALL* cycle of the EEPROM data into the SRAM is initiated with a sequence of READ operations in a manner similar to the *STORE* initiation. To initiate the *RECALL* cycle the following sequence of READ operations must be performed:

| | | | |
|---|---|---|---|
| 1. | Read address | 0000 (hex) | Valid READ |
| 2. | Read address | 1555 (hex) | Valid READ |
| 3. | Read address | 0AAA (hex) | Valid READ |
| 4. | Read address | 1FFF (hex) | Valid READ |
| 5. | Read address | 10F0 (hex) | Valid READ |
| 6. | Read address | 0F0E (hex) | Initiate *RECALL* Cycle |

Internally, *RECALL* is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The *RECALL* operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

On power-up, once $V_{CC}$ exceeds the $V_{CC}$ sense voltage of 4.0V, a *RECALL* cycle is automatically initiated. The voltage on the $V_{CC}$ pin must not drop below 4.0V once it has risen above it in order for the *RECALL* to operate properly. Due to this automatic *RECALL*, SRAM operation cannot commence until $t_{RECALL}$ after $V_{CC}$ exceeds 4.0V. 4.0V is a typical, characterized value.

If the STK11C68-M is in a WRITE state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected between $\overline{W}$ and system $V_{CC}$.

## ORDERING INFORMATION

**STK11C68 - 5 C 35 M**

**Temperature Range**
M = Military (-55 to 125 degrees C)

**Access Time**
35 = 35ns
45 = 45ns
55 = 55ns

**Package**
C = Ceramic 28 pin 300-mil DIP with gold lead finish
K = Ceramic 28 pin 300-mil DIP with solder DIP finish
L = Ceramic 28 pin LCC

**Retention / Endurance**
10 years / 100,000 cycles

**5962-92324 04 MX X**

**Lead Finish**
A = Solder DIP lead finish
C = Gold lead DIP finish
X = lead finish "A" or "C" is acceptable

**Package**
MX = Ceramic 28 pin 300-mil DIP
MY = Ceramic 28 pin LCC

**Access Time**
04 = 55ns
05 = 45ns
06 = 35ns