

FEATURES

512K x 8 MRAM Memory

- Fast 35ns Read/Write Cycle
- SRAM Compatible Timing, Uses Existing SRAM Controllers Without Redesign
- Unlimited Read & Write Endurance
- Data Always Non-volatile for >20-years at Temperature
- One Memory Replaces Flash, SRAM, EEPROM and BBSRAM in System for Simpler, More Efficient Design
- Replace battery-backed SRAM solutions with MRAM to eliminate battery assembly, improving reliability
- 3.3 Volt Power Supply
- Automatic Data Protection on Power Loss
- Commercial, Industrial, Automotive Temperatures
- RoHS-Compliant SRAM TSOPII Package
- RoHS-Compliant SRAM BGA Package Shrinks Board Area By Three Times







INTRODUCTION

The MR2A08A is a 4,194,304-bit magnetoresistive random access memory (MRAM) device organized as 524,288 words of 8 bits. The MR2A08A offers SRAM compatible 35ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20-years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. The MR2A08A is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.

The MR2A08A is available in small footprint 400-mil, 44-lead plastic small-outline TSOP type-II package or 8 mm x 8 mm, 48-pin ball grid array (BGA) package with 0.75 mm ball centers. These packages are compatible with similar low-power SRAM products and other non-volatile RAM products.

The MR2A08A provides highly reliable data storage over a wide range of temperatures. The product is offered with commercial temperature (0 to +70 °C), industrial temperature (-40 to +85 °C), and automotive temperature (-40 to +125 °C) range options.

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1. DEVICE PIN ASSIGNMENT

Figure 1.1 Block Diagram

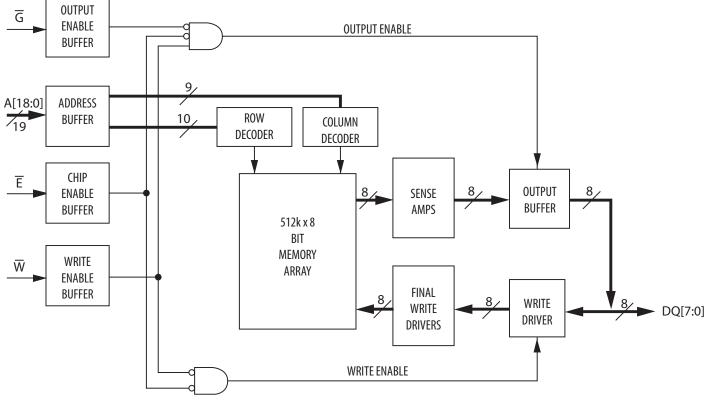
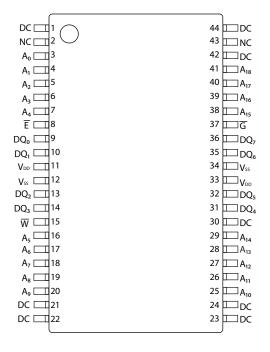


Table 1.1 Pin Functions

Signal Name	Function
А	Address Input
Ē	Chip Enable
\overline{W}	Write Enable
G	Output Enable
DQ	Data I/O
V _{DD}	Power Supply
V _{ss}	Ground
DC	Do Not Connect
NC	No Connection - Pin 2, 43 (TSOPII); Ball H6, G2 (BGA) Reserved For Future Expansion

Figure 1.2 Pin Diagrams for Available Packages (Top View)



G $\left(A_{2}\right)$ DC $\left(A_{o}\right)$ (DC)E (DC) (DQ₀ (NC) $\left(A_{5}\right)$ $\left(A_{6}\right)$ NC (DQ₄) C $\overline{DQ_1}$ (DQ₅) Vss $\left(A_{17}\right)$ (VDD) D $\left(DQ_{2}\right)$ $\left(DQ_{6}\right)$ $\left(V_{SS}\right)$ V_{DD} (DC) A₁₆ (NC)(DQ₇) DQ₃ (A_{14}) A₁₅ (NC) $\left(A_{12}\right)$ (NC) $\left(\overline{\mathsf{w}}\right)$ NC (A₁₃) (NC) A_8 A₉ A₁₀ A₁₁ (NC)

44 Pin TSOP II

48 Pin FBGA

Table 1.2 Operating Modes

ǹ	<u>G</u> 1	W ¹	Mode	V _{DD} Current	DQ[7:0] ²
Н	Х	Χ	Not selected	_{SB1} , _{SB2}	Hi-Z
L	Н	Н	Output disabled	l _{DDR}	Hi-Z
L	L	Н	Byte Read	I _{DDR}	D_{Out}
L	Х	L	Byte Write	l _{DDW}	D _{in}

 $^{^{1}}$ H = high, L = low, X = don't care

² Hi-Z = high impedance

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 2.1 Absolute Maximum Ratings¹

Parameter	Symbol	Value	Unit
Supply voltage ²	V _{DD}	-0.5 to 4.0	V
Voltage on an pin ²	V _{IN}	$-0.5 \text{ to V}_{DD} + 0.5$	V
Output current per pin	I _{OUT}	±20	mA
Package power dissipation	P_{D}	0.600	W
Temperature under bias MR2A08A (Commercial) MR2A08AC (Industrial) MR2A08AM (Automotive)	T _{BIAS}	-10 to 85 -45 to 95 -45 to 130	°C
Storage Temperature	T _{stg}	-55 to 150	°C
Lead temperature during solder (3 minute max)	T_{Lead}	260	°C
Maximum magnetic field during write MR2A08A (All Temperatures)	H _{max_write}	2000	A/m
Maximum magnetic field during read or standby	H _{max_read}	8000	A/m

¹ Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.

 $^{^{2}}$ All voltages are referenced to V_{ss} .

³ Power dissipation capability depends on package characteristics and use environment.

Parameter	Symbol	Value	Typical	Max	Unit
Power supply voltage	V _{DD}	3.0 i	3.3	3.6	V
Write inhibit voltage	V _{wi}	2.5	2.7	3.0 i	٧
Input high voltage	V _{IH}	2.2	-	V _{DD} + 0.3 ii	V
Input low voltage	V _{IL}	-0.5 ⁱⁱⁱ	-	0.8	V
Temperature under bias MR2A08A (Commercial) MR2A08AC (Industrial) MR2A08AM (Automotive) ^{iv}	T _A	0 -40 -40		70 85 125	°C

Table 2.2 Operating Conditions

Power Up and Power Down Sequencing

MRAM is protected from write operations whenever V_{DD} is less than V_{WI} . As soon as V_{DD} exceeds V_{DD} (min), there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The \overline{E} and \overline{W} control signals should track V_{DD} on power up to V_{DD}^- 0.2 V or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that signal remains high if the driving signal is Hi-Z during power up. Any logic that drives \overline{E} and \overline{W} should hold the signals high with a power-on reset signal for longer than the startup time.

During power loss or brownout where V_{DD} goes below V_{WI} , writes are protected and a startup time must be observed when power returns above V_{DD} (min).

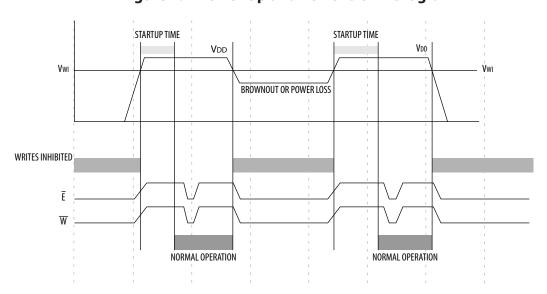


Figure 2.1 Power Up and Power Down Diagram

¹ There is a 2 ms startup time once V_{DD} exceeds V_{DD} (min). See **Power Up and Power Down Sequencing** below.

[&]quot; $V_{IH}(max) = V_{DD} + 0.3 V_{DC}$; $V_{IH}(max) = V_{DD} + 2.0 V_{AC}$ (pulse width ≤ 10 ns) for I ≤ 20.0 mA.

iii $V_{\parallel}(min) = -0.5 V_{DC}$; $V_{\parallel}(min) = -2.0 V_{AC}$ (pulse width ≤ 10 ns) for $I \leq 20.0$ mA.

iv Automotive temperature profile assumes 10% duty cycle at maximum temperature (2-years out of 20-year life)

Electrical Specifications MR2A08A

Table 2.3 DC Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Input leakage current	l _{lkg(l)}	-	-	±1	μΑ
Output leakage current	I _{lkg(O)}	-	-	±1	μΑ
Output low voltage $(I_{OL} = +4 \text{ mA})$ $(I_{OL} = +100 \mu\text{A})$	V _{OL}	-	-	0.4 V _{ss} + 0.2	V
Output high voltage $(I_{OL} = -4 \text{ mA})$ $(I_{OL} = -100 \mu\text{A})$	V _{OH}	2.4 V _{DD} - 0.2	-	-	V

Table 2.4 Power Supply Characteristics

Parameter	Symbol	Typical	Max	Unit
AC active supply current - read modes ¹ $(I_{OUT} = 0 \text{ mA}, V_{DD} = \text{max})$	I _{DDR}	30	66	mA
AC active supply current - write modes ¹ (V _{DD} = max) MR2A08A (Commercial) MR2A08AC (Industrial) MR2A08AM (Automotive)	I _{DDW}	50 50 50	135 135 135	mA
AC standby current $(V_{DD} = max, \overline{E} = V_{H})$ no other restrictions on other inputs	I _{SB1}	13	20	mA
CMOS standby current $(\overline{E} \geq V_{DD} - 0.2 \text{ V and } V_{In} \leq V_{SS} + 0.2 \text{ V or } \geq V_{DD} - 0.2 \text{ V})$ $(V_{DD} = \text{max, } f = 0 \text{ MHz})$	I _{SB2}	8	10	mA

¹ All active current measurements are measured with one address transition per cycle and at minimum cycle time.

3. TIMING SPECIFICATIONS

Table 3.1 Capacitance¹

Parameter	Symbol	Typical	Max	Unit
Address input capacitance	C _{In}	-	6	pF
Control input capacitance	C _{In}	-	6	pF
Input/Output capacitance	C _{1/0}	-	8	pF

 $^{^1~}$ f = 1.0 MHz, dV = 3.0 V, $\rm T_A$ = 25 °C, periodically sampled rather than 100% tested.

Table 3.2 AC Measurement Conditions

Parameter	Value	Unit
Logic input timing measurement reference level	1.5	V
Logic output timing measurement reference level	1.5	V
Logic input pulse levels	0 or 3.0	V
Input rise/fall time	2	ns
Output load for low and high impedance parameters		3.1
Output load for all other timing parameters	ad for all other timing parameters See Figure 3.2	

Figure 3.1 Output Load Test Low and High

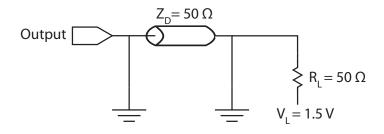
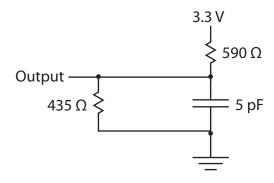


Figure 3.2 Output Load Test All Others



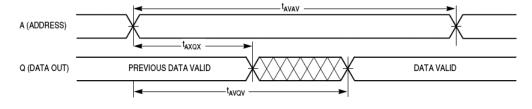
Read Mode

Table 3.3 Read Cycle Timing¹

Parameter	Symbol	Min	Max	Unit
Read cycle time	t _{AVAV}	35	-	ns
Address access time	t _{AVQV}	-	35	ns
Enable access time ²	t _{ELQV}	-	35	ns
Output enable access time	t _{GLQV}	-	15	ns
Output hold from address change	t _{AXQX}	3	-	ns
Enable low to output active ³	t _{ELQX}	3	-	ns
Output enable low to output active ³	t _{GLQX}	0	-	ns
Enable high to output Hi-Z ³	t _{EHQZ}	0	15	ns
Output enable high to output Hi-Z ³	t _{GHQZ}	0	10	ns

 $[\]overline{W}$ is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.

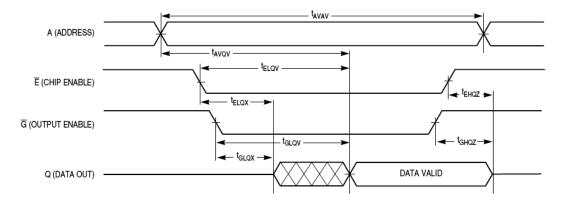
Figure 3.3A Read Cycle 1



NOTES:

Device is continuously selected ($\overline{E} \leq V_{IL}, \ \overline{G} \leq V_{IL}).$

Figure 3.3B Read Cycle 2



² Addresses valid before or at the same time \overline{E} goes low.

³ This parameter is sampled and not 100% tested. Transition is measured ±200 mV from the steady-state voltage.

Timing Specifications MR2A08A

Table 3.4 Write Cycle Timing 1 (W Controlled)¹

	c cycic i iiiiiii g i (ii		-,	
Parameter	Symbol	Min	Max	Unit
Write cycle time ²	t _{AVAV}	35	-	ns
Address set-up time	t _{AVWL}	0	-	ns
Address valid to end of write (\overline{G} high)	t _{avwh}	18	-	ns
Address valid to end of write (\overline{G} low)	t _{avwh}	20	-	ns
Write pulse width (G high)	t _{wlwh}	15	-	ns
Write pulse width (G low)	t _{wlwh}	15	-	ns
Data valid to end of write	t _{DVWH}	10	-	ns
Data hold time	t _{whdx}	0	-	ns
Write low to data Hi-Z³	t _{wLQZ}	0	12	ns
Write high to output active ³	t _{whqx}	3	-	ns
Write recovery time	t _{whax}	12	-	ns

All write occurs during the overlap of \overline{E} low and \overline{W} low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If \overline{G} goes low at the same time or after \overline{W} goes low, the output will remain in a high impedance state. After \overline{W} or \overline{E} has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between \overline{E} being asserted low in one cycle to \overline{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

- ² All write cycle timings are referenced from the last valid address to the first transition address.
- This parameter is sampled and not 100% tested. Transition is measured ± 200 mV from the steady-state voltage. At any given voltage or temperature, $t_{WLOZ}(max) < t_{WHOX}(min)$

A (ADDRESS)

taywh

twhax

Figure 3.4 Write Cycle Timing 1 (W Controlled)

D (DATA IN)

W (WRITE ENABLE)

 t_{WLEH}

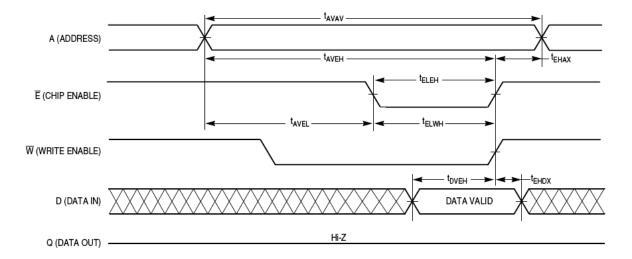
Table 3.5 Write Cycle Timing 2 (E Controlled)¹

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Parameter	Symbol	Min	Max	Unit				
Write cycle time ²	t _{AVAV}	35	-	ns				
Address set-up time	t _{AVEL}	0	-	ns				
Address valid to end of write (G high)	t _{AVEH}	18	-	ns				
Address valid to end of write (G low)	t _{AVEH}	20	-	ns				
Enable to end of write (G high)	t _{eleh} t _{elwh}	15	-	ns				
Enable to end of write (G low) ³	t _{eleh}	15	-	ns				
Data valid to end of write	t _{DVEH}	10	-	ns				
Data hold time	t _{EHDX}	0	-	ns				
Write recovery time	t _{EHAX}	12	-	ns				

All write occurs during the overlap of \overline{E} low and \overline{W} low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If \overline{G} goes low at the same time or after \overline{W} goes low, the output will remain in a high impedance state. After \overline{W} or \overline{E} has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between \overline{E} being asserted low in one cycle to \overline{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

- ² All write cycle timings are referenced from the last valid address to the first transition address.
- If \overline{E} goes low at the same time or after \overline{W} goes low, the output will remain in a high-impedance state. If \overline{E} goes high at the same time or before \overline{W} goes high, the output will remain in a high-impedance state.

Figure 3.5 Write Cycle Timing 2 (E Controlled)



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4. ORDERING INFORMATION

Figure 4.1 Part Numbering System

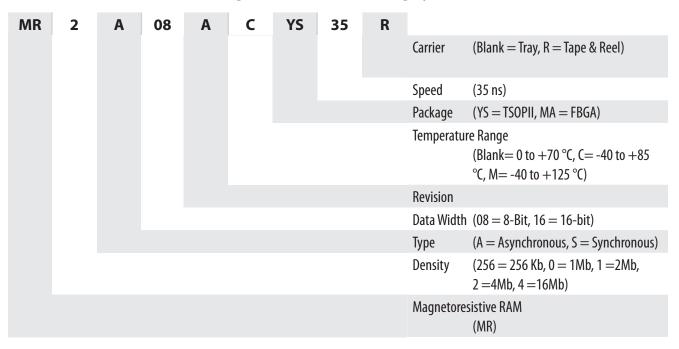


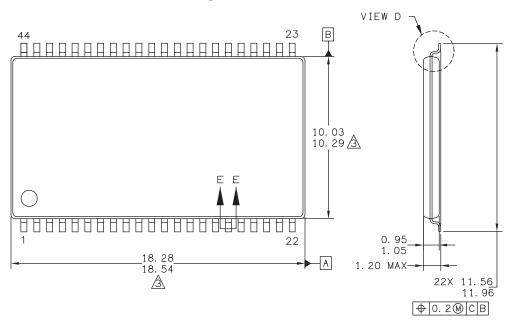
Table 4.1 Available Parts

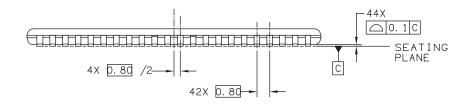
Part Number	Description	Temperature
MR2A08AYS35	3.3 V 512Kx8 MRAM 44-TSOP	Commercial
MR2A08ACYS35	3.3 V 512Kx8 MRAM 44-TSOP	Industrial
MR2A08AMYS35 ¹	3.3 V 512Kx8 MRAM 44-TSOP	Automotive
MR2A08AYS35R	3.3 V 512Kx8 MRAM 44-TSOP T&R	Commercial
MR2A08ACYS35R	3.3 V 512Kx8 MRAM 44-TSOP T&R	Industrial
MR2A08AMYS35R ¹	3.3 V 512Kx8 MRAM 44-TSOP T&R	Automotive
MR2A08AMA35	3.3 V 512Kx8 MRAM 48-BGA	Commercial
MR2A08ACMA35	3.3 V 512Kx8 MRAM 48-BGA	Industrial
MR2A08AMMA35 ¹	3.3 V 512Kx8 MRAM 48-BGA	Automotive

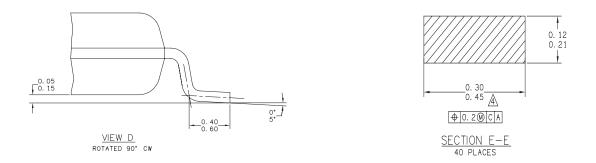
¹ The automotive temperature grade parts are classified as Preliminary, a product in development and/or qualification that has fixed target specifications that are subject to change pending characterization results.

5. MECHANICAL DRAWING

Figure 5.1 TSOP-II







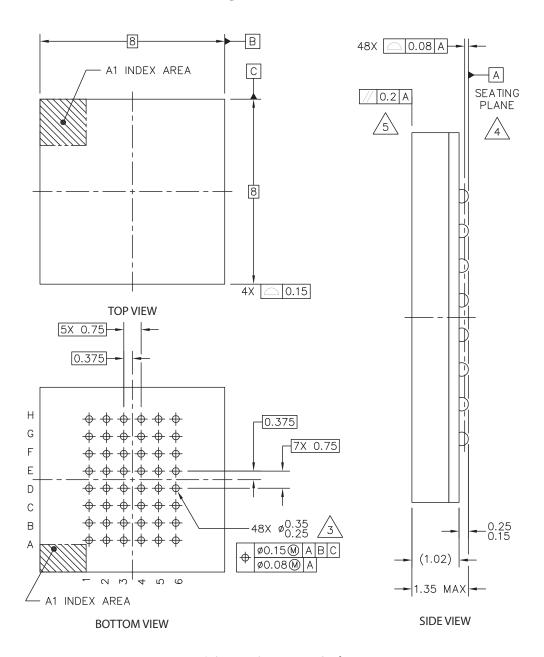
Print Version Not To Scale

- 1. Dimensions and tolerances per ASME Y14.5M 1994.
- 2. Dimensions in Millimeters.
- Dimensions do not include mold protrusion.
- Dimension does not include DAM bar protrusions.

 DAM Bar protrusion shall not cause the lead width to exceed 0.58.

MR2A08A

Figure 5.2 FBGA



Print Version Not To Scale

- 1. Dimensions in Millimeters.
- 2. Dimensions and tolerances per ASME Y14.5M 1994.
- 3. Maximum solder ball diameter measured parallel to DATUM A
- <u>A.</u> DATUM A, the seating plane is determined by the spherical crowns of the solder balls.
- 25. Parallelism measurement shall exclude any effect of mark on top surface of package.

6. REVISION HISTORY

Revision	Date	Description of Change	
0	Oct 25, 2007	Initial Advance Information Release	
1	Oct 29, 2007	Designate pin 23, 24, 42 of TSOPII as DC "Don't Connect" pins since these pins should remain floating at all times. Functional operation of E2 pin defined.	
2	Sep 12, 2008	Reformat Datasheet for Everspin, Delete E2 pin Function, Add BGA Package Information Add Tape & Reel Part Numbers, Add Power Sequencing Info, Correct IOH Spec For VOH to -100 uA, Correct ac Test Conditions	
3	Apr 10, 2009	Add typical and worst case current specifications	
4	July 6, 2009	Changed datasheet from Preliminary to Production except where noted. Updated format.	

Unless otherwise noted, this is a Production Product - This product conforms to specifications per the terms of the Everspin standard warranty. The product has completed Everspin internal qualification testing and has reached production status.

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Document Control Number:

EST00170_MR2A08A, Revision 4.1, 7/2009

File Name:

EST_MR2A08A_prod.pdf

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