GSM/GPRS Digital Baseband Processor

Preliminary Technical Data AD6526

FEATURES

Complete Single Chip Programmable Digital Baseband Processor divided into three main subsystems:
- **Control Processor Subsystem including:**
  - **32-bit MCU ARM7TDMI® Control Processor**
  - **On-chip Zero-wait-state System SRAM**
- **DSP Subsystem including**
  - **16-bit Fixed Point DSP Processor**
  - **Data and Program SRAM**
  - **Program Instruction Cache**
  - **Full Rate, Enhanced Full Rate and Half Rate Speech Encoding/Decoding**
- **Peripheral Subsystem including**
  - **Shared Peripheral Bus and Interface Peripherals**

Peripheral Functions
- **Parallel and Serial Display Interface**
- **Keypad Interface**
- **FLASH Memory Interface**
- **1.8V and 3.0V, 64 kbps SIM Interface**
- **Universal System Connector Interface**
- **Baseband Converter Interface**
- **Data Services Interface**

Control of Radio Subsystem
Three independent programmable backlight outputs
Real Time Clock with Alarm
Programmable Power Management and Clock Management
Supports 13 MHz and 26 MHz Input Clocks
Slow Clocking Scheme for Low Idle Mode Current
Power Down modes
On-chip support for GSM Data Services up to 14.4 kbits/sec, Class 12 GPRS, HSCSD
JTAG Interface for Test and In-Circuit Emulation
1.8V Typical Operating Voltage
Operating Voltage Range 1.7V - 1.9V
Independent I/O and Memory Voltages
160-Ball LFBGA (mini-BGA) package

APPLICATIONS

GSM850/900/DCS1800/PCS1900 Wireless Terminals
GSM Phase 2 & GPRS Compliant

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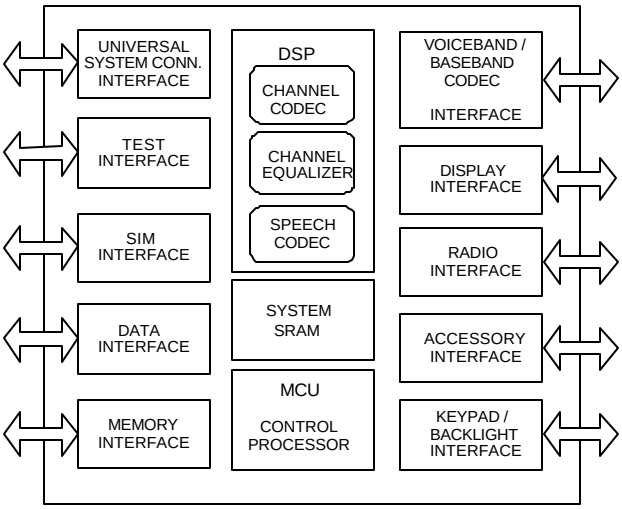

FIGURE 1. AD6526 FUNCTIONAL BLOCK DIAGRAM

GENERAL DESCRIPTION

The AD6526 is the second device, after the AD6522, of the Analog Devices AD20msp430 series of SoftFone® GSM Baseband Processors. The AD6526 provides a competitive solution for GSM/GPRS terminal designs. It is designed to be fully integrated, easy to use, and compatible with GSM900, DCS1800 and PCS1900 handsets as well as direct PC data interface. No external SRAM is needed in most applications.

The AD6526 integrates full rate, enhanced full rate and half rate speech codecs as well as a full range of data services including circuit-switched 14.4 kb/s, GPRS to Class 12, and HSCSD. In addition, it supports both A5/1 and A5/2 encryption algorithms as well as operation in non-encrypted mode.

The highly programmable architecture and sophisticated internal communication channels of the AD6526 offer maximum flexibility to system designers. It can adapt to tighter requirements led by changes in standards and end-market feature set requirements.

A complete data sheet is available under Non-Disclosure Agreement to pre-qualified developers of GSM/GPRS terminal equipment. Contact your local Analog Devices Sales Office.

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