Intel® 80314 I/O Processor Companion Chip

Specification Update

July 2005

Notice: The Intel® 80314 I/O Processor Companion Chip may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Order Number: 273759-010US

Contents

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Revision History

Date	Version	Description
July 2005	010	• Added Documentation Changes 21 and 22.
April 2005	009	• Corrected Port_Arb settings in Erratum 34 and 40 and updated them to include a setting of 11b as fixed in the B1 stepping. • Corrected Errata 43 to read “PCI Class Override Register”. • Edited Specification Clarification 17, adding “PORT_ARB=11 is not effected” to the description. • Added Documentation Change 20.
March 2005	008	• Added Specification Change 13. • Added Documentation Change 19.
August 2004	007	Added erratum 46 (“Possible lost interrupt due to read/write of aliased IACKx registers” on page 27).
July 2004	006	Post-silicon B1 update: • Added erratum 45 (“External PCI/X DMA to SRAM sync packet” on page 27). • Added specification change 12 (“Removal of shadow registers” on page 31). • Added specification clarification 17 (“Driver consideration for shared memory structures under PORT_ARB = 01” on page 35). • Added specification clarification 18 (“PCI Target Abort when Start Address + Cache Line exceeds physical memory” on page 36). • Added documentation change 18 (“GPIO attribute reversal” on page 42). • Minor edits throughout
May 2004	005	• Added information for B1 identification. • Updated Errata 42 (External PCI/X DMA to SDRAM Sync Packet). • Added Errata 44 (GPIO[7:0] pins are driven on reset). • Changed power sequencing requirement in Specification Change 7. • Added Specification Changes 9, 10, and 11.
April 2004	004	• Added information for B0 stepping • Changed status of several errata to “Fixed” (for B0 stepping). • Text corrected in Errata 37 from “low” to “high”. • Added Errata 38–43. • Added Specification Changes 8, 9. • Added Specification Clarifications 11–16. • Added Documentation Changes 15–17.

Date	Version	Description
January 2004	003	• Added Errata 31 to 37. • Added Specification Changes 6 and 7. • Removed Specification Change 4. • Added Specification Clarifications 8, 9, and 10. • Added Documentation Changes 6 to 13. • Changed all references to the *Intel® 80314 I/O Processor Companion Chip Developer Manual* to version 273756-002. • Minor edits for style, grammar, and consistency throughout.
December 2003	002	• Added Errata 28, 29, 30 • Updated Documentation Changes section, added specific references and added documentation change 5 • Updated Specification Changes, Specification Clarifications and Documentation Changes sections with correct formats and sub-sections • Updated this specification update document with Intel template changes
September 2003	001	Initial release.

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
Intel® 80314 I/O Processor Companion Chip Developer's Manual	273756
Intel® 80314 I/O Processor Companion Chip Datasheet	273757
Intel® 80314 I/O Processor Companion Chip Design Guide	273758

Nomenclature

Errata are design defects or errors. These may cause the behavior of the Intel® 80314 I/O Processor Companion Chip to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel® 80314 I/O Processor Companion Chip. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.
Plan Fix:	This erratum may be fixed in a future stepping of the product.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata (Sheet 1 of 2)

No.	Steppings			Page	Status	Errata
	A-0	B-0	B-1			
1.	X			16	Fixed	PE_CSR[R_TA] status bit may not be set
2.	X			16	Fixed	Large burst read may result in SFN queue overwrite
3.	X			16	Fixed	TX FIFO may be mismanaged in half-duplex mode
4.	X	X	X	17	No Fix	Frame abort feature does not work
5.	X	X	X	17	No Fix	CLK_EN signal may glitch high
6.	X	X	X	17	No Fix	High DC current draw when core supply collapses
7.	X			17	Fixed	LS_VECTOR field of the VECTORx registers may report incorrect value 0
8.	X			17	Fixed	A VECTORx read of 0xFF does not always mean that no interrupts are pending
9.	X			18	Fixed	Two Intel XScale® cores cannot be the target of a single interrupt
10.	X	X	X	18	No Fix	DMA channel may require reset following SFN TEA errors
11.	X			18	Fixed	Limitations on SFN outstanding transactions
12.	X	X	X	18	No Fix	DMA and CRC32 or byte-swapping and CRC32 in a single operation may corrupt data
13.	X	X	X	19	No Fix	RxQueue INT is not triggered on error condition
14.	X			19	Fixed	Blank EPROM delays booting of the Intel® 80314 I/O Processor Companion Chip
15.	X			19	Fixed	Inconsistent results when using SRAM
16.	X	X	X	19	No Fix	Multi-byte writes are not supported on the Intel® 80314 I/O Processor Companion Chip
17.	X			20	Fixed	Register swapping lock up
18.	X			20	Fixed	Enable Relaxed Ordering Bit attributes
19.	X			20	Fixed	Bus master enable bit not functional
20.	X	X	X	20	No Fix	Remaining byte-count in split completion message may be incorrect
21.	X			20	Fixed	SDRAM bridging throughput performance limitations
22.	X			21	Fixed	Extra clock cycle on SRAM reads
23.	X			21	Fixed	Use of MSI
24.	X			21	Fixed	IRP_INTAD must be used to mask PCI INTs
25.	X			21	Fixed	MemRead DWORD transaction writes to reserved bits
26.	X			21	Fixed	PFAB_CSR TEA bit is not functional
27.	X			22	Fixed	Bus Number is not updated correctly in the PCI-X Status Register
28.	X			22	Fixed	PCIXCAP[1:0] = 01b is not a valid setting
29.	X			22	Fixed	Clock synchronization issues
30.	X	X	X	22	No Fix	DMA channel hangs when it is stopped with STOP_REQ while CRC is enabled

Errata (Sheet 2 of 2)

No.	Steppings			Page	Status	Errata
	A-0	B-0	B-1			
31.	X	X	X	22	No Fix	5-volt tolerance
32.	X			23	Fixed	INT_PIN field PE_MISC2 00 for A0
33.	X	X	X	23	No Fix	Default SDRAM port arbitration setting can cause SFN starvation
34.	X	X	X	23	No Fix	80/20 port arbitration is not functional
35.	X	X	X	24	No Fix	Erroneous “undersize frame counter” increment
36.	X	X	X	24	No Fix	I2C hang condition
37.	X			24	Fixed	Incorrect PME output signaling
38.	X	X	X	25	No Fix	Testing SDRAM single-bit ECC errors with 64-bit writes
39.	X			25	Fixed	INT_DIS read-only field prevents enabling INTx# assertion
40.		X		25	Fixed	80200 lockup for Port Arbitration settings 11
41.	X	X	X	26	No Fix	INTx_EN (x = A, B, C, D) bits of IRP_INTAD register do not function properly
42.	X	X		26	Fixed	External PCI/X DMA to SDRAM Sync Packet
43.	X	X		26	Fixed	Bit[0] of the Revision ID field of the PCI Class Override Register is stuck at 0
44.	X	X	X	26	No Fix	GPIO[7:0] pins are driven on reset
45.	X	X	X	27	No Fix	External PCI/X DMA to SRAM sync packet
46.	X	X	X	27	No Fix	Possible lost interrupt due to read/write of aliased IACKx registers

Specification Changes

No.	Document Revision	Page	Specification Changes
1.	273756-002	28	Intel® 80314 I/O Processor Companion Chip does not support transparent mode operation
2.	273756-002	28	SFN buffer sizes for PCI-X and SDRAM interfaces
3.	273756-002	28	Only two REQ/GNT pairs are available with the internal arbiter when the PCI-X interface is 100 MHz or greater
4.	N/A	28	This item has been corrected and removed from this specification update
5.	273756-002	28	CacheLineWrap mode is not supported
6.	273757-001	29	Additional nominal and maximum power data; correction of power dissipation values
7.	273757-001 273758-001	29	Power-sequencing requirement
8.	273756-002	30	MPIC interrupt mapping change
9.	273757-001	30	Input hold time on CPU interface
10.	273757-001 273758-001	30	Reset slew rate for battery-backup entry
11.	273757-001 273758-001	31	Reset input hold time for HBA battery-backup entry
12.	273758-001	31	Removal of shadow registers
13.	273756-002	31	Single Data Rate SDRAM is not supported

Specification Clarifications

No.	Document Revision	Page	Specification Clarifications
1.	273756-002	32	Byte swapping must be on data word-aligned boundaries
2.	273756-002	32	MISC_CSR register SOFT_RESET not only asserts the Px_RST pin but also resets the PCI block
3.	273756-002	32	SD_BANK_CTRL register programming restrictions
4.	273756-002	32	Multi-bit ECC error behaviors
5.	273756-002	32	Requirements for booting to other than an 8-bit PBI width
6.	273756-002	33	Time-outs may result in data overwrites
7.	273756-002	33	The Intel® 80314 I/O Processor Companion Chip configuration retry mechanism requires the use of SEEROM
8.	273756-002	33	Intel® 80314 I/O Processor Companion Chip is capable of up to 12 GB but tested only to 3 GB
9.	273756-002	33	Maximum I2C memory
10.	273756-002	33	Proper handling of Gigabit Ethernet WAIT condition
11.	273756-002	34	Proper handling of multi-bit ECC errors in abort handler
12.	273756-002	34	Enabling ECC/parity for SRAM
13.	273756-002	34	64-bit PCI/X addressability
14.	273756-002	35	Reset of Intel® 80314 I/O Processor Companion Chip primary PCI/X without host PCI/X reset
15.	273756-002	35	PCI/X cannot be the destination of a sync packet
16.	273756-002 273757-001	35	SRAM enable/disable pin
17.	273756-002	35	Driver consideration for shared memory structures under PORT_ARB = 01
18.	273756-002	36	PCI Target Abort when Start Address + Cache Line exceeds physical memory

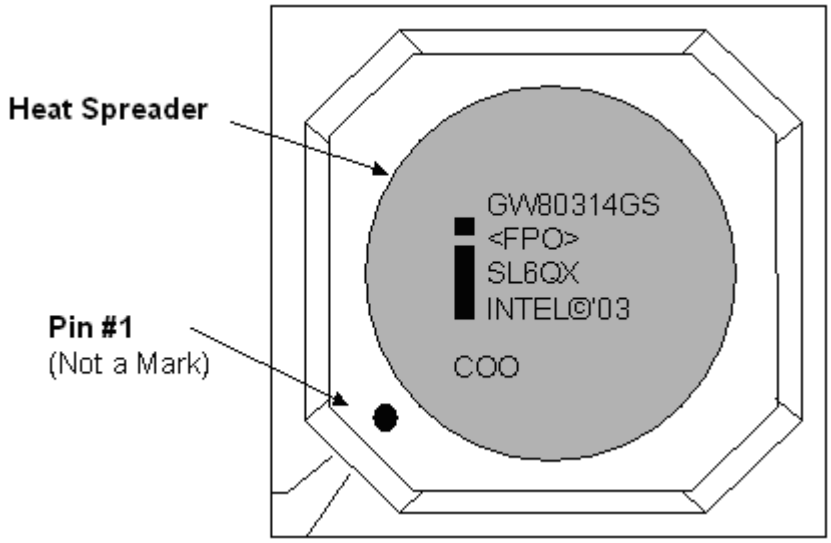
Documentation Changes

No.	Document Revision	Page	Documentation Changes
1.	273756-002	37	PCI-X Bridge Status Register (Embedded Mode) (PE_PCI/X _S) has incorrect values for default bus and function numbers
2.	273756-002	37	PFAB_CSR Register is described incorrectly
3.	273756-002	37	Removed and moved to Errata #39
4.	273756-002	37	Various attribute bits are not correct
5.	273756-002	37	I2C_RD_DATA Register defines incorrect byte order
6.	273756-002	37	GPIO offset is not correct
7.	273757-001	38	Various ball map diagram signals are not correct
8.	273758-001	38	SDRAM feedback clock length
9.	273756-002	38	PCI Interrupt Assertion register IRP_PIA added
10.	273756-002	38	PFAB_MEM32[11:0] field description should be reserved
11.	273756-002 273757-001	39	Incorrect GPIO mappings for UART signals
12.	273756-002	40	I2C capability wording
13.	273756-002	40	PCI/X initialization sequence
14.	273757-001	41	Signal Listing Corrections
15.	273757-001	42	SDRAM PLL bypass
16.	273758-001	42	PWRDELAY circuitry not required for non-battery-backup designs
17.	273758-001	42	Design guideline table missing data
18.	273756-002	42	GPIO attribute reversal
19.	273756-002	42	Single Data Rate SDRAM is not supported
20.	273756-003	42	EE_Bx_ADDR Register Bit [31:8] description is not correct
21.	273756-003	42	Section 2.3.1.3 and 2.3.1.4 not correct
22.	273756-003	43	Table 12 not correct

Identification Information

Markings

Topside Markings (A-0 Example)



Die Details

Stepping	Part Number	QDF (Q)/ Specification Number (SL)	Notes
A-0	GW80314GH	Q468	
A-0	GW80314GN	Q469	
A-0	GW80314GS	Q471	
A-0	GW80314GS	Q472	
B-0	GW80314GN	Q738	
B-0	GW80314GN	Q739	
B-0	GW80314GN	SL7DC	
B-0	GW80314GS	Q740	
B-0	GW80314GS	Q741	
B-0	GW80314GS	SL7DD	
B-1	GW80314GN	Q869	
B-1	GW80314GN	Q865	
B-1	GW80314GN	SL7NL	
B-1	GW80314GS	Q868	
B-1	GW80314GS	Q864	
B-1	GW80314GS	SL7NK	

Device ID Registers

Device and Stepping	PCI ID Register (Offset 0x000)	PCI Revision ID (Offset 0x008)	JTAG Device ID
80314 A-0	• 0x5378 = with SRAM • 0x5389 = without SRAM • VID = 0x8060 always	0x0	• 0x00584013 = with SRAM • 0x00585013 = without SRAM
80314 B-0	• 0x5378 = with SRAM • 0x5389 = without SRAM • VID = 0x8060 always	0x1	• 0x10584013 = with SRAM • 0x10585013 = without SRAM
80314 B-1	• 0x5378 = with SRAM • 0x5389 = without SRAM • VID = 0x8060 always	0x2	• 0x20584013 = with SRAM • 0x20585013 = without SRAM

Errata

1. PE_CSR[R_TA] status bit may not be set

Problem: When the Intel® 80314 I/O Processor Companion Chip (called hereafter "the 80314") is configured for embedded mode and the destination is one of the PCI-X interfaces, when the 80314 masters a Mem_Read_Mult command for which it receives target abort, the PE_CSR[R_TA] status bit is not set.

Implication: This behavior prevents the assertion of an interrupt that may be mapped to this bit.

Workaround: When the source is one of the PCI interfaces, the 80314 signals a target abort to the originating master.

When the source is one of the PCI-X interfaces, the 80314 returns a split completion message indicating a device-specific error. When the initiator receives one of these error indications and finds no status detailing the source of the error after interrogating the PE_CSR register, then the initiator must interrogate the CSR register of the destination targets to determine whether one of them signaled a target abort.

All other sources other than the PCI-X blocks receive an SFN response indicating an error.

Status: Fixed

2. Large burst read may result in SFN queue overwrite

Problem: When the 80314 PCI-X interface accepts a burst read that is decomposed (broken down to 256-byte chunks) for SFN transmission, and an error response is received from the SFN while doing the completion, then the 80314 overwrites the SFN queue.

Implication: This may or may not overwrite the data for the related transaction, and it may also cause issues with other PCI-X transactions.

Workaround: Sources of the error can be a Master Abort, Target Abort, PERR, SERR on the other PCI-X port, or a parity error on the SDRAM interface. When the system sees any of these errors, it must address the problem and reset the system.

Status: Fixed

3. TX FIFO may be mismanaged in half-duplex mode

Problem: When operating in half-duplex mode, it is possible for the TX FIFO to be mismanaged.

Implication: Mismanagement of the TX FIFO may result in under-run reporting and dropped frames. Ultimately this may lead to a lockup condition in which TX data is no longer transmitted.

Workaround: Use only full-duplex mode.

Status: Fixed

4. Frame abort feature does not work

Problem: The MAC has a feature that allows an “excessively deferred frame” to be aborted when it is backed up in the TX outgoing FIFO due to heavy Ethernet traffic. This feature does not work correctly.

Implication: When enabled, the firmware sees status indicating that the frame is aborted, when in fact it still sits in the FIFO. The FIFO status is reported correctly, so no over-run occurs.

Workaround: Do not enable this feature at offset 0x00c or 0x40c, or use only full-duplex mode. Note that this feature is disabled by default.

Status: No Fix

5. CLK_EN signal may glitch high

Problem: The SSTL2 I/O can glitch and change state when the 2.5 V supply is held up as the 1.2 V core supply collapses.

Implication: This problem can cause the CLK_EN signal, which must be held low when entering power-down mode, to glitch high.

Workaround: The 2.5 V supply to the 80314 must be isolated by means of a FET switch during power-down to ensure that the I/Os on the interface cannot switch.

Status: No Fix

6. High DC current draw when core supply collapses

Problem: The SSTL2 I/O potentially drives to a high state when the 2.5 V supply is held up and the 1.2 V core supply collapses.

Implication: This problem causes high DC current draw, since all signals are terminated to 1.25 V through a 65 Ω resistor. Current is 20 mA per I/O, or 2.5 A for the entire interface.

Workaround: The 2.5 V supply to the 80314 must be isolated by means of a FET switch during power-down to ensure that the I/Os on the interface cannot switch.

Status: No Fix

7. LS_VECTOR field of the VECTORx registers may report incorrect value 0

Problem: In the event that a level-sensitive interrupt is de-asserted prior to processing, the LS_VECTOR field of the VECTORx registers may intermittently report 0 instead of the correct vector value.

Implication: The source vector for a spurious vector might be reported at 0x0.

Workaround: When configured to use level-sensitive interrupts, initialize all source vector registers to non-zero values. These values are application-dependent and must be chosen so as not to adversely impact the system. Upon receiving notification of a spurious vector, first check to see that the source is non-zero to ensure that it is a real spurious vector.

Status: Fixed

8. A VECTORx read of 0xFF does not always mean that no interrupts are pending

Problem: A VECTORx read of 0xFF does not always mean that no interrupts are pending.

Implication: Software mechanisms that poll the VECTOR register in their ISR in order to process multiple INTs with minimal context switches cannot use the value of 0xFF to identify when no INTs are pending.

Workaround: When a spurious vector is reported, software must read the register indicated by the LS_VECTOR field in the VECTORx register to determine whether the INT is truly spurious

Status: Fixed

9. Two Intel XScale® cores cannot be the target of a single interrupt

Problem: Only one interrupt output may be selected in the SEL_OUT field of the control registers for each interrupt source.

Implication: When two Intel XScale® cores are implemented in a single design, they cannot both be the target of an interrupt.

Workaround: When both cores require notification of an interrupt, one core must be specified as the target and must use an application-specific mechanism to report the interrupt to the other core. Examples are shared memory, use of the doorbell interrupt in the MPIC, and so on.

Status: Fixed

10. DMA channel may require reset following SFN TEA errors

Problem: When a DMA receives a TEA from the SFN, a channel may get hung in the active state (DACT asserted).

Implication: When a DMA channel is hung with DACT asserted, the DMA channel cannot be re-programmed for another DMA transfer until it is soft-reset.

Workaround: When firmware detects a TEA from the SFN, it must ensure that the DMA channel(s) affected are soft-reset by means of the CHx_GCSR if they are hung with DACT asserted.

Status: No Fix

11. Limitations on SFN outstanding transactions

Problem: When a read transaction is decomposed internally by the 80314 with one PCI-X bus master controlling traffic to the other PCI-X block in embedded mode, all additional reads are held up until there is only one remaining segment to be returned.

Implication: In a worst-case scenario, only one outstanding transaction that is 256 bytes (or misaligned transaction > ~128 bytes) is serviced at one time.

Workaround: None

Status: Fixed

12. DMA and CRC32 or byte-swapping and CRC32 in a single operation may corrupt data

Problem: Performing a DMA+CRC32 operation or ByteSwap+CRC32 with one of the PCI-X blocks as source may corrupt the CRC because PCI-X read completions might complete out of order.

Implication: CRC32 cannot be calculated during a DMA operation with one of the PCI-X blocks as the source. Byte swapping cannot be performed together with a CRC32.

Workaround: The software workaround requires the data to be transferred from a PCI-X block to memory (SDRAM or SRAM), and then have the CRC calculated in place as a separate operation. As long as the data going into the DMA engine does not originate directly from a PCI-X block, the data can be transferred to any location (including PCI-X) while calculating the CRC.

Status: No Fix

13. RxQueue INT is not triggered on error condition

Problem: The RxQueue interrupt bit of the Gigabit Ethernet port interrupt status register is not set when an error condition occurs.

Implication: An RxQueue interrupt may be missed without proper attention to this errata.

Workaround: The driver must understand that when an RxError interrupt is seen in the Gigabit Ethernet port interrupt status register, an RXQueue interrupt is also associated, even though it is not set in the port interrupt status register.

Status: No Fix

14. Blank EPROM delays booting of the Intel® 80314 I/O Processor Companion Chip

Problem: When a blank EPROM is attached to the 80314 I^2C bus, the 80314 may take up to 90 seconds to boot.

Implication: Longer boot time.

Workaround: Program the EPROM to set some register values.

Status: Fixed

15. Inconsistent results when using SRAM

Problem: Data header integrity issues have been seen when DMA or GigE descriptors are placed in SRAM.

Implication: SRAM should not be used.

Workaround: Use SDRAM.

Status: Fixed

16. Multi-byte writes are not supported on the Intel® 80314 I/O Processor Companion Chip

Problem: When performing a multi-byte write on I^2C, the 80314 breaks up the write into multiple single-byte writes. The I^2C EEPROM requires at least 10 ms before accepting the next write. The I^2C does not provide enough time for one byte to complete before starting the next.

Read accesses are not affected by this issue.

Implication: For multi-byte writes on I^2C remaining byte, write(s) following the first time-out while waiting for the target device to come out of the busy state.

Workaround: Multi-byte writes must not be performed. The software must write one byte at a time and must wait the proper amount of time between single-byte writes. The software must also monitor the status of the I^2C to ensure that the write went out and that enough time was given for the target device to become non-busy.

Status: No Fix

17. Register swapping lock up

Problem: The following two combinations of BSWAP, WSWAP, and RGSWAP registers causes the 80314 to lock up:

- RGSWAP and WSWAP without BSWAP
- RGSWAP and BSWAP without WSWAP

Implication: RGSWAP is not available without data swap.

Workaround: None

Status: Fixed

18. Enable Relaxed Ordering Bit attributes

Problem: The Enable Relaxed Order Bit (RO_EN) in the PCI-X Capability Register (PE_PCI/X_C) is incorrectly reset to 0. This bit should be reset to 1.

Implication: None

Workaround: Because the value is read/write, firmware may change the value to 0.

Status: Fixed

19. Bus master enable bit not functional

Problem: Setting the Bus Master Enable bit to 0 in the PCI-X Command Register may not prohibit the 80314 from mastering transactions on the respective PCI-X segment.

Implication: Implications vary depending on usage/reliance of the BME bit.

Workaround: None

Status: Fixed

20. Remaining byte-count in split completion message may be incorrect

Problem: The 80314 may return the incorrect byte-count on a split completion message when both of the following occur:

1. A read is accepted that is greater than 1024 bytes, and
2. An error occurs in the first 256 bytes.

Implication: Some upstream bridges may use this byte count to optimize their own buffer usage.

Workaround: None

Status: No Fix

21. SDRAM bridging throughput performance limitations

Problem: There is an issue with the way the synchronization is done between the SFN and SDRAM clock domains that may impact performance.

Implication: Performance through SDRAM (one PCI bus writing and one reading) is impacted by approximately 5%.

Workaround: None

Status: Fixed

22. Extra clock cycle on SRAM reads

Problem: When making multiple 32-byte reads to internal SRAM, there is a dead clock cycle inserted between the 32-byte accesses.

Implication: Performance on multiple 32-byte reads to SRAM may be impacted by up to 20%.

Workaround: None

Status: Fixed

23. Use of MSI

Problem: The MM_CAP[2:0] field in the P_MSIC register at offset 0x0E0 cannot be changed from its default value of four messages.

Implication: In an environment where another agent is configuring MSI, the 80314 does not support MSI functionality, since the configuring agent may allocate less than four messages, which the 80314 would be unable to accommodate.

Workaround: Use legacy interrupts.

Status: Fixed

24. IRP_INTAD must be used to mask PCI INTs

Problem: The P_INT bit in the IRP_ENABLE register at offset 0x188 does not function as documented. The IRP_INTAD register at offset 0x18C can be used to selectively mask INTA–D interrupt inputs for passing to the internal interrupt controller, and IRP_ENABLE[P_INT] is designed to allow masking all (the “OR”) of the A–D interrupts from being passed to the MPIC. Instead, the INTA–D interrupts are passed to the MPIC, regardless of the setting of IRP_ENABLE[P_INT].

Implication: The P_INT bit in the IRP_ENABLE register cannot be used to mask interrupts.

Workaround: Use the IRP_INTAD register to mask INTA–D.

Status: Fixed

25. MemRead DWORD transaction writes to reserved bits

Problem: As an initiator, the 80314 drives a value of 0x8 on AD[7:0] during the attribute phase. This behavior occurs only when doing a MemRead DWORD transaction.

Implication: The PCI-X 1.0a specification defines these bits as reserved.

Workaround: None

Status: Fixed

26. PFAB_CSR TEA bit is not functional

Problem: The PFAB_CSR register time-out bit located at bit 28 does not get set on a time-out.

Implication: None

Workaround: None

Status: Fixed

27. Bus Number is not updated correctly in the PCI-X Status Register

Problem: The PCI-X Status Register at offset 0x0F4 bits[15:8] do not correctly update on a configuration write.

Implication: The 80314 cannot respond to split transactions when configured from behind another bridge.

Workaround: None

Status: Fixed

28. PCIXCAP[1:0] = 01b is not a valid setting

Problem: A PCIXCAP[1:0] setting of 01b selects the incorrect internal clock phasing on the 80314.

Implication: PCI-X 50–66 MHz is not a valid mode using A0 silicon.

Workaround: None

Status: Fixed

29. Clock synchronization issues

Problem: A0 silicon does not always correctly handle clock-boundary transitions between the various interfaces. Unpredictable behavior may result when data is transferred from one clock domain to the next when the clocks are not synchronized.

Implication: All clocks must originate from a single clock source, and the CIU clock and SFN domains must run at 100 MHz. For HBA designs, the SFN clock must be a multiple of the PCI input clock. For embedded designs, the PCI clocks can be derived from either the same source as the SFN clock, or from a clock output of the 80314.

Note: By design, 100 MHz PCI operation must always be driven by an external clock source, since in 100 MHz mode the PCI clock output of the 80314 is SFN clock/2.

Workaround: None

Status: Fixed

30. DMA channel hangs when it is stopped with STOP_REQ while CRC is enabled

Problem: The DMA channel hangs and the ACT bit remains asserted. No data is transferred.

Implication: None

Workaround: The channel can be reset and restarted without data impact, since the hang occurs only on the initial read of the CRC (no data is transferred prior to the hang). Alternately, the situation can be avoided by using the HALT_REQ bit instead of the STOP_REQ bit when utilizing the CRC functionality.

Status: No Fix

31. 5-volt tolerance

Problem: The 80314 is not 5-volt PCI tolerant.

Implication: Plugging the 80314 into a 33 MHz 5 V PCI bus draws excessive current, leading to damage and/or device failure.

Workaround: None. Do not design the 80314 into a 5 V bus/backplane. Also, do not connect 5-volt PCI devices to either of the FL PCI interfaces.

Status: No Fix

32. INT_PIN field PE_MISC2 00 for A0

Problem: The value of the PCI configuration register INT_PIN is 00 for the A-0 stepping and cannot be changed.

Implication: The 80314 does not have the ability to instruct the PCI configuration software to assign an interrupt.

Correct behavior would be as follows:

- IRP_CFG_CTRL[LOC_INT_DEST] = 2'b01 INT_PIN = 8'h01
- IRP_CFG_CTRL[LOC_INT_DEST] = 2'b00 INT_PIN = 8'h00

Workaround: Where host enumeration source code is available, either modify the PCI configuration software to recognize the 80314 and assign an interrupt without reading the INT_PIN register, or implement polling in the host driver.

Status: Fixed

33. Default SDRAM port arbitration setting can cause SFN starvation

Problem: The default setting 00b of the PORT_ARB field of the SD_CNTRL register can result in time-outs on the SFN side when the CIU side is accessing the memory with repeated small requests (cache off, coalescing disabled).

Implication: When the SFN side is starved of SDRAM access, the agent attempting accesses eventually times out.

Workaround: When using PORT_ARB = 00, ensure that the cache is on and coalescing on, or use one of the alternative PORT_ARB settings.

Status: No Fix

34. 80/20 port arbitration is not functional

Problem: The 10b setting of the PORT_ARB field of the SD_CNTRL register [9:8] does not function correctly. This setting provisions 80% memory bandwidth for CIU access and 20% for SFN access. This setting is now reserved.

Implication: Under heavy system loads, use of the 80/20 PORT_ARB setting may cause data corruption, and the system may hang.

Workaround: Use only PORT_ARB 00*, 01* or 11 settings for B1 stepping. Use only 01 setting for A0/B0 steppings.

Note: Refer to Errata 33 on the implication of using PORT_ARB = 00. Refer to Specification Clarification 17 on the implication of using PORT_ARB = 01.

Status: No Fix

35. Erroneous “undersize frame counter” increment

Problem: A Gigabit Ethernet under-run may result in an erroneous “undersize frame counter” increment. Under heavy SFN traffic, the MAC may empty the TX FIFO faster than it is able to be fed by the DMA/SFN. As a result, the transceiver is not kept busy, and a TX error condition is triggered (under-run). When an under-run occurs, the MAC deliberately sends a bad CRC to force the receiver to discard the packet, but the “CRC error bit” is not set and the frame size is zeroed. This causes the statistics unit to erroneously detect an “undersized frame” (0 bytes) with a good CRC(FSC). As a result, the TUND (Transmit Undersize) Frame Counter field of PE-MSTAT (Table 296) of the MAC increments (address F8/4F8).

Implication: The transmit undersize frame counter statistics counter is off by number of transmit under-run events that have occurred.

During heavy traffic conditions, any TX frame larger than 2K may under-run, including jumbo frames.

Occurrence of under-run is highly dependent on the application and data profile; many applications do not experience this error.

Workaround: To avoid under-run during heavy traffic conditions:

1. Use only frame sizes <= 2K, so they can be entirely buffered in TX FIFO.
2. Ensure entire frame is buffered in FIFO prior to the start of transmission by setting the “Start sending threshold” TX Thresholds register (Offset: 0x230/0x630) >= the frame size. See Table 376 of the *Intel® 80314 I/O Processor Companion Chip Developer’s Manual*.

Some applications can use frames larger than 2K without occurrence of over-run and incorrect incrementing of TUND.

Status: No Fix

36. I^2C hang condition

Problem: I^2C can lock up when a multi-byte read follows a time-out from a single-byte read.

Implication: I^2C hangs. The 80314 must be reset.

Workaround: Follow single-byte read time-outs with a single-byte read to a valid device.

Status: No Fix

37. Incorrect PME output signaling

Problem: PME pin signaling is implemented incorrectly such that P1_PME# and P2_PME# signals are incorrectly driven high in the active state. These pins must be open-drain bi-directional such that they are three-state inactive (pulled high by external pull-up) and driven low (active).

Implication: P1_PME# and P2_PME# signals cannot be driven low (active) and instead drive high (active).

Workaround: None

Status: Fixed

38. Testing SDRAM single-bit ECC errors with 64-bit writes

Problem: Single-bit error occurrences/corrections resulting from soft insertion of an ECC syndrome (to test ECC) are not reported as expected for 64-bit writes (with 64- or 32-bit reads) to un-cacheable/un-bufferable memory. The inserted error is detected and corrected properly, but the occurrence is not noted in the SD_ECC_STATUS nor the SD_ECC_ADDR1/SD_ECC_ADDR2 registers for 64-bit writes. 64-bit writes to un-cacheable/un-bufferable memory are split into two 32-bit read-modify-write (RMW) transactions. The first 32-bit RMW inserts the syndrome, the second RMW corrects it, but no corrected error is reported.

Implication: This behavior impacts only the testing of single-bit ECC errors for 64-bit writes (soft-inserted single-bit errors). The inserted error is detected and corrected properly but is not reported. Hard single-bit ECC errors are detected, corrected, and reported properly.

Workaround: Insertion/testing of single bit ECC errors must either:

1. Use cacheable/bufferable access
2. Use 32-bit accesses

Status: No Fix

39. INT_DIS read-only field prevents enabling INTx# assertion

Problem: Both the MWI_EN and INT_DIS bits must be read/write. The INT_DIS bit enables/disables the ability of the interface to assert INTx#. Since this bit is cleared by default and is read-only, you cannot write to the INT_DIS field to enable assertion of INTx#.

In Table 91 in Section 3.18.3.2 of the *Intel® 80314 I/O Processor Companion Chip Developer's Manual* (273756-002), the register drawing shows the following incorrect bit labels:

- The MWI_EN bit (bit[4]) is **read/write** but is documented as **read-only**.
- The INT_DIS bit (bit[10]) is **read-only** but is documented as **read/write**.

Implication: For the A0 stepping, you cannot write to the INT_DIS field to enable assertion of INTx#

Workaround: None

Status: Fixed

40. 80200 lockup for Port Arbitration settings 11

Problem: Concurrent Intel XScale® core and SFN SDRAM access within an approximately 4 KByte memory region can result in 80200 lockup for port arbitration settings 11.

Implication: A0/B0 steppings are restricted to using a PORT_ARB setting of 01*. This setting gives SDRAM priority to the SFN and may hold off Intel XScale® SDRAM accesses.

Workaround: Use only the 01 PORT_ARB settings for A0/B0 steppings. Use only 00*, 01*, 11 for B1 stepping.

Note: Refer to Specification Clarification 17 for the implication of using PORT_ARB = 0. Refer to Errata 33 on implications of using PORT_ARB = 00.

Status: Fixed

41. INTx_EN (x = A, B, C, D) bits of IRP_INTAD register do not function properly

Problem: Selective masking of INTA, INTB, INTC, and INTD by the IRP_INTAD register (offset 0x18C) does not function correctly, resulting in these interrupt sources being passed to the MPIC regardless of the state of the INTA_EN, INTB_EN, INTC_EN, INTD_EN bits of the IRP_INTAD register.

Implication: None

Workaround: With the fixing of Errata 24 (page 21), the P_INT field of the IRP_ENABLE register can be used to mask/unmask all four interrupts together. Each interrupt (INTA, INTB, INTC, INTD) can be individually masked and processed by the MPIC.

Status: No Fix

42. External PCI/X DMA to SDRAM Sync Packet

Problem: Sync packets from the PCI/X block do not function correctly and can lead to lockup and/or data corruption. Sync packets are intended primarily to ensure data integrity of the dual-ported SDRAM memory controller, specifically to ensure inbound data from the PCI/X block to the SDRAM is flushed from the SFN fabric to SDRAM before being accessed by the Intel XScale® core through the second memory port.

For more complete information on when sync packets are needed see section 4.2.6 of the *Intel® 80314 I/O Processor Companion Chip Developer's Manual* (273756). Also see the white paper entitled *Sync Packet Architectural Usage for the Intel® 80314 I/O Companion Chip* (302325).

Implication: Software semaphores must be used to ensure data has been completely transferred from the SFN fabric to memory before being accessed/manipulated by the Intel XScale® core through the second memory port. External DMA to SRAM is not allowed.

Workaround: None

Status: Fixed

43. Bit[0] of the Revision ID field of the PCI Class Override Register is stuck at 0

Problem: The Revision ID field (RID) of the PCI Class Register (0x008) can be overridden by writing the RID field of the PCI Class Override Register (0x1A0). Bit[0] is stuck at 0 and cannot be overridden.

Implication: The RID cannot be overridden with a value other than 0 in bit[0]. RID override is typically used only in a development environment.

Workaround: Override values of the RID must use values with 0 in bit[0].

Status: Fixed

44. GPIO[7:0] pins are driven on reset

Problem: The GPIO[7:0] signals are muxed with various UART signals and are driven outputs instead of inputs on reset (0x88h).

Implication: Systems can receive unexpected driven logic levels on GPIO[7:0] on reset. GPIO[7] and GPIO[3] are driven high while GPIO[6:4] and GPIO[2:0] are driven low. See Documentation Change 11 (Incorrect GPIO mappings for UART signals) on page 39 for correct UART/GPIO pin mappings.

Workaround: Systems wishing to use these pins as GPIO must isolate these pins from the reset of the system using a FET or other device until the boot code has properly configured the GPIO port. Typically the default state of one GPIO pin is used to control the FET gate for the other pins.

Status: No Fix

45. External PCI/X DMA to SRAM sync packet

Problem: Sync packets from the PCI/X block to SRAM do not function correctly and can lead to data corruption. During heavy fabric traffic, servicing of an external DMA interrupt can beat the actual inbound data. The sync packet in this case is intended to ensure that inbound external DMA data from the PCI/X block to the SRAM is flushed from the SFN fabric to SRAM before being accessed by the Intel XScale® core. For more complete information on when sync packets are needed, see Section 4.2.6 of the *Intel® 80314 I/O Processor Companion Chip Developer's Manual* (273756). Also see the white paper entitled *Sync Packet Architectural Usage for the Intel® 80314 I/O Processor Companion Chip* (302325).

Implication: Since the PCI/X to SRAM sync packet does not work properly, external DMA must transfer data only to/from SDRAM (PCI/X to SDRAM sync packets work).

Workaround: External DMA data to SDRAM only. Updates by external DMA engines to descriptors located in SRAM are allowable when access is coordinated by a semaphore type structure; in other words, a CPU descriptor processing thread must not process a descriptor unless it sees that the external DMA engine has set a "done" bit in the descriptor. Interrupt software, triggered by the external DMA, must check for the descriptor "done" type bit to be set and issue a PCI/X to SDRAM sync packet, before accessing the data in SDRAM.

Status: No Fix

46. Possible lost interrupt due to read/write of aliased IACKx registers

Problem: Read or write access to offsets 0x304, 0x344, 0x384, and 0x3C4 in the PCI, CIU, GigE, and DMA blocks are aliased to the MPIC IACKx registers 0x304, 0x344, 0x384, 0x3C4.

- PCI LUT registers overlap: 0x304, 0x344, 0x384, and 0x3C4
- CIU_SF_BAR1_LUTx registers overlap: 0x304, 0x344, 0x384, and 0x3C4
- GigE RXQ 0 Buf Cfg overlaps: 0x384
- DMA CH3_SRC_ADDR_L overlaps: 0x304
- DMA CH3_SRC1_ADDR_L overlaps: 0x344
- DMA CH3_SRC10_ADDR_L overlaps: 0x384

Implication: Unintended read or write access to the IACKx registers can cause an interrupt to be falsely acknowledged and/or lost.

Workaround: Only use DMA channel 3 for linked mode DMA/Memfill/XOR operation (direct mode not allowed). Do not modify the following registers after initial setup.

In general, the conflicts with PCI, CIU, and GigE are benign, since it is expected that the overlapping registers will not be modified after initial setup. The conflicting DMA registers are not used if "chained" DMA mode is used. Be advised that even in "chained" DMA/Memfill/XOR mode, a read or write of the ch3_src_addr_l, ch3_src1_addr_l, or ch3_src10_addr_l aliases to the MPIC IACKx registers. DMA channels 0, 1, and 2 have no restrictions.

Status: No Fix

Specification Changes

1. Intel® 80314 I/O Processor Companion Chip does not support transparent mode operation

Issue: Several critical issues have been identified with the 80314 PCI-X blocks configured in transparent mode. The 80314 does not support transparent modes of operation. The PCI-X blocks in the 80314 must be configured for embedded mode.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

2. SFN buffer sizes for PCI-X and SDRAM interfaces

Issue: Starting with the B0 stepping of the *Intel® 80314 I/O Processor Companion Chip*, the fabric buffer size in both the PCI-X and SDRAM interfaces is increased from 256 bytes to 1024 bytes (default). External storage traffic patterns from PCI-X to PCI-X or PCI-X to SDRAM can achieve higher throughput. The 1 K buffers are utilized only for transactions that are initiated on one of the PCI-X buses (PCI-X mode only). Configurations with PCI-initiated transactions must still use 256 bytes. Transactions initiated by all other sources (DMA, GigE, CIU) also use 256-byte packets.

A PCI configuration must disable 1 KByte packet use (use 256-byte packet size) by clearing bit[2] of the MISC_CSR (0x040). Bit[2] was previously reserved.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

3. Only two REQ/GNT pairs are available with the internal arbiter when the PCI-X interface is 100 MHz or greater

Issue: For A0, only two devices are supported on a PCI-X segment running at 100 MHz or greater. B0 and later silicon removes this restriction.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

4. This item has been corrected and removed from this specification update

5. CacheLineWrap mode is not supported

Issue: CacheLineWrap mode is not supported in the 80314.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

6. Additional nominal and maximum power data; correction of power dissipation values

Issue: Table 29 (in Section 4.1 of the *Intel® 80314 I/O Processor Companion Chip Datasheet)*, does not list nominal and maximum power consumption for each voltage rail. The following entries are to be added to Table 29:

Symbol	Parameter	Min.	Max.	Units	Notes
PVCC33	3.3 V supply power	756	1710	mW	
PVCC25	2.5 V supply power	270	609	mW	
PVCC12	1.2 V supply power	1430	1907	mW	

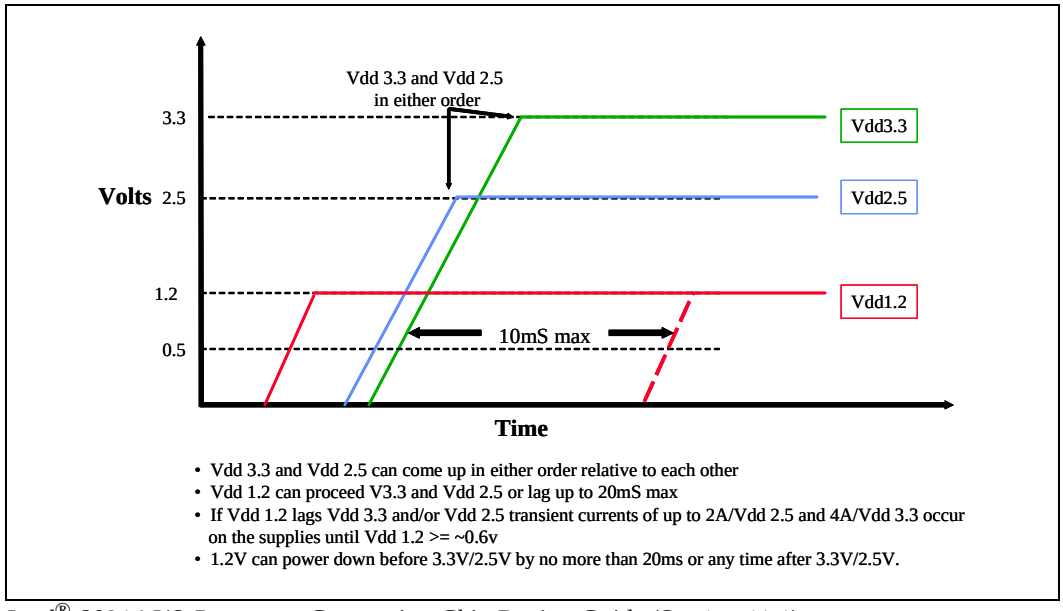
In addition, the power dissipation values in Table 22 must be updated from 2.4 typ./4.2 max. (predicted) to 2.456 typ./4.226 max. (actual).

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Datasheet*

7. Power-sequencing requirement

Issue: The power-up and power-down sequences of the 80314 1.2 V/2.5 V/3.3 V supply rails has been revised from version 003 and 004 of this specification update. The power sequencing requirements initially presented in version 003 were designed to avoid transient current draw that could appear on the 2.5 V/3.3 V supply rails. Further investigation has determined that no current transients occur when the 1.2 V supply is ramped first. In addition, it is acceptable to ramp the 1.2 V supply after the 2.5 V and 3.3 V supplies as long as the lag is less than or equal to 20 mS. When the 1.2 V rail lags the 2.5 V and/or 3.3 V rail, transient currents of up to 2 $A/V_{DD2.5}$ and 4 $A/V_{DD3.3}$ can occur on the supplies until $V_{DD1.2}$ >= ~0.6 V. The 1.2 V supply can power down no more than 20 ms before or any time after the 3.3 V/2.5 V supplies power down. These requirements are illustrated in Figure 1.

Figure 1. Power-Sequencing Requirements



Affected Docs: *Intel® 80314 I/O Processor Companion Chip Design Guide* (Section 11.1)
Intel® 80314 I/O Processor Companion Chip Datasheet

8. MPIC interrupt mapping change

Issue: The MPIC interrupt mapping of the Ethernet and UARTs was changed from the A0 to B0 stepping to provide separate interrupts for the UARTs and GigE ports. In addition, the B0 stepping maps only the Misc. interrupt to I2C. The output of the interrupt pending register (IPR) is an interrupt number permanently assigned to each interrupt source. The following entries from Table 461 of the *Intel® 80314 I/O Processor Companion Chip Design Guide* are to be changed from A0 to B0.

MPIC Interrupt Flag Number (Decimal)	Source	
	A0 (currently shown in the *Intel® 80314 I/O Processor Companion Chip Developer's Manual*)	B0
13	INT[13]	UART0
14	INT[14]	UART1
15	INT[15]	GigE Port 0
16	GigE (ports 0 and 1 combined)	GigE Port 1
21	Misc. (I2C, UART0, UART1 combined)	I2C

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

9. Input hold time on CPU interface

Issue: The current input hold time maximum specifications (T_{IH1} and T_{IH2}) for the CPU interface of the Intel® 80314 I/O Processor Companion Chip is 0.6 ns (see Table 38, "AC Specifications for Intel XScale® Microprocessor Interface" in section 4.4.5 of the datasheet). This specification is planned to be changed to 2.2 ns starting with the B1 stepping and is not expected to impact design guidelines.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Datasheet*

10. Reset slew rate for battery-backup entry

Issue: The slew rate for the assertion of reset (P1_RST#, P2_RST#, SFN_RST#) must be no slower than 20 nS/V when entering DDR battery-backup mode, so a reset slew-rate specification is being added:

Tsrst 20 nS/V maximum

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Design Guide*
Intel® 80314 I/O Processor Companion Chip Datasheet

11. Reset input hold time for HBA battery-backup entry

Issue: The PCI/X reset input hold time parameters for the 80314, Tih2 and Tih3, are being changed from 0 to -600 pS. This change is applicable only to the assertion edge when using reset to enter SDRAM standby mode.

In an HBA configuration, the host bus PCI/X reset (P1_RST# or P2_RST#) to the 80314 becomes the primary reset input to the 80314. In this configuration, SFN_RST# is no longer a reset input (disabled). During power failure, an HBA voltage monitor circuit must be able to assert the Px_RST# input pin to the 80314 to enter battery-backup mode. This must be done, however, without resetting the host bus. The isolation of the power-failure reset from the host bus can be achieved by inserting an OR gate between the host bus Px_RST# signal and the 80314 Px_RST# pin. Changing Tih2 and Tih3 to -600 pS enables selection of a gate to achieve this and still meet timing requirements for the PCI-X initialization sequence.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Design Guide*
Intel® 80314 I/O Processor Companion Chip Datasheet

12. Removal of shadow registers

Issue: Starting with the B0 stepping, the following shadow registers are de-featured:

- P_CSR_SHADOW
- P_MISC1_SHADOW
- P_MISC2_SHADOW
- SERR_STAT_SHADOW
- P_PCI/X_C_SHADOW
- P_PCI/X_S_SHADOW

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Design Guide*

13. Single Data Rate SDRAM is not supported

Issue: The 80314 memory controller supports Double Data Rate (DDR) SDRAM. Single Data Rate (SDR) SDRAM is not supported.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

Specification Clarifications

1. Byte swapping must be on data word-aligned boundaries

Issue: Performing byte swapping on data word-unaligned DMA transfers does not result in the correct swapping. Data integrity is lost when the byte-swapping capability of the DMA engines is used on data word-unaligned addresses. When the application in question requires byte swapping, consider having the initial DMA transfer the data with an offset so that the data that needs swapping ends up on a word-aligned address.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

2. MISC_CSR register SOFT_RESET not only asserts the Px_RST pin but also resets the PCI block

Issue: The SOFT_RESET bit in the MISC_CSR register (offset 0x040) not only asserts the Px_RST pin on the bus, but also resets the corresponding PCI block. PCI soft-resets are not possible without resetting the full corresponding PCI blocks.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

3. SD_BANK_CTRL register programming restrictions

Issue: ACT to PRECHARGE timing problem when a refresh occurs. With regard to the SD_BANK_CTRL register at offset 0x008, the sum of T_WR + T_RCD + 2 must be equal or greater than T_RAS.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

4. Multi-bit ECC error behaviors

Issue: When a multi-bit ECC error occurs in the second data phase of a burst write from the Intel XScale® processor into the 80314, the 80314 incorrectly forward the write to the destination. The correct function is to disable the byte enables when forwarding a write transaction where the ECC was detected. An interrupt is asserted upon detection of the ECC error. Target addresses meant to be overwritten with good data are overwritten with corrupt data. Firmware must be aware that upon an ECC error from an Intel XScale® processor write, the data is still written to the target

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

5. Requirements for booting to other than an 8-bit PBI width

Issue: The 80314 PBI width is 8 bits by default. In order to boot from devices wider than 8 bits, a PROM must be used on the I^2C bus to reconfigure the PBI width appropriately. When a design does not include the use of an I^2C EEPROM for some initial device configuration, an 8-bit flash device must be used.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

6. Time-outs may result in data overwrites

Issue: 17-bit timers are implemented to time-out SFN transactions that do not complete after a set period of time. When a completion does come back after the time-out has occurred, data for one transaction may overwrite another transaction. Transactions must not time-out beyond the range of a 17-bit timer when the system is correctly configured. When these large time-outs occur, the system-level issue must be addressed. When the timers cause problems, the PCI SFN timers can be disabled.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

7. The Intel® 80314 I/O Processor Companion Chip configuration retry mechanism requires the use of SEEROM

Issue: There are two issues with the LOCKOUT bit functionality (bit 7 of the MISC_CSR register):

- Setting the bit does not retry configuration cycles.
- The default value is 0 instead of 1.

The implication of not retrying configuration cycles is that, when used on an HBA, a host may read PCI resource requirements before the 80314 has programmed the P2S_PAGE_SIZES register. The implication of the default value being set to 0 is that a host may attempt to configure the 80314 before firmware has changed this value to 1.

When the I^2C/SEEPROM state machine is programming the 80314 register values, all cycles including configuration cycles are retried. Therefore, using the SEEPROM, it is possible to change both the default value of the lockout bit as well as program the 80314 resource requirements (P2S_PAGE_SIZES).

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

8. Intel® 80314 I/O Processor Companion Chip is capable of up to 12 GB but tested only to 3 GB

Issue: The 80314 is logically capable of supporting up to 12 GB memory but at this time has been validated only up to 3 GB (3 × 1 GB DIMM).

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

9. Maximum I^2C memory

Issue: The maximum supported size for data in EEPROM is 255 bytes (byte count field 0x00FE).

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

10. Proper handling of Gigabit Ethernet WAIT condition

Issue: Heavy Ethernet and SFN traffic resulting in slow interrupt response and/or insufficient data buffer capacity may fail to free up Gigabit Ethernet RX buffers (receive queue) fast enough, triggering a WAIT condition (data in FIFO but no buffers available). Use of the Abort function (ABT) from within a WAIT service routine to flush the full or partial frame from the RX FIFO is not recommended. Using this method to service a WAIT condition can corrupt the descriptor status and data buffer contents. The recommended method to service a WAIT condition is for the WAIT service routine to provide additional empty data buffers in the receive queue before re-enabling the queue, thereby allowing the RX DMA to complete the transfer of the frame into memory.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

11. Proper handling of multi-bit ECC errors in abort handler

Issue: Incorrect handling of multi-bit ECC errors within the abort handler, for 64-bit read accesses to un-cacheable/un-bufferable memory, can result in multiple data aborts and an invalid link register leading to CPU crash. For this type of access, the Intel® 80200 issues two 32-bit RMW cycles. When multi-bit ECC errors occur, two back-to-back ECC syndromes are presented to the Intel XScale® bus, resulting in two aborts and triggering an existing Intel® 80200 errata.

To detect this condition and handle it properly, the abort handler must check to see whether the link register contains 0x14 or points elsewhere. When the link register points to 0x14, this indicates that the back-to-back abort condition has been triggered. When it points elsewhere, this condition is not triggered.

For the most up-to-date workaround information, refer to errata #2, “Multiple ECC errors reported on a single transaction” in the *Intel® 80200 Processor based on Intel XScale® Microarchitecture Specification Update* (document number 273415).

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer’s Manual*

12. Enabling ECC/parity for SRAM

Issue: When the proper SRAM initialization sequence is not followed when enabling ECC and parity, multi-bit ECC errors and parity errors are generated. This can occur when writing 4-byte words because the CIU unit does a read-modify-write. During the read, the CIU checks the SRAM content against parity that has not yet been initialized, and thus reports an error.

The proper sequence is as follows:

1. Write 0x4 to CIU_CFG register (offset 0x38) to enable parity.
2. Write to every 4-byte word in SRAM—expect a parity error in CIU_ERROR (offset 0x48)
3. Write 0x20 to the CIU_ERROR register to clear the parity error.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer’s Manual*

13. 64-bit PCI/X addressability

Issue: Current documentation leads the reader to believe that the PFAB_BAR’s must be enabled for all SFN→PCI/X traffic and are therefore restricted to 5 GB of addressability (PFAB_MEM32 1 G + PFAB_PFM3 2 G + PFAB_PFM4 2 G).

An outbound SFN transaction routed to a PCI/X port that is not claimed by a PFABx BAR is passed through untranslated. Thus, where address translation is not required, 64 bits of PCI/X addressability is available through port routing. This provides 64-bit PCI/X addressability to SFN sources such as the CIU and DMA. One implication is that the DMA destination port can conveniently be used to direct DMA to PCI/X transfers to PCI1 or PCI2 memory space.

It is important to remember that PCI/X memory access directly from the Intel XScale® processor (without DMA/XOR, 32-bit addresses) still needs a configured CIU BAR (and its LUT) to route the access through to the desired PCI/X port with the correct translated address.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer’s Manual*

14. Reset of Intel® 80314 I/O Processor Companion Chip primary PCI/X without host PCI/X reset

Issue: When configured for a host bus adaptor (HBA) application, resetting only the primary PCI/X interface of the 80314 without resetting the entire host PCI/X bus can cause several issues, including but not limited to high current draw and loss of proper PCI/X mode and frequency by the 80314.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

15. PCI/X cannot be the destination of a sync packet

Issue: Current documentation does not make it clear that the PCI/X block must not be the destination (second specified port) of a sync packet; otherwise, the 80314 can behave incorrectly. Due to PCI/X strict ordering rules, the sync packet is not required for the PCI/X block (write always completes before a subsequent read).

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

16. SRAM enable/disable pin

Issue: The SRAM_SKU pin (AW33, previously listed as NC) is an input-only pin with an internal pull-up. When this pin is tied low, the SDRAM inside the 80314 is inaccessible. When this pin is left floating, the SRAM is accessible. "No SRAM" skew parts must tie this pin low. When this pin is left floating, the device ID incorrectly indicates that SDRAM is usable.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*
Intel® 80314 I/O Processor Companion Chip Datasheet

17. Driver consideration for shared memory structures under PORT_ARB = 01

Issue: Due to the dual-ported memory controller of the Intel® 80314 I/O Processor Companion Chip, care must be taken to ensure sequence-dependent writes occur in order. For example, consider the case where an Intel XScale® write to a PCI/X SDRAM NIC descriptor (descriptor command setup) is followed by an Intel XScale® write to the PCI/X NIC device to append the new descriptor to the tail of the descriptor chain. A system configured with the PORT_ARB = 01setting gives priority to the fabric over the CPU. Due to this setting, under heavy fabric traffic, the CPU access to the SDRAM can be held off in favor of fabric access to the SDRAM. The unintended result is that the write to the NIC (over fabric) competes before the descriptor write to SDRAM. This signals the NIC to start processing (read descriptor from SDRAM) before the descriptor setup write from the CPU occurs.

The solution for PORT_ARB = 01 mode involves inserting a read between the SDRAM write and the PCI/X agent writes. This works because ordering rules require posted writes to complete before reads, and the Intel XScale® port stalls until the read returns from SDRAM, so the write to the NIC is delayed. Be careful that the read is to uncacheable/unbufferable SDRAM, so that the Intel XScale® port is forced to fetch data from SDRAM.

This is not an issue for the PORT_ARB = 00 setting because the Intel XScale® port has priority access to the SDRAM over the fabric, thus ensuring that the Intel XScale® write to SDRAM completes before the PCI/X NIC write

This issue does not effect PORT_ARB = 11.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

18. PCI Target Abort when Start Address + Cache Line exceeds physical memory

Issue: When the PCI interface is the target of a “Memory Read Multiple” (MRM) command from a bus master, target aborts can occur when the start address plus the cache-line size exceeds the end of physical memory. This can occur when the bus master is attempting to read the last few words of memory. The memory controller fetches cacheline-sized chunks of memory from the memory controller. A fetch near to the end, but within valid physical memory, can cause a portion of the fetched chunk to be requested beyond physical memory. When this happens, the PCI interface signals Target Abort.

This behavior can be avoided by reserving the last page of physical RAM for uses other than PCI DMA. Some OS implementations simply set the OS managed memory size to one less than the maximum memory discovered.

This behavior does not apply to operation in PCI-X mode.

Host address map / BAR settings for the Intel® 80314 I/O Processor Companion Chip in the embedded HBA configuration must not hit the end of physical memory. Inbound transactions are expected to be comprised of mainly command and status operations, with host data transfers being handled through the internal DMA of the Intel® 80314 I/O Processor Companion Chip.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer’s Manual*

Documentation Changes

1. PCI-X Bridge Status Register (Embedded Mode) (PE_PCI/X _S) has incorrect values for default bus and function numbers

Issue: In Section 3.18.4.23, Table 129 shows bus and function numbers for this register with values of 0x00 and 111b respectively. The correct default values are 0xff and 0x0 respectively.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

2. PFAB_CSR Register is described incorrectly

Issue: In Section 3.18.5.20, Table 152, the behavior of the SW_RST bit (bit[8]) is incorrectly documented. The bit does not affect all registers as indicated. The correct behavior for this bit is to flush the Switch Fabric Network (SFN) buffers.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

3. Removed and moved to Errata #39

4. Various attribute bits are not correct

Issue: The following bits are not documented correctly:

- The attributes of bits[15:8] at offset 0x3C of the PCI configuration space are documented as **read-only**. They should be **read/write**.
- The attributes of bit[24] at offset 0xE0 of the PCI configuration space are documented as **read/write.** They should be **read-only**.
- Bits[15:0] at offset 0xE4 of the PCI configuration space are read-only but can be cleared by writing all 1s.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

5. I2C_RD_DATA Register defines incorrect byte order

Issue: In Section 9.7.4, Table 448, the I2C_RD_DATA must be defined as follows:

Bits[31:24]—Received I^2C data, byte 0
Bits[23:16]—Received I^2C data, byte 1
Bits[15:8]—Received I^2C data, byte 2
Bits[7:1]—Received I^2C data, byte 3

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

6. GPIO offset is not correct

Issue: The *Intel® 80314 I/O Processor Companion Chip Developer's Manual* incorrectly lists the following:

- GPIO Data Register offset is documented as 0x5A0 (Table 458). It should be 0xA0.
- GPIO Control Register offset is documented as 0x5A4 (Table 459). It should 0xA4.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

7. Various ball map diagram signals are not correct

Issue: In section 3.1.18, Figure 3, the following ball labels are incorrect:

- C12 is documented as SD_DQS[35]. It should be SD_DQ[35].
- C14 is documented as SD_DQ[14]. It should be SD_DQS[14].
- C16 and C17 are both documented as SD_DQ[37]. C16 should be SD_DQ[37], and C17 should be SD_DQ[32].
- AU33 is documented as NT[6]. It should be INT[6].

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Datasheet* (273757-001)

8. SDRAM feedback clock length

Issue: The note in Section 7.3 (bottom of page 54) specifies to design the SD_CKFBI trace length to match the average clock length plus the average DQS length. The SD_CKFBI trace should be 3 inches.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Design Guide* (273758-001)

9. PCI Interrupt Assertion register IRP_PIA added

Issue: Current documentation omits a register required to interrupt the host in a host bus adaptor configuration. The register described below is now a valid register of the PCI/X block (offset 0x190) and is present in all steppings. For further information on the use of this register for host messaging and interrupts, refer to the application note, *Host Bus Adapter Considerations with the Intel® 80314 I/O Processor Companion Chip* (order number 274048).

IRP_PIA (PCI Interrupt Assertion)
Register Offset: 0x190

Bit	Default	Description
31:29	–	Reserved
28	0	Writing a 1 asserts PCI interrupt INTA. Clearing the bit de-asserts the interrupt. Note the following requirements for this bit to function: • The PCI block must be configured with RST_DIR = 0 • IRP_CFG_CTL (0x180) INTA_TYPE field must be 01b • IRP_CFG_CTL (0x180) LOC_INT_DEST must be 01b • IRP_CFG_CTL (0x180) INTA_DIR must be 1b
27:0	–	Reserved

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

10. PFAB_MEM32[11:0] field description should be reserved

Issue: In Section 3.18.5.25, Table 157, bit field [11:0] of the PFAB_MEM32 register should be reserved.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

11. Incorrect GPIO mappings for UART signals

Issue: The *Intel® 80314 I/O Processor Companion Chip Datasheet* GPIO mappings for UART signals are incorrect in both the "Pin Name" and "Description" columns.

The following entries of Table 13 (Section 3.1.11 in the datasheet) should be corrected as follows (in both the "Pin Name" and "Description" columns):

Change This…	To This…
U0_DSR# GPIO[0]	U0_DSR# GPIO[6]
U0_DTR#/ GPIO[1]	U0_DTR# GPIO[7]
U0_DCD# GPIO[2]	U0_DCD# GPIO[4]
U0_RI# GPIO[3]	U0_RI# GPIO[5]
U1_DSR# GPIO[4]	U1_DSR# GPIO[2]
U1_DTR# GPIO[5]	U1_DTR# GPIO[3]
U1_DCD# GPIO[6]	U1_DCD# GPIO[0]
U1_RI# GPIO[7]	U1_RI# GPIO[1]

The *Intel® 80314 I/O Processor Companion Chip Developer's Manual* refers to UARTs 1 and 2, while the datasheet refers to UARTs 0 and 1. Thus, the UART signals in the *Intel® 80314 I/O Processor Companion Chip Developer's Manual* (in bit 0 of Table 459, "GPIO Control (GPIO_CNTRL)", in Section 11.4) should be re-labeled as follows (in both the "Pin Name" and "Description" columns):

Change This…	To This…
U1_DTR	U0_DTR# GPIO[7]
U1_DSR	U0_DSR# GPIO[6]
U1_RI	U0_RI# GPIO[5]
U1_DCD	U0_DCD# GPIO[4]
U2_DTR	U1_DTR# GPIO[3]
U2_DSR	U1_DSR# GPIO[2]
U2_RI	U1_RI# GPIO[1]
U2_DCD	U1_DCD# GPIO[0]
The bits are mapped as: GPIO_DATA_IN[7:0] = [U1_(DTR,DSR,RI,DCD), U2_(DTR,DSR,RI,DCD)]	The bits are mapped as: GPIO_DATA_IN[7:0] = [U0_(DTR#, DSR#, RI#, DCD#), U1_DTR#, DSR#, RI#, DCD#)]

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual* (273756-002)
Intel® 80314 I/O Processor Companion Chip Datasheet (273757-001)

12. I²C capability wording

Issue: The wording of the I²C capability is unclear. The text from Section 1.1 must be changed.

Currently incorrect:

> Two I²C two-wire interfaces for initial configuration, saving vital product data, and reading memory configuration

Must be changed to the following:

> Two I²C two-wire interfaces for initial configuration and reading memory configuration

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual* (273756-002)

13. PCI/X initialization sequence

Issue: The frequency tolerances listed in Table 46 in the *Intel® 80314 I/O Processor Companion Chip Developer's Manual* (Section 3.11.1) are misleading, resulting in an incorrect PCI/X CAP#[1,0] selection for the desired initialization sequence. For example, Px_RSTDIR = 1 and PCI/X CAP#[1,1] cause the PCI-X 133 MHz initialization sequence to be driven by the 80314. Thus, a device expecting 100 MHz operation with PCI/X CAP#[1,1] receives the incorrect initialization sequence (PCI/X 133).

The proper PCI/X CAP# selection for 100 MHz PCI/X operation is PCI/X CAP#[1,0]. Note that external clocking is recommended for 100 MHz PCI/X operation since the PCI/X CAP#[1,0] setting causes the 80314 to drive its Px_CLK_OUT at SFN_CLK/2.

A new heading, "PCI/X Init. Pattern", must be added to Table 46 to aid in proper PCI/X CAP# selection:

Table 46. PCI/X CAP#[0,1] Encoding When Px_RSTDIR = 1

PCI/X CAP#[1]	PCI/X CAP#[0]	PCI Speed Range	PCI/X Init. Pattern
1	1	PCI-X 100–133 MHz	PCI-X 133
1	0	PCI-X 66–100 MHz†	PCI-X 100
0	1	PCI-X 50–66 MHz	PCI-X 66
0	0	PCI 33–66 MHz **Note:** For PCI devices, this speed setting is set by the M66EN pin.	PCI 33-66MHz

NOTE:

† When the PCI/X CAP value is 10b, the Intel® 80314 I/O Processor Companion Chip drives the SFN_CLK divided by two.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

14. Signal Listing Corrections

Issue: Incorrect signal listings are given in Section 3.1.18 of the *Intel® 80314 I/O Processor Companion Chip Datasheet*, Figures 3 and 4, Tables 20 and 21:

- In Table 21, “1025-Lead HSBGA Package”, the Alphabetical Signal Listing has some incorrect entries:
  - — Page 56—AN29 is documented as VCC_PC. It should be VCC_CORE.
  - — Page 56—Signals AP29, AP30, AP31 are missing from the table (VCC_PC type signals).
  - — Page 56—AN30 and AN31 are listed twice in the table; duplicates should be removed.
- In Table 20, “1025-Lead HSBGA Package”, the Alphabetical Ball Listing has some incorrect entries:
  - — Page 46—Remove AB2 VSS_CORE and add AB22 VSS_CORE.
  - — Page 48—Change AL33 entry from VCC_XS to VCC_PC.
- In Figures 3 and 4, the Ball Map has incorrect labels:
  - — The following active-low signals are improperly labelled (need “#” symbol to indicate active low) or are inconsistent (some signals used “_B” instead of “#” to indicate active-low; need to use “#”):

    A35, A36, A37, B21, B23, B24, B33, D34, F35, F37, G35, J36, K35, AA3, AU39, AD5, AC3, AE4, AR3, AR9, AR27, AR36, AR37, AT24, AT25, AT26, AT27, AT37, AT38, AT39, AP24, AP25, AP37, AF3, AF5, AN34, AN36, AG3, AC34, AM34, AM35, AV7, AV24
  - — The following signal names are incorrect:

    AV32 PWRUP_P1YP should be PWRUP_P1_BYP.

    M33 XS_DUMMY should be NC_M33.

    K38 XS_C_CK should be XS_CLK.

    F38 PBI_AD[20] should be PBI_RW.

    E20 SD_ECC_DM[1] should be SD_ECC[1].

    D3 E0_PCRS_SD should be E0_PCRS_SDET.

    AU36 PWRUP_P2YP should be PWRUP_P2_BYP.

    AH35 XS_A[14] should be XS_A[11].

Note the following potential problems that might result from using the incorrect information described above:

- A design based on Table 21 with AN29 connected to VCC_PC instead of VCC_CORE causes a short between VCC_PC and VCC_CORE supplies.
- A design based on Figures 3 and 4 with F38 connected to PBI_AD[20] instead of PBI_RW results in a non-functional PBI bus.
- A design based on Figures 3 and 4 with AH35 connected to XS_A[14] instead of XS_A[11] results in incorrect address mapping/operation on the processor bus.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Datasheet*

15. SDRAM PLL bypass

Issue: The “Description” column for SD_I2C_SDA (Table 5) incorrectly states that it can be used to enter “SDRAM PLL Bypass Mode”. Only the XS__FIQ[1]/PWRUP_SD_BYP pin can enter SDRAM PLL bypass mode.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Datasheet*

16. PWRDELAY circuitry not required for non-battery-backup designs

Issue: Section 7.5.3 of the *Intel® 80314 I/O Processor Companion Chip Design Guide* incorrectly states that applications that do not use battery backup still need to implement the PWRDELAY circuitry.

When no battery backup is required, the PWRDELAY pin can be tied to ground.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Design Guide*

17. Design guideline table missing data

Issue: Table 14 of the embedded 100 MHz design guidelines is missing lengths (listed as N/A) for the upper AD bus bits for the W4 and W5 segments. The W4 and W5 segments for the upper address lines have a minimum length of 1.65" and a maximum length of 3.5".

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Design Guide*

18. GPIO attribute reversal

Issue: Table 458 of the *Intel® 80314 I/O Processor Companion Chip Developer’s Manual* incorrectly reverses the attributes for bits[15:8] and bits[31:24] of the GPIO_DATA register (0x5A0). The correct attributes for bits[15:8] are RW, and the correct attributes for bits[31:24] are RO.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer’s Manual*

19. Single Data Rate SDRAM is not supported

Issue: The *Intel® 80314 I/O Processor Companion Chip Developer’s Manual* incorrectly states that the 80314 memory controller supports Single (SDR) and Double Data Rate (DDR) SDRAM. DDR SDRAM is supported; SDR is not supported.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer’s Manual*

20. EE_Bx_ADDR Register Bit [31:8] description is not correct

Issue: The *Intel® 80314 I/O Processor Companion Chip Developer’s Manual* incorrectly defines the EE_Bx_ADDR Register bit [31:8] description in Section 7.7.1 as A[31:12]. The correct description is A[35:12]

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer’s Manual*

21. Section 2.3.1.3 and 2.3.1.4 not correct

Issue: For Sections 2.3.1.3 and 2.3.1.4, the titles are reversed and are incorrect. The new section titles appear as follows:

2.3.1.3 Scenario S3: Internal DMA (Any Source, Any Destination)

For all scenarios involving internal DMA engines, the interrupt is not raised until the data has been enqueued to the SFN fabric. This means that the only requirement is to ensure that the data from the DMA transaction has been flushed from the receiving port’s queue. Sync packets are not used in this scenario. For example, if internal DMA is used to move data from a PCI/X port to SDRAM

or SRAM, a fabric-read to the memory (through the SFN fabric) is sufficient to flush the receiving port's queue. Ensure that the read actually goes through the SFN port to the memory instead of the Intel XScale® CPU's port to the memory.

2.3.1.4 Scenario S4: HBA Host Read/Write PCI/X to PCI/X with External DMA

The S4 case occurs in an HBA configuration when the host processor on one PCI/X bus, for example PCIX(1), makes a request for the Intel XScale® CPU to set up an external DMA transfer from PCI/X (2) to PCI/X(1). Direct PCI/X(1) requests to PCI/X(2) for a PCI/X(2)-to-PCI/X(1) DMA transfer are not allowed in embedded mode.

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

22. Table 12 not correct

Issue: Entries in Table 12 are incorrect. The new table appears as follows:

Table 12: Sync Packet versus Fabric Read Cases

CaseLabel	Case Description	How to handle
S1	PCI/X External DMA to SDRAM	Sync Packet
S2	External DMA on PCI/X writing to SRAM	No sync packet, no fabric read Descriptor based access control only Interrupt driven data access not allowed
S3	Internal DMA (any source/any destination)	Fabric Read
S4	HBA PC1(2) (host) Read/Write to PCI2(1) through external DMA	Non-destructive fabric read to downstream PCI/X adaptor device OR use S1 method, that is, DMA to SDRAM.*
S5a	Integrated GigE with descriptor in SRAM and data in SRAM	No sync packet or fabric read required (GigE automatically flushes data before updating descriptor)
S5b	Integrated GigE with descriptor in SRAM and data in SDRAM	Fabric Read (CPU to SDRAM)

* Please refer to Specification Clarification #15 in the *Intel® 80314 I/O Processor Companion Chip Specification Update*. PCIX cannot be the destination (second destination port) of a sync packet

Affected Docs: *Intel® 80314 I/O Processor Companion Chip Developer's Manual*

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