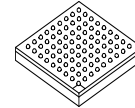




# MC9328MXS



**Package Information**  
Plastic Package  
Case 1304B-01  
(MAPBGA-225)

### Ordering Information

See [Table 1 on page 3](#)

# MC9328MXS

## 1 Introduction

The i.MX Family of applications processors provides a leap in performance with an ARM9™ microprocessor core and highly integrated system functions. The i.MX family specifically addresses the requirements of the personal, portable product market by providing intelligent integrated peripherals, an advanced processor core, and power management capabilities.

The MC9328MXS (i.MXS) processor features the advanced and power-efficient ARM920T™ core that operates at speeds up to 100 MHz. Integrated modules, which include a USB device and an LCD controller, support a suite of peripherals to enhance portable products. It is packaged in a 225-contact MAPBGA package. [Figure 1](#) shows the functional block diagram of the i.MXS processor.

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Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: i.MXS Product Family

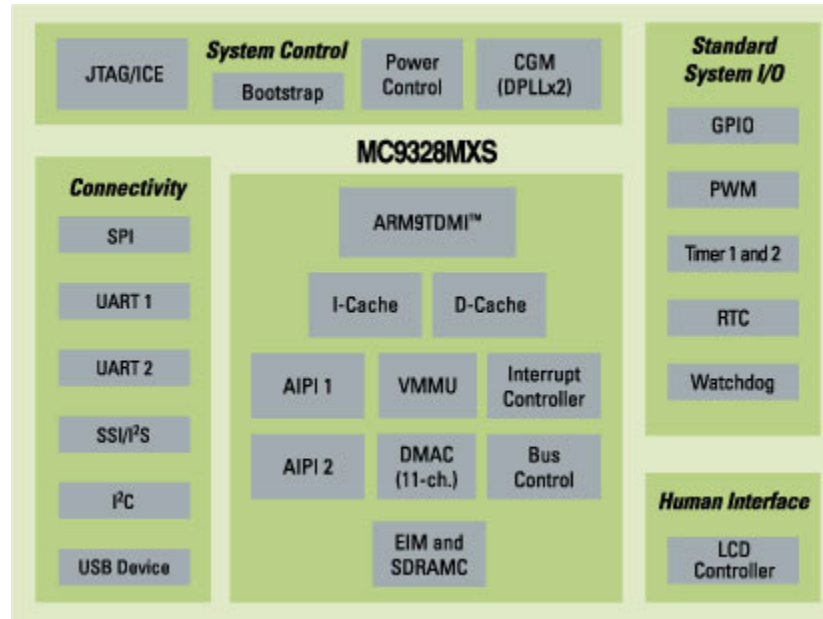


Figure 1. i.MXS Functional Block Diagram

## 1.1 Features

To support a wide variety of applications, the processor offers a robust array of features, including the following:

- ARM920T™ Microprocessor Core
- AHB to IP Bus Interfaces (APIs)
- External Interface Module (EIM)
- SDRAM Controller (SDRAMC)
- DPLL Clock and Power Control Module
- Two Universal Asynchronous Receiver/Transmitters (UART 1 and UART 2)
- Serial Peripheral Interface (SPI)
- Two General-Purpose 32-bit Counters/Timers
- Watchdog Timer
- Real-Time Clock/Sampling Timer (RTC)
- LCD Controller (LCDC)
- Pulse-Width Modulation (PWM) Module
- Universal Serial Bus (USB) Device
- Direct Memory Access Controller (DMAC)
- Synchronous Serial Interface and an Inter-IC Sound (SSI/I<sup>2</sup>S) Module
- Inter-IC (I<sup>2</sup>C) Bus Module
- General-Purpose I/O (GPIO) Ports
- Bootstrap Mode

- Power Management Features
- Operating Voltage Range: 1.7 V to 1.9 V core, 1.7 V to 3.3 V I/O
- 225-contact MAPBGA Package

## 1.2 Target Applications

The i.MXS applications processor is designed to meet the needs of medical instrumentation, low-end PDAs, point-of-sale terminals, security systems and other applications requiring a basic device based on ARM technology with support for open operating systems. Like other members of the i.MX family, the i.MXS is designed for high performance and low-power to maximize battery life.

## 1.3 Ordering Information

Table 1 provides ordering information.

Table 1. i.MXS Ordering Information

| Package Type       | Frequency | Temperature   | Solderball Type | Order Number       |
|--------------------|-----------|---------------|-----------------|--------------------|
| 225-contact MAPBGA | 100 MHz   | 0°C to 70°C   | Pb-free         | MC9328MXSVP10(R2)  |
|                    |           | -40°C to 85°C | Pb-free         | MC9328MXSCVP10(R2) |

## 1.4 Conventions

This document uses the following conventions:

- $\overline{\text{OVERBAR}}$  is used to indicate a signal that is active when pulled low: for example,  $\overline{\text{RESET}}$ .
- *Logic level one* is a voltage that corresponds to Boolean true (1) state.
- *Logic level zero* is a voltage that corresponds to Boolean false (0) state.
- To *set* a bit or bits means to establish logic level one.
- To *clear* a bit or bits means to establish logic level zero.
- A *signal* is an electronic construct whose state conveys or changes in state convey information.
- A *pin* is an external physical connection. The same pin can be used to connect a number of signals.
- *Asserted* means that a discrete signal is in active logic state.
  - *Active low* signals change from logic level one to logic level zero.
  - *Active high* signals change from logic level zero to logic level one.
- *Negated* means that an asserted discrete signal changes logic state.
  - *Active low* signals change from logic level zero to logic level one.
  - *Active high* signals change from logic level one to logic level zero.
- LSB means *least significant bit* or *bits*, and MSB means *most significant bit* or *bits*. References to low and high bytes or words are spelled out.
- Numbers preceded by a percent sign (%) are binary. Numbers preceded by a dollar sign (\$) or  $0x$  are hexadecimal.

## 2 Signals and Connections

Table 2 identifies and describes the i.MXS processor signals that are assigned to package pins. The signals are grouped by the internal module that they are connected to.

**Table 2. i.MXS Signal Descriptions**

| Signal Name                           | Function/Notes  |
|---------------------------------------|---|
| <b>External Bus/Chip-Select (EIM)</b> |   |
| A[24:0]                               | Address bus signals   |
| D[31:0]                               | Data bus signals  |
| $\overline{EB0}$                      | MSB Byte Strobe—Active low external enable byte signal that controls D [31:24].   |
| $\overline{EB1}$                      | Byte Strobe—Active low external enable byte signal that controls D [23:16].   |
| $\overline{EB2}$                      | Byte Strobe—Active low external enable byte signal that controls D [15:8].  |
| $\overline{EB3}$                      | LSB Byte Strobe—Active low external enable byte signal that controls D [7:0].   |
| $\overline{OE}$                       | Memory Output Enable—Active low output enables external data bus.   |
| $\overline{CS}$ [5:0]                 | Chip-Select—The chip-select signals $\overline{CS}$ [3:2] are multiplexed with $\overline{CSD}$ [1:0] and are selected by the Function Multiplexing Control Register (FMCR). By default $\overline{CSD}$ [1:0] is selected.   |
| $\overline{ECB}$                      | Active low input signal sent by a flash device to the EIM whenever the flash device must terminate an on-going burst sequence and initiate a new (long first access) burst sequence.  |
| $\overline{LBA}$                      | Active low signal sent by a flash device causing the external burst device to latch the starting burst address.   |
| BCLK (burst clock)                    | Clock signal sent to external synchronous memories (such as burst flash) during burst mode.   |
| $\overline{RW}$                       | $\overline{RW}$ signal—Indicates whether external access is a read (high) or write (low) cycle. Used as a $\overline{WE}$ input signal by external DRAM.  |
| $\overline{DTACK}$                    | $\overline{DTACK}$ signal—The external input data acknowledge signal. When using the external $\overline{DTACK}$ signal as a data acknowledge signal, the bus time-out monitor generates a bus error when a bus cycle is not terminated by the external $\overline{DTACK}$ signal after 1022 clock counts have elapsed. |
| <b>Bootstrap</b>                      |   |
| BOOT [3:0]                            | System Boot Mode Select—The operational system boot mode of the i.MXS processor upon system reset is determined by the settings of these pins.  |
| <b>SDRAM Controller</b>               |   |
| SDBA [4:0]                            | SDRAM non-interleave mode bank address multiplexed with address signals A [15:11]. These signals are logically equivalent to core address p_addr [25:21] in SDRAM cycles.   |
| SDIBA [3:0]                           | SDRAM interleave addressing mode bank address multiplexed with address signals A [19:16]. These signals are logically equivalent to core address p_addr [12:9] in SDRAM cycles.   |
| MA [11:10]                            | SDRAM address signals   |
| MA [9:0]                              | SDRAM address signals which are multiplexed with address signals A [10:1]. MA [9:0] are selected on SDRAM cycles.   |
| DQM [3:0]                             | SDRAM data enable   |
| $\overline{CSD0}$                     | SDRAM Chip-select signal which is multiplexed with the $\overline{CS2}$ signal. These two signals are selectable by programming the system control register.  |

Table 2. i.MXS Signal Descriptions (Continued)

| Signal Name                    | Function/Notes   |
|--------------------------------|--|
| $\overline{\text{CSD1}}$       | SDRAM Chip-select signal which is multiplexed with $\overline{\text{CS3}}$ signal. These two signals are selectable by programming the system control register. By default, $\overline{\text{CSD1}}$ is selected, so it can be used as boot chip-select by properly configuring BOOT [3:0] input pins.   |
| $\overline{\text{RAS}}$        | SDRAM Row Address Select signal  |
| $\overline{\text{CAS}}$        | SDRAM Column Address Select signal   |
| $\overline{\text{SDWE}}$       | SDRAM Write Enable signal  |
| SDCKE0                         | SDRAM Clock Enable 0   |
| SDCKE1                         | SDRAM Clock Enable 1   |
| SDCLK                          | SDRAM Clock  |
| $\overline{\text{RESET\_SF}}$  | Not Used   |
| <b>Clocks and Resets</b>       |  |
| EXTAL16M                       | Crystal input (4 MHz to 16 MHz), or a 16 MHz oscillator input when the internal oscillator circuit is shut down.   |
| XTAL16M                        | Crystal output   |
| EXTAL32K                       | 32 kHz crystal input   |
| XTAL32K                        | 32 kHz crystal output  |
| CLKO                           | Clock Out signal selected from internal clock signals.   |
| $\overline{\text{RESET\_IN}}$  | Master Reset—External active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module and the clock control module) are reset.   |
| $\overline{\text{RESET\_OUT}}$ | Reset Out—Internal active low output signal from the Watchdog Timer module and is asserted from the following sources: Power-on reset, External reset ( $\overline{\text{RESET\_IN}}$ ), and Watchdog time-out.  |
| POR                            | Power On Reset—Internal active high Schmitt trigger input signal. The POR signal is normally generated by an external RC circuit designed to detect a power-up event.  |
| <b>JTAG</b>                    |  |
| $\overline{\text{TRST}}$       | Test Reset Pin—External active low signal used to asynchronously initialize the JTAG controller.   |
| $\overline{\text{TDO}}$        | Serial Output for test instructions and data. Changes on the falling edge of TCK.  |
| TDI                            | Serial Input for test instructions and data. Sampled on the rising edge of TCK.  |
| TCK                            | Test Clock to synchronize test logic and control register access through the JTAG port.  |
| TMS                            | Test Mode Select to sequence the JTAG test controller's state machine. Sampled on the rising edge of TCK.  |
| <b>DMA</b>                     |  |
| $\overline{\text{DMA\_REQ}}$   | DMA Request—external DMA request signal. Multiplexed with SPI1_SPI_RDY.  |
| BIG_ENDIAN                     | Big Endian—Input signal that determines the configuration of the external chip-select space. If it is driven logic-high at reset, the external chip-select space will be configured to big endian. If it is driven logic-low at reset, the external chip-select space will be configured to little endian. This input must not change state after power-on reset negates or during chip operation. |

**Table 2. i.MXS Signal Descriptions (Continued)**

| Signal Name                   | Function/Notes   |
|-------------------------------|--|
| <b>ETM</b>                    |  |
| ETMTRACESYNC                  | ETM sync signal which is multiplexed with A24. ETMTRACESYNC is selected in ETM mode.   |
| ETMTRACECLK                   | ETM clock signal which is multiplexed with A23. ETMTRACECLK is selected in ETM mode.   |
| ETMPIESTAT [2:0]              | ETM status signals which are multiplexed with A [22:20]. ETMPIESTAT [2:0] are selected in ETM mode.  |
| ETMTRACEPKT [7:0]             | ETM packet signals which are multiplexed with $\overline{ECB}$ , $\overline{LBA}$ , BCLK (burst clock), PA17, A [19:16]. ETMTRACEPKT [7:0] are selected in ETM mode. |
| <b>LCD Controller</b>         |  |
| LD [15:0]                     | LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.   |
| FLM/VSYNC                     | Frame Sync or Vsync—This signal also serves as the clock signal output for the gate driver (dedicated signal SPS for Sharp panel HR-TFT).                            |
| LP/HSYNC                      | Line pulse or H sync   |
| LSCLK                         | Shift clock  |
| ACD/OE                        | Alternate crystal direction/output enable.   |
| CONTRAST                      | This signal is used to control the LCD bias voltage as contrast control.   |
| SPL_SPR                       | Program horizontal scan direction (Sharp panel dedicated signal).  |
| PS                            | Control signal output for source driver (Sharp panel dedicated signal).  |
| CLS                           | Start signal output for gate driver. This signal is an inverted version of PS (Sharp panel dedicated signal).  |
| REV                           | Signal for common electrode driving signal preparation (Sharp panel dedicated signal).   |
| <b>SPI 1</b>                  |  |
| SPI1_MOSI                     | Master Out/Slave In  |
| SPI1_MISO                     | Slave In/Master Out  |
| SPI1_ $\overline{SS}$         | Slave Select (Selectable polarity)   |
| SPI1_SCLK                     | Serial Clock   |
| SPI1_ $\overline{SPI\_RDY}$   | Serial Data Ready  |
| <b>General Purpose Timers</b> |  |
| TIN                           | Timer Input Capture or Timer Input Clock—The signal on this input is applied to both timers simultaneously.  |
| TMR2OUT                       | Timer 2 Output   |
| <b>USB Device</b>             |  |
| USBD_VMO                      | USB Minus Output   |
| USBD_VPO                      | USB Plus Output  |
| USBD_VM                       | USB Minus Input  |
| USBD_VP                       | USB Plus Input   |

Table 2. i.MXS Signal Descriptions (Continued)

| Signal Name  | Function/Notes  |
|--|---|
| USBD_SUSPND  | USB Suspend Output  |
| USBD_RCV   | USB Receive Data  |
| USBD_ROE   | USB $\overline{OE}$   |
| USBD_AFE   | USB Analog Front End Enable   |
| <b>UARTs – IrDA/Auto-Bauding</b>   |   |
| UART1_RXD  | Receive Data  |
| UART1_TXD  | Transmit Data   |
| $\overline{UART1\_RTS}$  | Request to Send   |
| $\overline{UART1\_CTS}$  | Clear to Send   |
| UART2_RXD  | Receive Data  |
| UART2_TXD  | Transmit Data   |
| $\overline{UART2\_RTS}$  | Request to Send   |
| $\overline{UART2\_CTS}$  | Clear to Send   |
| $\overline{UART2\_DSR}$  | Data Set Ready  |
| $\overline{UART2\_RI}$   | Ring Indicator  |
| $\overline{UART2\_DCD}$  | Data Carrier Detect   |
| $\overline{UART2\_DTR}$  | Data Terminal Ready   |
| <b>Serial Audio Port – SSI (configurable to I<sup>2</sup>S protocol)</b> |   |
| SSI_TXDAT  | Transmit Data   |
| SSI_RXDAT  | Receive Data  |
| SSI_TXCLK  | Transmit Serial Clock   |
| SSI_RXCLK  | Receive Serial Clock  |
| SSI_TXFS   | Transmit Frame Sync   |
| SSI_RXFS   | Receive Frame Sync  |
| <b>I<sup>2</sup>C</b>  |   |
| I2C_SCL  | I <sup>2</sup> C Clock  |
| I2C_SDA  | I <sup>2</sup> C Data   |
| <b>PWM</b>   |   |
| PWMO   | PWM Output  |
| <b>Test Function</b>   |   |
| TRISTATE   | Forces all I/O signals to high impedance for test purposes. For normal operation, terminate this input with a 1 k ohm resistor to ground. (TRI-STATE <sup>®</sup> is a registered trademark of National Semiconductor.) |
| <b>General Purpose Input/Output</b>                                      |   |
| PA[14:3]   | Dedicated GPIO  |

**Table 2. i.MXS Signal Descriptions (Continued)**

| Signal Name                         | Function/Notes                                   |
|-------------------------------------|--|
| PB[13:8]                            | Dedicated GPIO                                   |
| <b>Digital Supply Pins</b>          |  |
| NVDD                                | Digital Supply for the I/O pins                  |
| NVSS                                | Digital Ground for the I/O pins                  |
| <b>Supply Pins – Analog Modules</b> |  |
| AVDD                                | Supply for analog blocks                         |
| <b>Internal Power Supply</b>        |  |
| QVDD                                | Power supply pins for silicon internal circuitry |
| QVSS                                | Ground pins for silicon internal circuitry       |

## 2.1 I/O Pads Power Supply and Signal Multiplexing Scheme

This section describes detailed information about both the power supply for each I/O pin and its function multiplexing scheme. The user can reference information provided in [Table 6 on page 17](#) to configure the power supply scheme for each device in the system (memory and external peripherals). The function multiplexing information also shown in [Table 6](#) allows the user to select the function of each pin by configuring the appropriate GPIO registers when those pins are multiplexed to provide different functions.

**Table 3. MC9328MXS Signal Multiplexing Scheme**

| I/O Supply Voltage | 225 BGA Ball | Primary |     |         | Alternate        |     | GPIO |         | AIN          | BIN | AOUT | Default |
|--------------------|--------------|---------|-----|---------|------------------|-----|------|---------|--------------|-----|------|---------|
|                    |              | Signal  | Dir | Pull-Up | Signal           | Dir | Mux  | Pull-Up |              |     |      |         |
| NVDD1              | D2           | A24     | O   |         | ETMTRAC<br>ESYNC | O   | PA0  | 69K     | Reser<br>ved |     |      | A24     |
| NVDD1              | C1           | D31     | I/O | 69K     |                  |     |      |         |              |     |      |         |
| NVDD1              | D1           | A23     | O   |         | ETMTRAC<br>ECLK  | O   | PA31 | 69K     |              |     |      | A23     |
| NVDD1              | E3           | D30     | I/O | 69K     |                  |     |      |         |              |     |      |         |
| NVDD1              | E2           | A22     | O   |         | ETMPIPE<br>STAT2 | O   | PA30 | 69K     |              |     |      | A22     |
| NVDD1              | E4           | D29     | I/O | 69K     |                  |     |      |         |              |     |      |         |
| NVDD1              | E1           | A21     | O   |         | ETMPIPE<br>STAT1 | O   | PA29 | 69K     |              |     |      | A21     |
| NVDD1              | F3           | D28     | I/O | 69K     |                  |     |      |         |              |     |      |         |
| NVDD1              | F1           | A20     | O   |         | ETMPIPE<br>STAT0 | O   | PA28 | 69K     |              |     |      | A20     |
| NVDD1              | F4           | D27     | I/O | 69K     |                  |     |      |         |              |     |      |         |
| NVDD1              | F2           | A19     | O   |         | ETMTRAC<br>EPKT3 | O   | PA27 | 69K     |              |     |      | A19     |
| NVDD1              | G3           | D26     | I/O | 69K     |                  |     |      |         |              |     |      |         |



**Table 3. MC9328MXS Signal Multiplexing Scheme (Continued)**

| I/O Supply Voltage | 225 BGA Ball | Primary          |     |         | Alternate        |     | GPIO |         | AIN | BIN | AOUT | Default |
|--------------------|--------------|------------------|-----|---------|------------------|-----|------|---------|-----|-----|------|---------|
|                    |              | Signal           | Dir | Pull-Up | Signal           | Dir | Mux  | Pull-Up |     |     |      |         |
| NVDD1              | G2           | A18              | O   |         | ETMTRAC<br>EPKT2 | O   | PA26 | 69K     |     |     |      | A18     |
| NVDD1              | G4           | D25              | I/O | 69K     |                  |     |      |         |     |     |      |         |
| NVDD1              | G1           | A17              | O   |         | ETMTRAC<br>EPKT1 | O   | PA25 | 69K     |     |     |      | A17     |
| NVDD1              | H4           | D24              | I/O | 69K     |                  |     |      |         |     |     |      |         |
| NVDD1              | H2           | A16              | O   |         | ETMTRAC<br>EPKT0 | O   | PA24 | 69K     |     |     |      | A16     |
| NVDD1              | H3           | D23              | I/O | 69K     |                  |     |      |         |     |     |      |         |
| NVDD1              | H1           | A15              | O   |         |                  |     |      |         |     |     |      |         |
| NVDD1              | H5           | D22              | I/O | 69K     |                  |     |      |         |     |     |      |         |
| NVDD1              | J1           | A14              | O   |         |                  |     |      |         |     |     |      |         |
| NVDD1              | J3           | D21              | I/O | 69K     |                  |     |      |         |     |     |      |         |
| NVDD1              | K1           | A13              | O   |         |                  |     |      |         |     |     |      |         |
| NVDD1              | J4           | D20              | I/O | 69K     |                  |     |      |         |     |     |      |         |
| NVDD1              | J2           | A12              | O   |         |                  |     |      |         |     |     |      |         |
| NVDD1              | K4           | D19              | I/O | 69K     |                  |     |      |         |     |     |      |         |
| NVDD1              | K2           | A11              | O   |         |                  |     |      |         |     |     |      |         |
| NVDD1              | L4           | D18              | I/O | 69K     |                  |     |      |         |     |     |      |         |
| NVDD1              | L1           | A10              | O   |         |                  |     |      |         |     |     |      |         |
| NVDD1              | L3           | D17              | I/O | 69K     |                  |     |      |         |     |     |      |         |
| NVDD1              | L2           | A9               | O   |         |                  |     |      |         |     |     |      |         |
| NVDD1              | M1           | D16              | I/O | 69K     |                  |     |      |         |     |     |      |         |
| NVDD1              | N1           | A8               | O   |         |                  |     |      |         |     |     |      |         |
| NVDD1              | M2           | D15              | I/O | 69K     |                  |     |      |         |     |     |      |         |
| NVDD1              | N2           | A7               | O   |         |                  |     |      |         |     |     |      |         |
| NVDD1              | P1           | D14              | I/O | 69K     |                  |     |      |         |     |     |      |         |
| NVDD1              | R1           | A6               | O   |         |                  |     |      |         |     |     |      |         |
| NVDD1              | M3           | D13              | I/O | 69K     |                  |     |      |         |     |     |      |         |
| NVDD1              | P2           | A5               | O   |         |                  |     |      |         |     |     |      |         |
| NVDD1              | N3           | D12              | I/O | 69K     |                  |     |      |         |     |     |      |         |
| NVDD1              | P3           | A4               | O   |         |                  |     |      |         |     |     |      |         |
| NVDD1              | R2           | D11              | I/O | 69K     |                  |     |      |         |     |     |      |         |
| NVDD1              | N4           | $\overline{EB0}$ | O   |         |                  |     |      |         |     |     |      |         |
| NVDD1              | M4           | D10              | I/O | 69K     |                  |     |      |         |     |     |      |         |
| NVDD1              | P4           | A3               | O   |         |                  |     |      |         |     |     |      |         |
| NVDD1              | R3           | $\overline{EB1}$ | O   |         |                  |     |      |         |     |     |      |         |
| NVDD1              | N5           | D9               | I/O | 69K     |                  |     |      |         |     |     |      |         |
| NVDD1              | R4           | $\overline{EB2}$ | O   |         |                  |     |      |         |     |     |      |         |

**Table 3. MC9328MXS Signal Multiplexing Scheme (Continued)**

| I/O Supply Voltage | 225 BGA Ball | Primary                  |     |         | Alternate                |     | GPIO |         | AIN          | BIN | AOUT                      | Default                  |
|--------------------|--------------|--------------------------|-----|---------|--------------------------|-----|------|---------|--------------|-----|---------------------------|--------------------------|
|                    |              | Signal                   | Dir | Pull-Up | Signal                   | Dir | Mux  | Pull-Up |              |     |                           |                          |
| NVDD1              | P5           | A2                       | O   |         |                          |     |      |         |              |     |                           |                          |
| NVDD1              | M5           | $\overline{\text{EB3}}$  | O   |         |                          |     |      |         |              |     |                           |                          |
| NVDD1              | N6           | D8                       | I/O | 69K     |                          |     |      |         |              |     |                           |                          |
| NVDD1              | R5           | $\overline{\text{OE}}$   | O   |         |                          |     |      |         |              |     |                           |                          |
| NVDD1              | P6           | A1                       | O   |         |                          |     |      |         |              |     |                           |                          |
| NVDD1              | L7           | $\overline{\text{CS5}}$  | O   |         |                          |     | PA23 | 69K     |              |     |                           | PA23                     |
| NVDD1              | R6           | D7                       | I/O | 69K     |                          |     |      |         |              |     |                           |                          |
| NVDD1              | M7           | $\overline{\text{CS4}}$  | O   |         |                          |     | PA22 | 69K     |              |     |                           | PA22                     |
| NVDD1              | R7           | A0                       | O   |         |                          |     | PA21 | 69K     |              |     |                           | A0                       |
| NVDD1              | N7           | $\overline{\text{CS3}}$  | O   |         | $\overline{\text{CSD1}}$ |     |      |         |              |     |                           | $\overline{\text{CSD1}}$ |
| NVDD1              | P7           | D6                       | I/O | 69K     |                          |     |      |         |              |     |                           |                          |
| NVDD1              | K3           | $\overline{\text{CS2}}$  | O   |         | $\overline{\text{CSD0}}$ |     |      |         |              |     |                           | $\overline{\text{CSD0}}$ |
| NVDD1              | R8           | SDCLK                    | O   |         |                          |     |      |         |              |     |                           |                          |
| NVDD1              | M8           | $\overline{\text{CS1}}$  | O   |         |                          |     |      |         |              |     |                           |                          |
| NVDD1              | N8           | $\overline{\text{CS0}}$  | O   |         |                          |     |      |         |              |     |                           |                          |
| NVDD1              | P8           | D5                       | I/O | 69K     |                          |     |      |         |              |     |                           |                          |
| NVDD1              | L9           | $\overline{\text{ECB}}$  | I   |         | ETMTRAC<br>EPKT7         |     | PA20 | 69K     |              |     |                           | $\overline{\text{ECB}}$  |
| NVDD1              | R9           | D4                       | I/O | 69K     |                          |     |      |         |              |     |                           |                          |
| NVDD1              | R10          | $\overline{\text{LBA}}$  | O   |         | ETMTRAC<br>EPKT6         |     | PA19 | 69K     |              |     |                           | $\overline{\text{LBA}}$  |
| NVDD1              | R11          | D3                       | I/O | 69K     |                          |     |      |         |              |     |                           |                          |
| NVDD1              | M9           | BCLK                     |     |         | ETMTRAC<br>EPKT5         |     | PA18 | 69K     |              |     |                           | BCLK                     |
| NVDD1              | L8           | D2                       | I/O | 69K     |                          |     |      |         |              |     |                           |                          |
| NVDD1              | N9           | PA17                     |     |         | ETMTRAC<br>EPKT4         |     | PA17 | 69K     | Reser<br>ved |     | $\overline{\text{DTACK}}$ | PA17                     |
| NVDD1              | K10          | D1                       | I/O | 69K     |                          |     |      |         |              |     |                           |                          |
| NVDD1              | M10          | $\overline{\text{RW}}$   |     |         |                          |     |      |         |              |     |                           |                          |
| NVDD1              | P10          | MA11                     | O   |         |                          |     |      |         |              |     |                           |                          |
| NVDD1              | P9           | MA10                     | O   |         |                          |     |      |         |              |     |                           |                          |
| NVDD1              | N10          | D0                       | I/O | 69K     |                          |     |      |         |              |     |                           |                          |
| NVDD1              | R12          | DQM3                     | O   |         |                          |     |      |         |              |     |                           |                          |
| NVDD1              | N11          | DQM2                     | O   |         |                          |     |      |         |              |     |                           |                          |
| NVDD1              | P11          | DQM1                     | O   |         |                          |     |      |         |              |     |                           |                          |
| NVDD1              | N12          | DQM0                     | O   |         |                          |     |      |         |              |     |                           |                          |
| NVDD1              | P12          | $\overline{\text{RAS}}$  | O   |         |                          |     |      |         |              |     |                           |                          |
| NVDD1              | R13          | $\overline{\text{CAS}}$  | O   |         |                          |     |      |         |              |     |                           |                          |
| NVDD1              | R14          | $\overline{\text{SDWE}}$ | O   |         |                          |     |      |         |              |     |                           |                          |

Table 3. MC9328MXS Signal Multiplexing Scheme (Continued)

| I/O Supply Voltage | 225 BGA Ball | Primary                 |        |         | Alternate |     | GPIO |         | AIN | BIN | AOUT | Default |
|--------------------|--------------|-------------------------|--------|---------|-----------|-----|------|---------|-----|-----|------|---------|
|                    |              | Signal                  | Dir    | Pull-Up | Signal    | Dir | Mux  | Pull-Up |     |     |      |         |
| NVDD1              | N13          | SDCKE0                  | O      |         |           |     |      |         |     |     |      |         |
| NVDD1              | P13          | SDCKE1                  | O      |         |           |     |      |         |     |     |      |         |
| NVDD1              | P15          | RESET_SF                | O      |         |           |     |      |         |     |     |      |         |
| NVDD1              | P14          | CLKO                    | O      |         |           |     |      |         |     |     |      |         |
| AVDD1              | R15          | AVDD1                   | Static |         |           |     |      |         |     |     |      |         |
| QVDD2              | M13          | QVDD2                   | Static |         |           |     |      |         |     |     |      |         |
| AVDD1              | N15          | TRST                    | I      | 69K     |           |     |      |         |     |     |      |         |
| AVDD1              | N14          | TRISTATE <sub>1</sub>   | I      |         |           |     |      |         |     |     |      |         |
| AVDD1              | M15          | EXTAL16M                | I      |         |           |     |      |         |     |     |      |         |
| AVDD1              | L14          | XTAL16M                 | O      |         |           |     |      |         |     |     |      |         |
| AVDD1              | L15          | EXTAL32K                | I      |         |           |     |      |         |     |     |      |         |
| AVDD1              | K15          | XTAL32K                 | O      |         |           |     |      |         |     |     |      |         |
| AVDD1              | M14          | RESET_IN <sup>2</sup>   | I      | 69K     |           |     |      |         |     |     |      |         |
| AVDD1              | K14          | RESET_OUT               | O      |         |           |     |      |         |     |     |      |         |
| AVDD1              | L12          | POR <sup>2</sup>        | I      |         |           |     |      |         |     |     |      |         |
| AVDD1              | K13          | BIG_ENDIAN <sup>3</sup> | I      |         |           |     |      |         |     |     |      |         |
| AVDD1              | M12          | BOOT3 <sup>3</sup>      | I      |         |           |     |      |         |     |     |      |         |
| AVDD1              | K11          | BOOT2 <sup>3</sup>      | I      |         |           |     |      |         |     |     |      |         |
| AVDD1              | J14          | BOOT1 <sup>3</sup>      | I      |         |           |     |      |         |     |     |      |         |
| AVDD1              | J15          | BOOT0 <sup>3</sup>      | I      |         |           |     |      |         |     |     |      |         |
| NVDD2              | J13          | TDO <sup>4</sup>        | O      |         |           |     |      |         |     |     |      |         |
| NVDD2              | H15          | TMS                     | I      | 69K     |           |     |      |         |     |     |      |         |
| NVDD2              | J12          | TCK                     | I      | 69K     |           |     |      |         |     |     |      |         |
| NVDD2              | K12          | TDI                     | I      | 69K     |           |     |      |         |     |     |      |         |
| NVDD2              | J11          | I2C_SCL                 | O      |         |           |     | PA16 | 69K     |     |     |      | PA16    |
| NVDD2              | H14          | I2C_SDA                 | I/O    |         |           |     | PA15 | 69K     |     |     |      | PA15    |
| NVDD2              | H13          | Reserved                | I      |         |           |     | PA14 | 69K     |     |     |      | PA14    |
| NVDD2              | G14          | Reserved                | I      |         |           |     | PA13 | 69K     |     |     |      | PA13    |
| NVDD2              | H12          | Reserved                | I      |         |           |     | PA12 | 69K     |     |     |      | PA12    |
| NVDD2              | G13          | Reserved                | I      |         |           |     | PA11 | 69K     |     |     |      | PA11    |
| NVDD2              | J10          | Reserved                | I      |         |           |     | PA10 | 69K     |     |     |      | PA10    |
| NVDD2              | G15          | Reserved                | I      |         |           |     | PA9  | 69K     |     |     |      | PA9     |

**Table 3. MC9328MXS Signal Multiplexing Scheme (Continued)**

| I/O Supply Voltage | 225 BGA Ball | Primary        |     |         | Alternate |               | GPIO |         | AIN | BIN      | AOUT     | Default |
|--------------------|--------------|----------------|-----|---------|-----------|---------------|------|---------|-----|----------|----------|---------|
|                    |              | Signal         | Dir | Pull-Up | Signal    | Dir           | Mux  | Pull-Up |     |          |          |         |
| NVDD2              | F15          | Reserved       | I   |         |           |               | PA8  | 69K     |     |          |          | PA8     |
| NVDD2              | G12          | Reserved       | I   |         |           |               | PA7  | 69K     |     |          |          | PA7     |
| NVDD2              | F14          | Reserved       | I   |         |           |               | PA6  | 69K     |     |          |          | PA6     |
| NVDD2              | H11          | Reserved       | I   |         |           |               | PA5  | 69K     |     |          |          | PA5     |
| NVDD2              | E14          | Reserved       | I   |         |           |               | PA4  | 69K     |     |          |          | PA4     |
| NVDD2              | E15          | Reserved       | O   |         |           |               | PA3  | 69K     |     |          |          | PA3     |
| NVDD2              | G11          | PWMO           | O   |         |           |               | PA2  | 69K     |     |          |          | PA2     |
| NVDD2              | E13          | TIN            | I   |         |           |               | PA1  | 69K     |     |          | Reserved | PA1     |
| NVDD2              | D14          | TMR2OUT        | O   |         |           |               | PD31 | 69K     |     | Reserved |          | PD31    |
| NVDD2              | F13          | LD15           | O   |         |           |               | PD30 | 69K     |     |          |          | PD30    |
| NVDD2              | F12          | LD14           | O   |         |           |               | PD29 | 69K     |     |          |          | PD29    |
| NVDD2              | D15          | LD13           | O   |         |           |               | PD28 | 69K     |     |          |          | PD28    |
| NVDD2              | C14          | LD12           | O   |         |           |               | PD27 | 69K     |     |          |          | PD27    |
| NVDD2              | D13          | LD11           | O   |         |           |               | PD26 | 69K     |     |          |          | PD26    |
| NVDD2              | E12          | LD10           | O   |         |           |               | PD25 | 69K     |     |          |          | PD25    |
| NVDD2              | C13          | LD9            | O   |         |           |               | PD24 | 69K     |     |          |          | PD24    |
| NVDD2              | C12          | LD8            | O   |         |           |               | PD23 | 69K     |     |          |          | PD23    |
| NVDD2              | B15          | LD7            | O   |         |           |               | PD22 | 69K     |     |          |          | PD22    |
| NVDD2              | B14          | LD6            | O   |         |           |               | PD21 | 69K     |     |          |          | PD21    |
| NVDD2              | A15          | LD5            | O   |         |           |               | PD20 | 69K     |     |          |          | PD20    |
| NVDD2              | A14          | LD4            | O   |         |           |               | PD19 | 69K     |     |          |          | PD19    |
| NVDD2              | B13          | LD3            | O   |         |           |               | PD18 | 69K     |     |          |          | PD18    |
| NVDD2              | A13          | LD2            | O   |         |           |               | PD17 | 69K     |     |          |          | PD17    |
| NVDD2              | D12          | LD1            | O   |         |           |               | PD16 | 69K     |     |          |          | PD16    |
| NVDD2              | B12          | LD0            | O   |         |           |               | PD15 | 69K     |     |          |          | PD15    |
| NVDD2              | C11          | FLM/VSYN<br>NC | O   |         |           |               | PD14 | 69K     |     |          |          | PD14    |
| NVDD2              | D11          | LP/HSYN<br>C   | O   |         |           |               | PD13 | 69K     |     |          |          | PD13    |
| NVDD2              | E11          | ACD/OE         | O   |         |           |               | PD12 | 69K     |     |          |          | PD12    |
| NVDD2              | C10          | CONTR<br>ST    | O   |         |           |               | PD11 | 69K     |     |          |          | PD11    |
| NVDD2              | B11          | SPL_SPR        | O   |         |           | UART2_D<br>SR | O    | PD10    | 69K | Reserved |          | PD10    |
| NVDD2              | A12          | PS             | O   |         |           | UART2_RI      | O    | PD9     | 69K |          | Reserved | PD9     |
| NVDD2              | F10          | CLS            | O   |         |           | UART2_D<br>CD | O    | PD8     | 69K | Reserved |          | PD8     |
| NVDD2              | A11          | REV            | O   |         |           | UART2_D<br>TR | I    | PD7     | 69K | Reserved |          | PD7     |

Table 3. MC9328MXS Signal Multiplexing Scheme (Continued)

| I/O Supply Voltage | 225 BGA Ball | Primary      |     |         | Alternate |     | GPIO |         | AIN | BIN | AOUT    | Default |
|--------------------|--------------|--------------|-----|---------|-----------|-----|------|---------|-----|-----|---------|---------|
|                    |              | Signal       | Dir | Pull-Up | Signal    | Dir | Mux  | Pull-Up |     |     |         |         |
| NVDD2              | B10          | LSCLK        | O   |         |           |     | PD6  | 69K     |     |     |         | PD6     |
| NVDD3              | D10          | SPI1_MOSI    | I/O |         |           |     | PC17 | 69K     |     |     |         | PC17    |
| NVDD3              | E10          | SPI1_MISO    | I/O |         |           |     | PC16 | 69K     |     |     |         | PC16    |
| NVDD3              | B9           | SPI1_SS      | I/O |         |           |     | PC15 | 69K     |     |     |         | PC15    |
| NVDD3              | A10          | SPI1_SCLK    | I/O |         |           |     | PC14 | 69K     |     |     |         | PC14    |
| NVDD3              | A9           | SPI1_SPI_RDY | I/O |         |           |     | PC13 | 69K     |     |     | DMA_REQ | PC13    |
| NVDD3              | E8           | UART1_RXD    | I   |         |           |     | PC12 | 69K     |     |     |         | PC12    |
| NVDD3              | B8           | UART1_TXD    | O   |         |           |     | PC11 | 69K     |     |     |         | PC11    |
| NVDD3              | C9           | UART1_RTS    | I   |         |           |     | PC10 | 69K     |     |     |         | PC10    |
| NVDD3              | E9           | UART1_CTS    | O   |         |           |     | PC9  | 69K     |     |     |         | PC9     |
| NVDD3              | A8           | SSI_TXCLK    | I/O |         |           |     | PC8  | 69K     |     |     |         | PC8     |
| NVDD3              | C8           | SSI_TXFS     | I/O |         |           |     | PC7  | 69K     |     |     |         | PC7     |
| NVDD3              | F9           | SSI_TXDATA   | O   |         |           |     | PC6  | 69K     |     |     |         | PC6     |
| NVDD3              | B7           | SSI_RXDATA   | I   |         |           |     | PC5  | 69K     |     |     |         | PC5     |
| NVDD3              | F8           | SSI_RXCLK    | I   |         |           |     | PC4  | 69K     |     |     |         | PC4     |
| NVDD3              | A7           | SSI_RXFS     | I   |         |           |     | PC3  | 69K     |     |     |         | PC3     |
| NVDD4              | C7           | UART2_RXD    | I   |         |           |     | PB31 | 69K     |     |     |         | PB31    |
| NVDD4              | D8           | UART2_TXD    | O   |         |           |     | PB30 | 69K     |     |     |         | PB30    |
| NVDD4              | E7           | UART2_RTS    | I   |         |           |     | PB29 | 69K     |     |     |         | PB29    |
| NVDD4              | F7           | UART2_CTS    | O   |         |           |     | PB28 | 69K     |     |     |         | PB28    |
| NVDD4              | B6           | USBDM_VMO    | O   |         |           |     | PB27 | 69K     |     |     |         | PB27    |
| NVDD4              | C6           | USBDM_VPO    | O   |         |           |     | PB26 | 69K     |     |     |         | PB26    |
| NVDD4              | A6           | USBDM_VMI    | I   |         |           |     | PB25 | 69K     |     |     |         | PB25    |
| NVDD4              | D6           | USBDM_VPI    | I   |         |           |     | PB24 | 69K     |     |     |         | PB24    |
| NVDD4              | A5           | USBDM_SSPND  | O   |         |           |     | PB23 | 69K     |     |     |         | PB23    |

**Table 3. MC9328MXS Signal Multiplexing Scheme (Continued)**

| I/O Supply Voltage | 225 BGA Ball | Primary      |        |         | Alternate |     | GPIO |                    | AIN | BIN | AOUT | Default |
|--------------------|--------------|--------------|--------|---------|-----------|-----|------|--------------------|-----|-----|------|---------|
|                    |              | Signal       | Dir    | Pull-Up | Signal    | Dir | Mux  | Pull-Up            |     |     |      |         |
| NVDD4              | B5           | USBD_RC<br>V | I/O    |         |           |     | PB22 | 69K                |     |     |      | PB22    |
| NVDD4              | A4           | USBD_RO<br>E | O      |         |           |     | PB21 | 69K                |     |     |      | PB21    |
| NVDD4              | B4           | USBD_AF<br>E | O      |         |           |     | PB20 | 69K                |     |     |      | PB20    |
| NVDD4              | A3           | PB19         | I/O    |         |           |     |      | 69K                |     |     |      | PB19    |
| NVDD4              | C4           | PB18         | I/O    |         |           |     |      | 69K                |     |     |      | PB18    |
| NVDD4              | D4           | PB17         | O      |         |           |     |      | 69K                |     |     |      | PB17    |
| NVDD4              | B3           | PB16         | I      |         |           |     |      | 69K                |     |     |      | PB16    |
| NVDD4              | A2           | PB15         | I      |         |           |     |      | 69K                |     |     |      | PB15    |
| NVDD4              | C3           | PB14         | I      |         |           |     |      | 69K                |     |     |      | PB14    |
| NVDD4              | A1           | Reserved     | I/O    |         | Reserved  |     | PB13 | 69K                |     |     |      | PB13    |
| NVDD4              | B2           | Reserved     | O      |         | Reserved  |     | PB12 | 69K                |     |     |      | PB12    |
| NVDD4              | B1           | Reserved     | I/O    |         | Reserved  |     | PB11 | 69K<br>(pull down) |     |     |      | PB11    |
| NVDD4              | C5           | Reserved     | I/O    |         | Reserved  |     | PB10 | 69K                |     |     |      | PB10    |
| NVDD4              | D3           | Reserved     | I/O    |         | Reserved  |     | PB9  | 69K                |     |     |      | PB9     |
| NVDD4              | C2           | Reserved     | I/O    |         | Reserved  |     | PB8  | 69K                |     |     |      | PB8     |
| NVDD1              | D5           | NVDD1        | Static |         |           |     |      |                    |     |     |      |         |
|                    | G6           | NVSS         | Static |         |           |     |      |                    |     |     |      |         |
| NVDD1              | E5           | NVDD1        | Static |         |           |     |      |                    |     |     |      |         |
|                    | H6           | NVSS         | Static |         |           |     |      |                    |     |     |      |         |
| QVDD1              | J8           | QVDD1        | Static |         |           |     |      |                    |     |     |      |         |
|                    | E6           | QVSS         | Static |         |           |     |      |                    |     |     |      |         |
| NVDD1              | F5           | NVDD         | Static |         |           |     |      |                    |     |     |      |         |
|                    | J6           | NVSS         | Static |         |           |     |      |                    |     |     |      |         |
| NVDD1              | G5           | NVDD1        | Static |         |           |     |      |                    |     |     |      |         |
|                    | K6           | NVSS         | Static |         |           |     |      |                    |     |     |      |         |
| NVDD1              | J5           | NVDD1        | Static |         |           |     |      |                    |     |     |      |         |
|                    | H7           | NVSS         | Static |         |           |     |      |                    |     |     |      |         |
| NVDD1              | K5           | NVDD1        | Static |         |           |     |      |                    |     |     |      |         |
|                    | J7           | NVSS         | Static |         |           |     |      |                    |     |     |      |         |
| NVDD1              | L5           | NVDD1        | Static |         |           |     |      |                    |     |     |      |         |
|                    | G8           | NVSS         | Static |         |           |     |      |                    |     |     |      |         |
| NVDD1              | L5           | NVDD1        | Static |         |           |     |      |                    |     |     |      |         |
|                    | H8           | NVSS         | Static |         |           |     |      |                    |     |     |      |         |
|                    | K7           | QVSS         | Static |         |           |     |      |                    |     |     |      |         |

Table 3. MC9328MXS Signal Multiplexing Scheme (Continued)

| I/O Supply Voltage | 225 BGA Ball | Primary |        |         | Alternate |     | GPIO |         | AIN | BIN | AOUT | Default |
|--------------------|--------------|---------|--------|---------|-----------|-----|------|---------|-----|-----|------|---------|
|                    |              | Signal  | Dir    | Pull-Up | Signal    | Dir | Mux  | Pull-Up |     |     |      |         |
| NVDD2              | H10          | NVDD2   | Static |         |           |     |      |         |     |     |      |         |
|                    | G9           | NVSS    | Static |         |           |     |      |         |     |     |      |         |
| QVDD3              | F11          | QVDD3   | Static |         |           |     |      |         |     |     |      |         |
|                    | G10          | QVSS    | Static |         |           |     |      |         |     |     |      |         |
| NVDD2              | C15          | NVDD2   | Static |         |           |     |      |         |     |     |      |         |
|                    | H9           | NVSS    | Static |         |           |     |      |         |     |     |      |         |
| QVDD4              | D7           | QVDD4   | Static |         |           |     |      |         |     |     |      |         |
|                    | L13          | QVSS    | Static |         |           |     |      |         |     |     |      |         |
| NVDD3              | D9           | NVDD3   | Static |         |           |     |      |         |     |     |      |         |
|                    | J9           | NVSS    | Static |         |           |     |      |         |     |     |      |         |
|                    | K9           | NVSS    | Static |         |           |     |      |         |     |     |      |         |
| NVDD4              | G7           | NVDD4   | Static |         |           |     |      |         |     |     |      |         |
| NVDD1              | F6           | NVDD1   | Static |         |           |     |      |         |     |     |      |         |
| NVDD1              | L6           | NVDD1   | Static |         |           |     |      |         |     |     |      |         |
| NVDD1              | M6           | NVDD1   | Static |         |           |     |      |         |     |     |      |         |
| NVDD1              | K8           | NVDD1   | Static |         |           |     |      |         |     |     |      |         |
|                    | L10          | NVSS    | Static |         |           |     |      |         |     |     |      |         |
|                    | L11          | NVSS    | Static |         |           |     |      |         |     |     |      |         |
|                    | M11          | NVSS    | Static |         |           |     |      |         |     |     |      |         |

- <sup>1</sup> Pull down this input with 1K $\Omega$  resistor to GND.
- <sup>2</sup> External circuit required to drive this input.
- <sup>3</sup> Tie this input high (to AVDD) or pull down with 1K $\Omega$  resistor to GND.
- <sup>4</sup> Pull up this output with a resistor to NVDD2.

## 3 Electrical Characteristics

This section contains the electrical specifications and timing diagrams for the i.MXS processor.

### 3.1 Maximum Ratings

Table 4 provides information on maximum ratings which are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits listed in Recommended Operating Range Table 5 on page 17 or the DC Characteristics table.

**Table 4. Maximum Ratings**

| Symbol              | Rating                                      | Minimum          | Maximum           | Unit |
|---------------------|---|------------------|-------------------|------|
| NV <sub>DD</sub>    | DC I/O Supply Voltage                       | -0.3             | 3.3               | V    |
| QV <sub>DD</sub>    | DC Internal (core = 100 MHz) Supply Voltage | -0.3             | 1.9               | V    |
| AV <sub>DD</sub>    | DC Analog Supply Voltage                    | -0.3             | 3.3               | V    |
| BTRFV <sub>DD</sub> | DC Bluetooth Supply Voltage                 | -0.3             | 3.3               | V    |
| VESD_HBM            | ESD immunity with HBM (human body model)    | –                | 2000              | V    |
| VESD_MM             | ESD immunity with MM (machine model)        | –                | 100               | V    |
| ILatchup            | Latch-up immunity                           | –                | 200               | mA   |
| Test                | Storage temperature                         | -55              | 150               | °C   |
| Pmax                | Power Consumption                           | 800 <sup>1</sup> | 1300 <sup>2</sup> | mW   |

<sup>1</sup> A typical application with 30 pads simultaneously switching assumes the GPIO toggling and instruction fetches from the ARM<sup>®</sup> core—that is, 7x GPIO, 15x Data bus, and 8x Address bus.

<sup>2</sup> A worst-case application with 70 pads simultaneously switching assumes the GPIO toggling and instruction fetches from the ARM core—that is, 32x GPIO, 30x Data bus, 8x Address bus. These calculations are based on the core running its heaviest OS application at 100MHz, and where the whole image is running out of SDRAM. QVDD at 1.9V, NVDD and AVDD at 3.3V, therefore, 180mA is the worst measurement recorded in the factory environment, max 5mA is consumed for OSC pads, with each toggle GPIO consuming 4mA.

### 3.2 Recommended Operating Range

Table 5 provides the recommended operating ranges for the supply voltages and temperatures. The i.MXS processor has multiple pairs of VDD and VSS power supply and return pins. QVDD and QVSS pins are used for internal logic. All other VDD and VSS pins are for the I/O pads voltage supply, and each pair of VDD and VSS provides power to the enclosed I/O pads. This design allows different peripheral supply voltage levels in a system.

Because AVDD pins are supply voltages to the analog pads, it is recommended to isolate and noise-filter the AVDD pins from other VDD pins.

For more information about I/O pads grouping per VDD, please refer to Table 2 on page 4.



Table 5. Recommended Operating Range

| Symbol         | Rating   | Minimum | Maximum | Unit |
|----------------|--|---------|---------|------|
| T <sub>A</sub> | Operating temperature range<br>MC9328MXSVP10                                   | 0       | 70      | °C   |
| T <sub>A</sub> | Operating temperature range<br>MC9328MXSCVP10                                  | -40     | 85      | °C   |
| NVDD           | I/O supply voltage (if using SPI, LCD, and USBd which are only 3 V interfaces) | 2.70    | 3.30    | V    |
| NVDD           | I/O supply voltage (if not using the peripherals listed above)                 | 1.70    | 3.30    | V    |
| QVDD           | Internal supply voltage (Core = 100 MHz)                                       | 1.70    | 1.90    | V    |
| AVDD           | Analog supply voltage  | 1.70    | 3.30    | V    |

### 3.3 Power Sequence Requirements

For required power-up and power-down sequencing, please refer to the “Power-Up Sequence” section of application note AN2537 on the i.MX applications processor website.

### 3.4 DC Electrical Characteristics

Table 6 contains both maximum and minimum DC characteristics of the i.MXS processor.

Table 6. Maximum and Minimum DC Characteristics

| Number or Symbol  | Parameter  | Min                | Typical   | Max                  | Unit |
|-------------------|--|--------------------|---|----------------------|------|
| I <sub>op</sub>   | Full running operating current at 1.8V for QVDD, 3.3V for NVDD/AVDD (Core = 96 MHz, System = 96 MHz, driving TFT display panel, and OS with MMU enabled memory system is running on external SDRAM). | –                  | QVDD at 1.8V = 120mA;<br>NVDD+AVDD at 3.0V = 30mA | –                    | mA   |
| Sidd <sub>1</sub> | Standby current<br>(Core = 100 MHz, QVDD = 1.8V, temp = 25°C)  | –                  | 25  | –                    | μA   |
| Sidd <sub>2</sub> | Standby current<br>(Core = 100 MHz, QVDD = 1.8V, temp = 55°C)  | –                  | 45  | –                    | μA   |
| Sidd <sub>3</sub> | Standby current<br>(Core = 100 MHz, QVDD = 1.9V, temp = 25°C)  | –                  | 35  | –                    | μA   |
| Sidd <sub>4</sub> | Standby current<br>(Core = 100 MHz, QVDD = 1.9V, temp = 55°C)  | –                  | 60  | –                    | μA   |
| V <sub>IH</sub>   | Input high voltage   | 0.7V <sub>DD</sub> | –   | V <sub>dd</sub> +0.2 | V    |
| V <sub>IL</sub>   | Input low voltage  | –                  | –   | 0.4                  | V    |
| V <sub>OH</sub>   | Output high voltage (I <sub>OH</sub> = 2.0 mA)   | 0.7V <sub>DD</sub> | –   | V <sub>dd</sub>      | V    |
| V <sub>OL</sub>   | Output low voltage (I <sub>OL</sub> = -2.5 mA)   | –                  | –   | 0.4                  | V    |
| I <sub>IL</sub>   | Input low leakage current<br>(V <sub>IN</sub> = GND, no pull-up or pull-down)  | –                  | –   | ±1                   | μA   |

Table 6. Maximum and Minimum DC Characteristics (Continued)

| Number or Symbol | Parameter  | Min  | Typical | Max     | Unit    |
|------------------|--|------|---------|---------|---------|
| $I_{IH}$         | Input high leakage current<br>( $V_{IN} = V_{DD}$ , no pull-up or pull-down) | –    | –       | $\pm 1$ | $\mu A$ |
| $I_{OH}$         | Output high current<br>( $V_{OH} = 0.8V_{DD}$ , $V_{DD} = 1.8V$ )            | 4.0  | –       | –       | mA      |
| $I_{OL}$         | Output low current<br>( $V_{OL} = 0.4V$ , $V_{DD} = 1.8V$ )                  | -4.0 | –       | –       | mA      |
| $I_{OZ}$         | Output leakage current<br>( $V_{out} = V_{DD}$ , output is high impedance)   | –    | –       | $\pm 5$ | $\mu A$ |
| $C_i$            | Input capacitance  | –    | –       | 5       | pF      |
| $C_o$            | Output capacitance   | –    | –       | 5       | pF      |

### 3.5 AC Electrical Characteristics

The AC characteristics consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of other signals. All timing specifications are specified at a system operating frequency from 0 MHz to 96 MHz (core operating frequency 100 MHz) with an operating supply voltage from  $V_{DD\ min}$  to  $V_{DD\ max}$  under an operating temperature from  $T_L$  to  $T_H$ . All timing is measured at 30 pF loading.

Table 7. Tristate Signal Timing

| Pin      | Parameter  | Minimum | Maximum | Unit |
|----------|--|---------|---------|------|
| TRISTATE | Time from TRISTATE activate until I/O becomes Hi-Z | –       | 20.8    | ns   |

Table 8. 32k/16M Oscillator Signal Timing

| Parameter   | Minimum | RMS | Maximum | Unit |
|---|---------|-----|---------|------|
| EXTAL32k input jitter (peak to peak)              | –       | 5   | 20      | ns   |
| EXTAL32k startup time                             | 800     | –   | –       | ms   |
| EXTAL16M input jitter (peak to peak) <sup>1</sup> | –       | TBD | TBD     | –    |
| EXTAL16M startup time <sup>1</sup>                | TBD     | –   | –       | –    |

<sup>1</sup> The 16 MHz oscillator is not recommended for use in new designs.

## 4 Functional Description and Application Information

This section provides the electrical information including and timing diagrams for the individual modules of the i.MXS.

## 4.1 Embedded Trace Macrocell

All registers in the ETM9 are programmed through a JTAG interface. The interface is an extension of the ARM920T processor’s TAP controller, and is assigned scan chain 6. The scan chain consists of a 40-bit shift register comprised of the following:

- 32-bit data field
- 7-bit address field
- A read/write bit

The data to be written is scanned into the 32-bit data field, the address of the register into the 7-bit address field, and a 1 into the read/write bit.

A register is read by scanning its address into the address field and a 0 into the read/write bit. The 32-bit data field is ignored. A read or a write takes place when the TAP controller enters the UPDATE-DR state. The timing diagram for the ETM9 is shown in Figure 2. See Table 9 for the ETM9 timing parameters used in Figure 2.

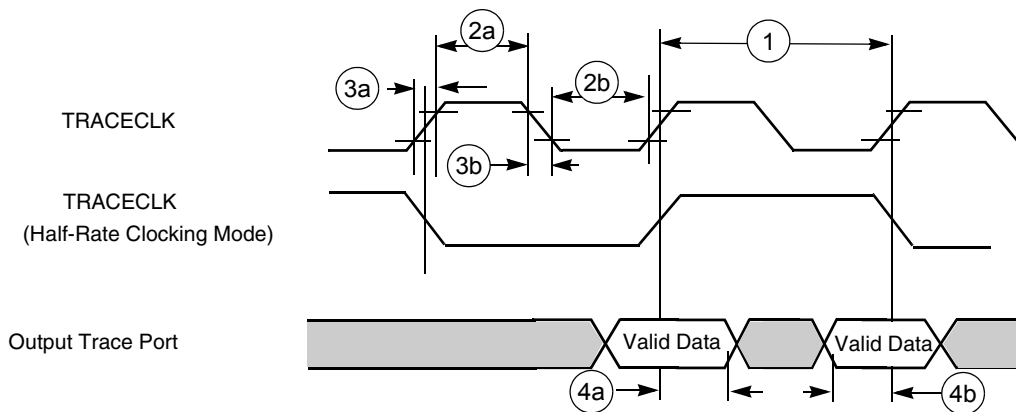


Figure 2. Trace Port Timing Diagram

Table 9. Trace Port Timing Diagram Parameter Table

| Ref No. | Parameter         | 1.8 ± 0.1 V |         | 3.0 ± 0.3 V |         | Unit |
|---------|-------------------|-------------|---------|-------------|---------|------|
|         |                   | Minimum     | Maximum | Minimum     | Maximum |      |
| 1       | CLK frequency     | 0           | 85      | 0           | 100     | MHz  |
| 2a      | Clock high time   | 1.3         | –       | 2           | –       | ns   |
| 2b      | Clock low time    | 3           | –       | 2           | –       | ns   |
| 3a      | Clock rise time   | –           | 4       | –           | 3       | ns   |
| 3b      | Clock fall time   | –           | 3       | –           | 3       | ns   |
| 4a      | Output hold time  | 2.28        | –       | 2           | –       | ns   |
| 4b      | Output setup time | 3.42        | –       | 3           | –       | ns   |

## 4.2 DPLL Timing Specifications

Parameters of the DPLL are given in Table 10. In this table,  $T_{ref}$  is a reference clock period after the pre-divider and  $T_{dck}$  is the output double clock period.

Table 10. DPLL Specifications

| Parameter                              | Test Conditions   | Minimum | Typical          | Maximum | Unit              |
|--|---|---------|------------------|---------|-------------------|
| DPLL input clock freq range            | Vcc = 1.8V  | 5       | –                | 100     | MHz               |
| Pre-divider output clock freq range    | Vcc = 1.8V  | 5       | –                | 30      | MHz               |
| DPLL output clock freq range           | Vcc = 1.8V  | 80      | –                | 220     | MHz               |
| Pre-divider factor (PD)                | –   | 1       | –                | 16      | –                 |
| Total multiplication factor (MF)       | Includes both integer and fractional parts                            | 5       | –                | 15      | –                 |
| MF integer part                        | –   | 5       | –                | 15      | –                 |
| MF numerator                           | Should be less than the denominator                                   | 0       | –                | 1022    | –                 |
| MF denominator                         | –   | 1       | –                | 1023    | –                 |
| Pre-multiplier lock-in time            | –   | –       | –                | 312.5   | μsec              |
| Freq lock-in time after full reset     | FOL mode for non-integer MF (does not include pre-multi lock-in time) | 250     | 280<br>(56 μs)   | 300     | $T_{ref}$         |
| Freq lock-in time after partial reset  | FOL mode for non-integer MF (does not include pre-multi lock-in time) | 220     | 250<br>(50 μs)   | 270     | $T_{ref}$         |
| Phase lock-in time after full reset    | FPL mode and integer MF (does not include pre-multi lock-in time)     | 300     | 350<br>(70 μs)   | 400     | $T_{ref}$         |
| Phase lock-in time after partial reset | FPL mode and integer MF (does not include pre-multi lock-in time)     | 270     | 320<br>(64 μs)   | 370     | $T_{ref}$         |
| Freq jitter (p-p)                      | –   | –       | 0.005<br>(0.01%) | 0.01    | $2 \cdot T_{dck}$ |
| Phase jitter (p-p)                     | Integer MF, FPL mode, Vcc=1.8V  | –       | 1.0<br>(10%)     | 1.5     | ns                |
| Power supply voltage                   | –   | 1.7     | –                | 2.5     | V                 |
| Power dissipation                      | FOL mode, integer MF,<br>$f_{dck} = 100$ MHz, Vcc = 1.8V              | –       | –                | 4       | mW                |

## 4.3 Reset Module

The timing relationships of the Reset module with the POR and RESET\_IN are shown in Figure 3 and Figure 4.

### NOTE

Be aware that NVDD must ramp up to at least 1.8V before QVDD is powered up to prevent forward biasing.

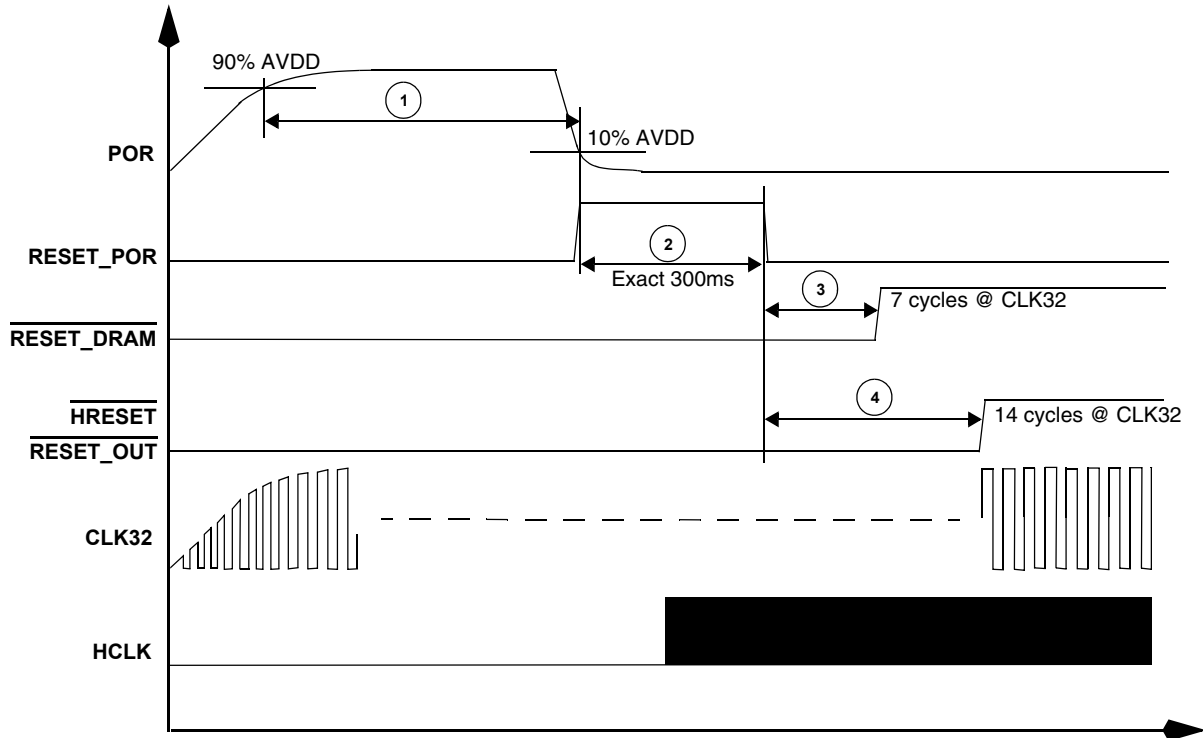


Figure 3. Timing Relationship with POR

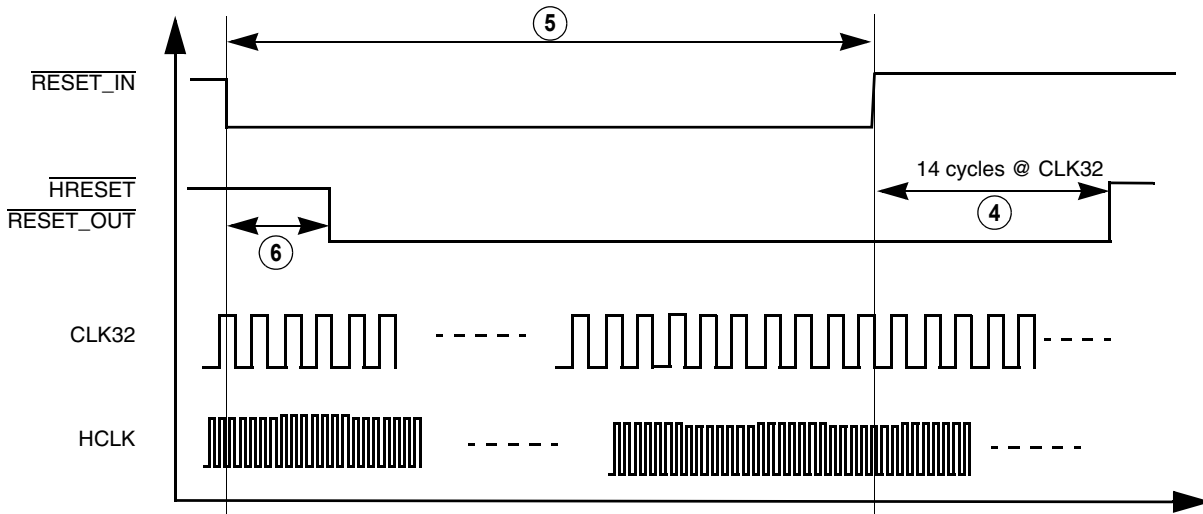


Figure 4. Timing Relationship with RESET\_IN

Table 11. Reset Module Timing Parameter Table

| Ref No. | Parameter  | 1.8 ± 0.1 V       |     | 3.0 ± 0.3 V       |     | Unit            |
|---------|--|-------------------|-----|-------------------|-----|-----------------|
|         |  | Min               | Max | Min               | Max |                 |
| 1       | Width of input POWER_ON_RESET  | note <sup>1</sup> | –   | note <sup>1</sup> | –   | –               |
| 2       | Width of internal $\overline{\text{POWER\_ON\_RESET}}$ (CLK32 at 32 kHz)   | 300               | 300 | 300               | 300 | ms              |
| 3       | 7K to 32K-cycle stretcher for SDRAM reset  | 7                 | 7   | 7                 | 7   | Cycles of CLK32 |
| 4       | 14K to 32K-cycle stretcher for internal system reset $\overline{\text{HRESET}}$ and output reset at pin $\overline{\text{RESET\_OUT}}$ | 14                | 14  | 14                | 14  | Cycles of CLK32 |
| 5       | Width of external hard-reset $\overline{\text{RESET\_IN}}$   | 4                 | –   | 4                 | –   | Cycles of CLK32 |
| 6       | 4K to 32K-cycle qualifier  | 4                 | 4   | 4                 | 4   | Cycles of CLK32 |

<sup>1</sup> POR width is dependent on the 32 or 32.768 kHz crystal oscillator start-up time. Design margin should allow for crystal tolerance, i.MX chip variations, temperature impact, and supply voltage influence. Through the process of supplying crystals for use with CMOS oscillators, crystal manufacturers have developed a working knowledge of start-up time of their crystals. Typically, start-up times range from 400 ms to 1.2 seconds for this type of crystal. If an external stable clock source (already running) is used instead of a crystal, the width of POR should be ignored in calculating timing for the start-up process.

## 4.4 External Interface Module

The External Interface Module (EIM) handles the interface to devices external to the i.MXS processor, including the generation of chip-selects for external peripherals and memory. The timing diagram for the EIM is shown in [Figure 5](#), and [Table 12](#) defines the parameters of signals.

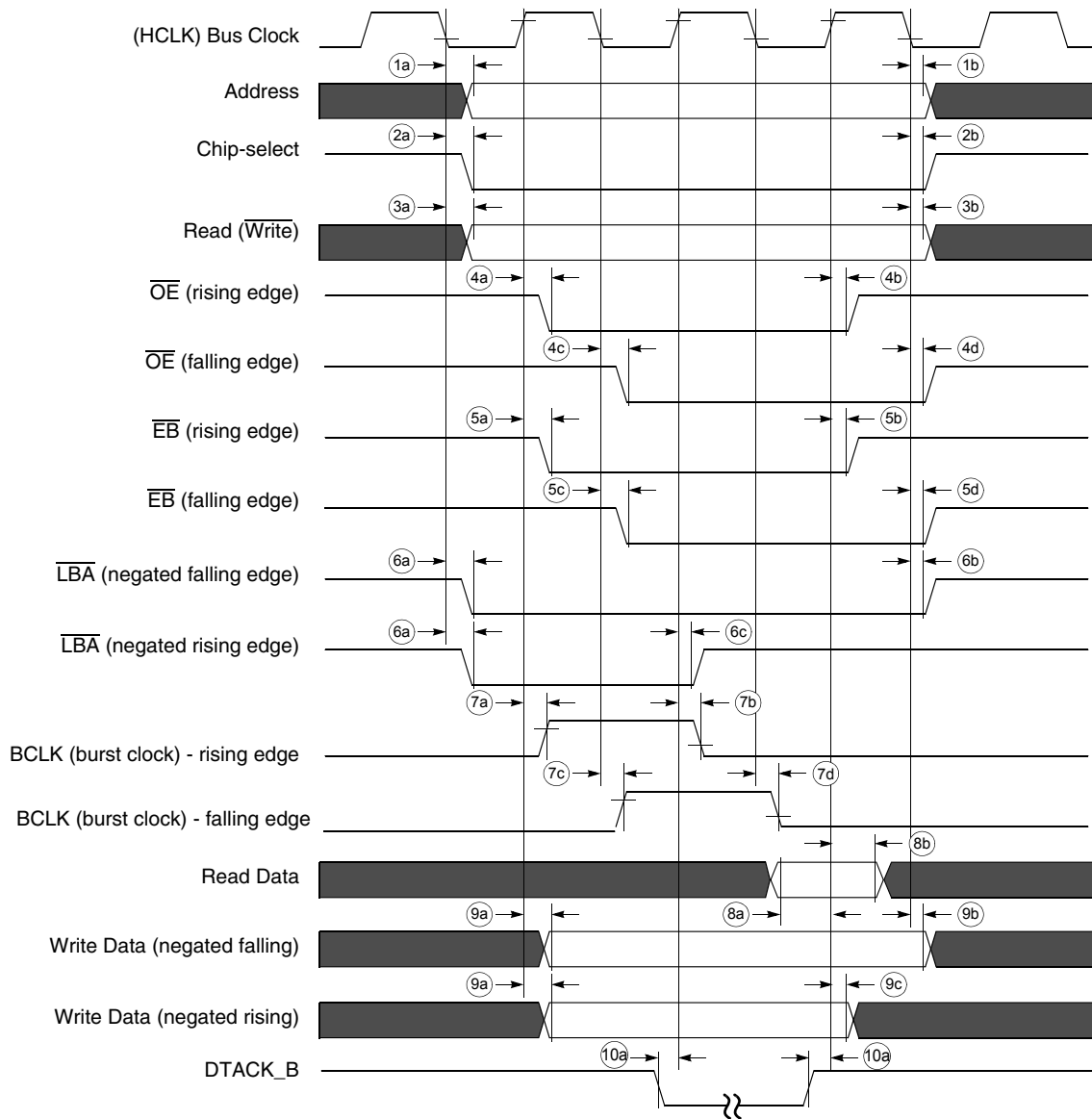


Figure 5. EIM Bus Timing Diagram

Table 12. EIM Bus Timing Parameter Table

| Ref No. | Parameter                          | 1.8 ± 0.1 V |         |      | 3.0 ± 0.3 V |         |     | Unit |
|---------|------------------------------------|-------------|---------|------|-------------|---------|-----|------|
|         |                                    | Min         | Typical | Max  | Min         | Typical | Max |      |
| 1a      | Clock fall to address valid        | 2.48        | 3.31    | 9.11 | 2.4         | 3.2     | 8.8 | ns   |
| 1b      | Clock fall to address invalid      | 1.55        | 2.48    | 5.69 | 1.5         | 2.4     | 5.5 | ns   |
| 2a      | Clock fall to chip-select valid    | 2.69        | 3.31    | 7.87 | 2.6         | 3.2     | 7.6 | ns   |
| 2b      | Clock fall to chip-select invalid  | 1.55        | 2.48    | 6.31 | 1.5         | 2.4     | 6.1 | ns   |
| 3a      | Clock fall to Read (Write) Valid   | 1.35        | 2.79    | 6.52 | 1.3         | 2.7     | 6.3 | ns   |
| 3b      | Clock fall to Read (Write) Invalid | 1.86        | 2.59    | 6.11 | 1.8         | 2.5     | 5.9 | ns   |

Table 12. EIM Bus Timing Parameter Table (Continued)

| Ref No. | Parameter   | 1.8 ± 0.1 V |         |      | 3.0 ± 0.3 V |         |     | Unit |
|---------|---|-------------|---------|------|-------------|---------|-----|------|
|         |   | Min         | Typical | Max  | Min         | Typical | Max |      |
| 4a      | Clock <sup>1</sup> rise to Output Enable Valid        | 2.32        | 2.62    | 6.85 | 2.3         | 2.6     | 6.8 | ns   |
| 4b      | Clock <sup>1</sup> rise to Output Enable Invalid      | 2.11        | 2.52    | 6.55 | 2.1         | 2.5     | 6.5 | ns   |
| 4c      | Clock <sup>1</sup> fall to Output Enable Valid        | 2.38        | 2.69    | 7.04 | 2.3         | 2.6     | 6.8 | ns   |
| 4d      | Clock <sup>1</sup> fall to Output Enable Invalid      | 2.17        | 2.59    | 6.73 | 2.1         | 2.5     | 6.5 | ns   |
| 5a      | Clock <sup>1</sup> rise to Enable Bytes Valid         | 1.91        | 2.52    | 5.54 | 1.9         | 2.5     | 5.5 | ns   |
| 5b      | Clock <sup>1</sup> rise to Enable Bytes Invalid       | 1.81        | 2.42    | 5.24 | 1.8         | 2.4     | 5.2 | ns   |
| 5c      | Clock <sup>1</sup> fall to Enable Bytes Valid         | 1.97        | 2.59    | 5.69 | 1.9         | 2.5     | 5.5 | ns   |
| 5d      | Clock <sup>1</sup> fall to Enable Bytes Invalid       | 1.76        | 2.48    | 5.38 | 1.7         | 2.4     | 5.2 | ns   |
| 6a      | Clock <sup>1</sup> fall to Load Burst Address Valid   | 2.07        | 2.79    | 6.73 | 2.0         | 2.7     | 6.5 | ns   |
| 6b      | Clock <sup>1</sup> fall to Load Burst Address Invalid | 1.97        | 2.79    | 6.83 | 1.9         | 2.7     | 6.6 | ns   |
| 6c      | Clock <sup>1</sup> rise to Load Burst Address Invalid | 1.91        | 2.62    | 6.45 | 1.9         | 2.6     | 6.4 | ns   |
| 7a      | Clock <sup>1</sup> rise to Burst Clock rise           | 1.61        | 2.62    | 5.64 | 1.6         | 2.6     | 5.6 | ns   |
| 7b      | Clock <sup>1</sup> rise to Burst Clock fall           | 1.61        | 2.62    | 5.84 | 1.6         | 2.6     | 5.8 | ns   |
| 7c      | Clock <sup>1</sup> fall to Burst Clock rise           | 1.55        | 2.48    | 5.59 | 1.5         | 2.4     | 5.4 | ns   |
| 7d      | Clock <sup>1</sup> fall to Burst Clock fall           | 1.55        | 2.59    | 5.80 | 1.5         | 2.5     | 5.6 | ns   |
| 8a      | Read Data setup time                                  | 5.54        | –       | –    | 5.5         | –       | –   | ns   |
| 8b      | Read Data hold time                                   | 0           | –       | –    | 0           | –       | –   | ns   |
| 9a      | Clock <sup>1</sup> rise to Write Data Valid           | 1.81        | 2.72    | 6.85 | 1.8         | 2.7     | 6.8 | ns   |
| 9b      | Clock <sup>1</sup> fall to Write Data Invalid         | 1.45        | 2.48    | 5.69 | 1.4         | 2.4     | 5.5 | ns   |
| 9c      | Clock <sup>1</sup> rise to Write Data Invalid         | 1.63        | –       | –    | 1.62        | –       | –   | ns   |
| 10a     | $\overline{\text{DTACK}}$ setup time                  | 2.52        | –       | –    | 2.5         | –       | –   | ns   |

<sup>1</sup> Clock refers to the system clock signal, HCLK, generated from the System DPLL

#### 4.4.1 $\overline{\text{DTACK}}$ Signal Description

The  $\overline{\text{DTACK}}$  signal is the external input data acknowledge signal. When using the external  $\overline{\text{DTACK}}$  signal as a data acknowledge signal, the bus time-out monitor generates a bus error when a bus cycle is not terminated by the external  $\overline{\text{DTACK}}$  signal after 1022 HCLK counts have elapsed. Only the CS5 group supports DTACK signal function when the external DTACK signal is used for data acknowledgement.

#### 4.4.2 $\overline{\text{DTACK}}$ Signal Timing

Figure 6 through Figure 9 show the access cycle timing used by chip-select 5. The signal values and units of measure for this figure are found in the associated tables.



### 4.4.2.1 WAIT Read Cycle without DMA

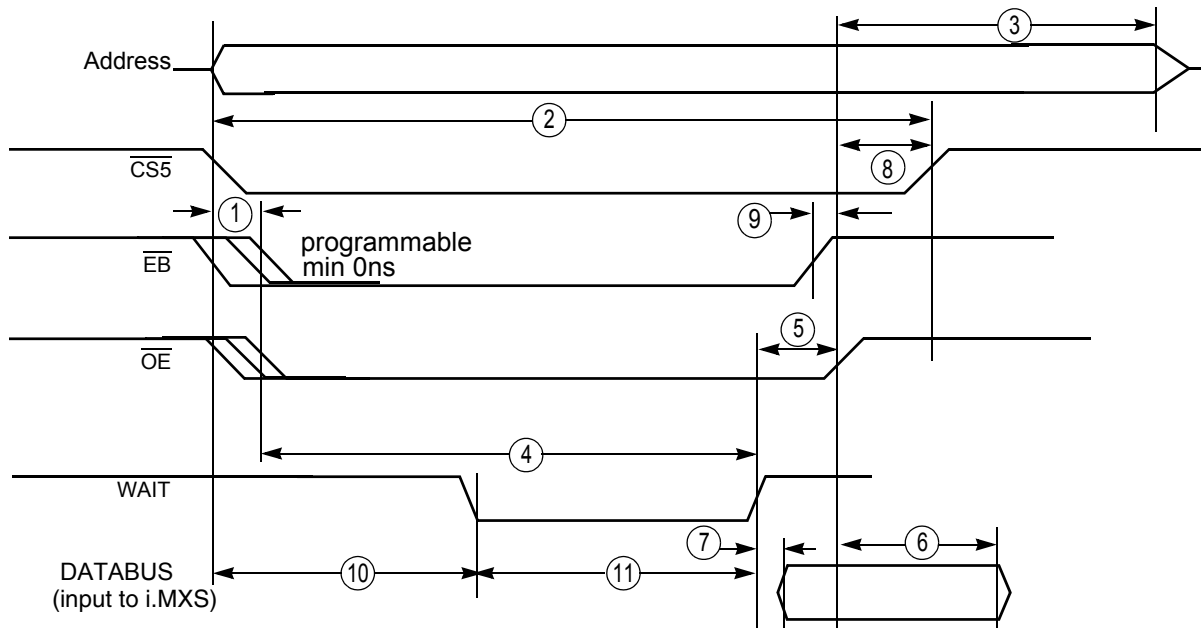


Figure 6. WAIT Read Cycle without DMA

Table 13. WAIT Read Cycle without DMA: WSC = 111111, DTACK\_SEL=1, HCLK=96MHz

| Number | Characteristic                                     | 3.0 ± 0.3 V |           | Unit |
|--------|--|-------------|-----------|------|
|        |  | Minimum     | Maximum   |      |
| 1      | $\overline{OE}$ and $\overline{EB}$ assertion time | See note 2  | –         | ns   |
| 2      | $\overline{CS5}$ pulse width                       | 3T          | –         | ns   |
| 3      | $\overline{OE}$ negated to address inactive        | 56.81       | 57.28     | ns   |
| 4      | Wait asserted after $\overline{OE}$ asserted       | –           | 1020T     | ns   |
| 5      | Wait asserted to $\overline{OE}$ negated           | 2T+1.57     | 3T+7.33   | ns   |
| 6      | Data hold timing after $\overline{OE}$ negated     | T-1.49      | –         | ns   |
| 7      | Data ready after wait asserted                     | 0           | T         | ns   |
| 8      | OE negated to CS negated                           | 1.5T-0.68   | 1.5T-0.06 | ns   |
| 9      | OE negated after EB negated                        | 0.06        | 0.18      | ns   |
| 10     | Become low after CS5 asserted                      | 0           | 1019T     | ns   |
| 11     | Wait pulse width                                   | 1T          | 1020T     | ns   |

**Note:**

1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2.  $\overline{OE}$  and  $\overline{EB}$  assertion time is programmable by OEA bit in CS5L register.  $\overline{EB}$  assertion in read cycle will occur only when EBC bit in CS5L register is clear.
3. Address becomes valid and CS asserts at the start of read access cycle.
4. The external wait input requirement is eliminated when CS5 is programmed to use internal wait state.

### 4.4.2.2 WAIT Read Cycle DMA Enabled

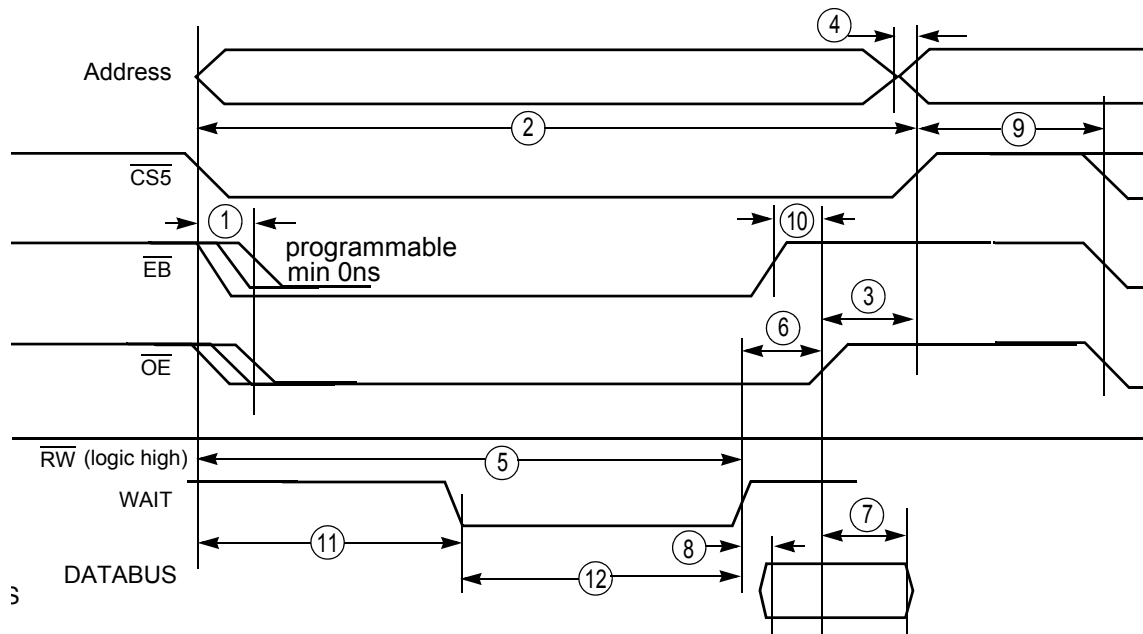


Figure 7. DTACK WAIT Read Cycle DMA Enabled

Table 14. DTACK WAIT Read Cycle DMA Enabled: WSC = 111111, DTACK\_SEL=1, HCLK=96MHz

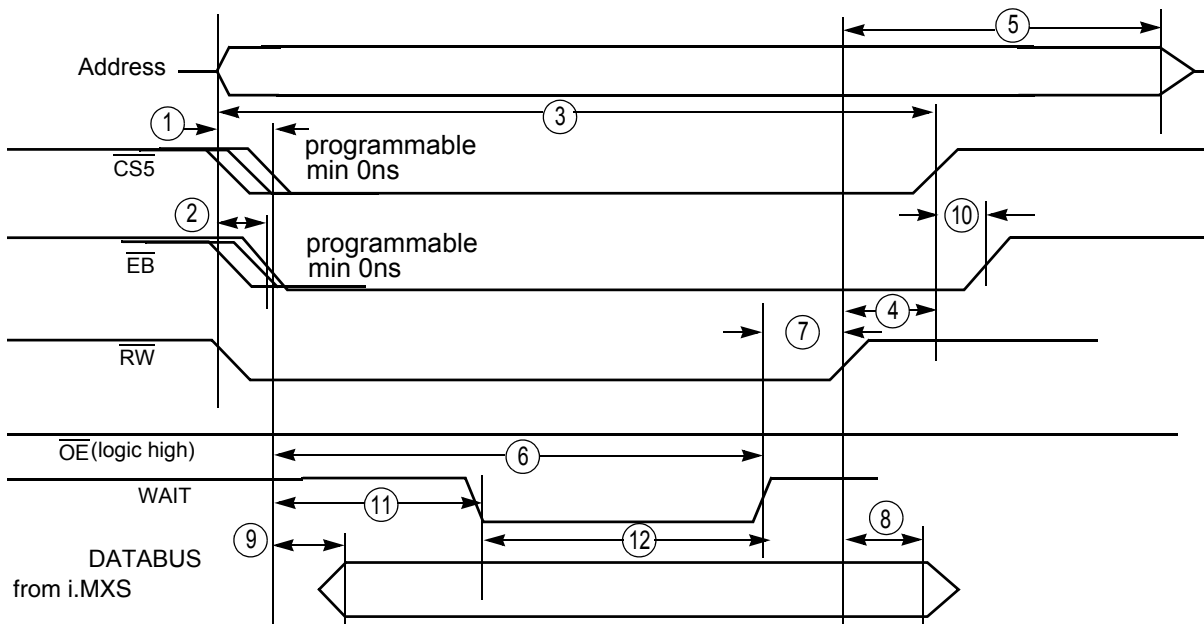
| Number | Characteristic   | 3.0 ± 0.3 V |           | Unit |
|--------|--|-------------|-----------|------|
|        |  | Minimum     | Maximum   |      |
| 1      | $\overline{OE}$ and $\overline{EB}$ assertion time         | See note 2  | –         | ns   |
| 2      | $\overline{CS5}$ pulse width                               | 3T          | –         | ns   |
| 3      | $\overline{OE}$ negated before $\overline{CS5}$ is negated | 1.5T-0.68   | 1.5T-0.06 | ns   |
| 4      | Address inactivated before $\overline{CS5}$ negated        | –           | 0.05      | ns   |
| 5      | Wait asserted after $\overline{CS5}$ asserted              | –           | 1020T     | ns   |
| 6      | Wait asserted to $\overline{OE}$ negated                   | 2T+1.57     | 3T+7.33   | ns   |
| 7      | Data hold timing after $\overline{OE}$ negated             | T-1.49      | –         | ns   |
| 8      | Data ready after wait is asserted                          | –           | T         | ns   |
| 9      | $\overline{CS5}$ deactive to next $\overline{CS5}$ active  | T           | –         | ns   |
| 10     | OE negate after EB negate                                  | 0.06        | 0.18      | ns   |
| 11     | Wait becomes low after CS5 asserted                        | 0           | 1019T     | ns   |

**Table 14. DTACK WAIT Read Cycle DMA Enabled: WSC = 111111, DTACK\_SEL=1, HCLK=96MHz (Continued)**

| Number | Characteristic   | 3.0 ± 0.3 V |         | Unit |
|--------|------------------|-------------|---------|------|
|        |                  | Minimum     | Maximum |      |
| 12     | Wait pulse width | 1T          | 1020T   | ns   |

**Note:**  
 1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)  
 2.  $\overline{OE}$  and  $\overline{EB}$  assertion time is programmable by OEA bit in CS5L register.  $\overline{EB}$  assertion in read cycle will occur only when EBC bit in CS5L register is clear.  
 3. Address becomes valid and CS asserts at the start of read access cycle.  
 4. The external wait input requirement is eliminated when CS5 is programmed to use internal wait state.

### 4.4.2.3 WAIT Write Cycle without DMA



**Figure 8. WAIT Write Cycle without DMA**

**Table 15. WAIT Write Cycle without DMA: WSC = 111111, DTACK\_SEL=1, HCLK=96MHz**

| Number | Characteristic   | 3.0 ± 0.3 V |           | Unit |
|--------|--|-------------|-----------|------|
|        |  | Minimum     | Maximum   |      |
| 1      | $\overline{CS5}$ assertion time                            | See note 2  | -         | ns   |
| 2      | $\overline{EB}$ assertion time                             | See note 2  | -         | ns   |
| 3      | $\overline{CS5}$ pulse width                               | 3T          | -         | ns   |
| 4      | $\overline{RW}$ negated before $\overline{CS5}$ is negated | 2.5T-3.63   | 2.5T-1.16 | ns   |
| 5      | $\overline{RW}$ negated to Address inactive                | 64.22       | -         | ns   |
| 6      | Wait asserted after $\overline{CS5}$ asserted              | -           | 1020T     | ns   |

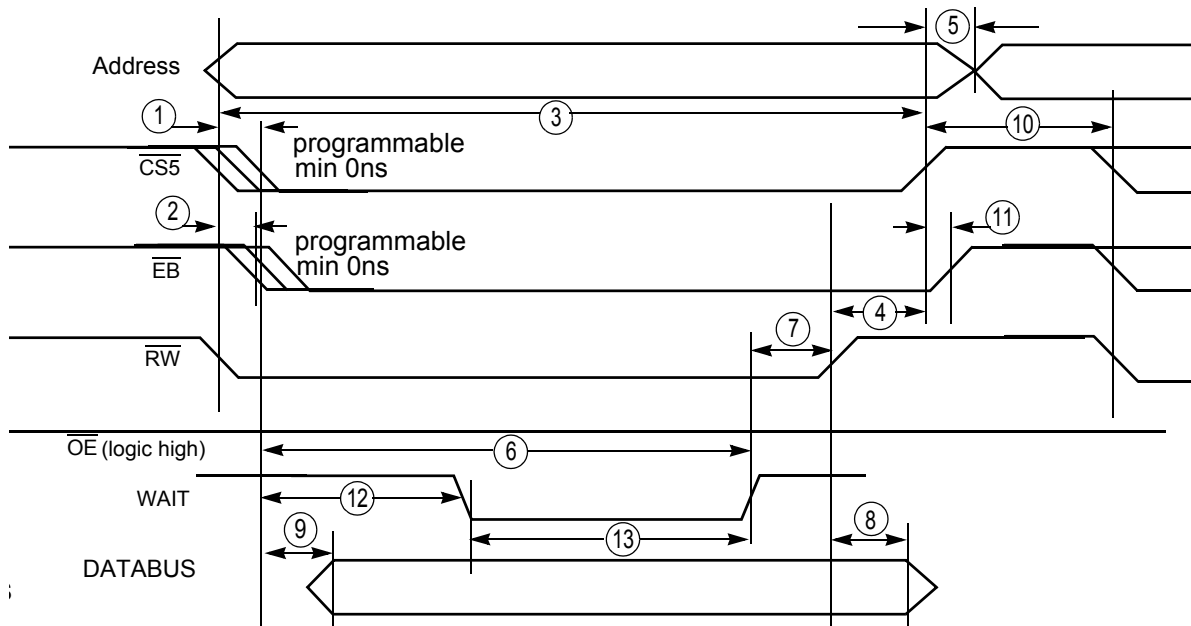
**Table 15. WAIT Write Cycle without DMA: WSC = 111111, DTACK\_SEL=1, HCLK=96MHz (Continued)**

| Number | Characteristic  | 3.0 ± 0.3 V |          | Unit |
|--------|---|-------------|----------|------|
|        |   | Minimum     | Maximum  |      |
| 7      | Wait asserted to $\overline{RW}$ negated                  | T+2.66      | 2T+7.96  | ns   |
| 8      | Data hold timing after $\overline{RW}$ negated            | 2T+0.03     | –        | ns   |
| 9      | Data ready after $\overline{CS5}$ is asserted             | –           | T        | ns   |
| 10     | $\overline{EB}$ negated after $\overline{CS5}$ is negated | 0.5T        | 0.5T+0.5 | ns   |
| 11     | Wait becomes low after $\overline{CS5}$ asserted          | 0           | 1019T    | ns   |
| 12     | Wait pulse width  | 1T          | 1020T    | ns   |

**Note:**

1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2.  $\overline{CS5}$  assertion can be controlled by CSA bits.  $\overline{EB}$  assertion can also be programmable by WEA bits in CS5L register.
3. Address becomes valid and  $\overline{RW}$  asserts at the start of write access cycle.
4. The external wait input requirement is eliminated when CS5 is programmed to use internal wait state.

**4.4.2.4 WAIT Write Cycle DMA Enabled**



**Figure 9. WAIT Write Cycle DMA Enabled**

Table 16. WAIT Write Cycle DMA Enabled: WSC = 111111, DTACK\_SEL=1, HCLK=96MHz

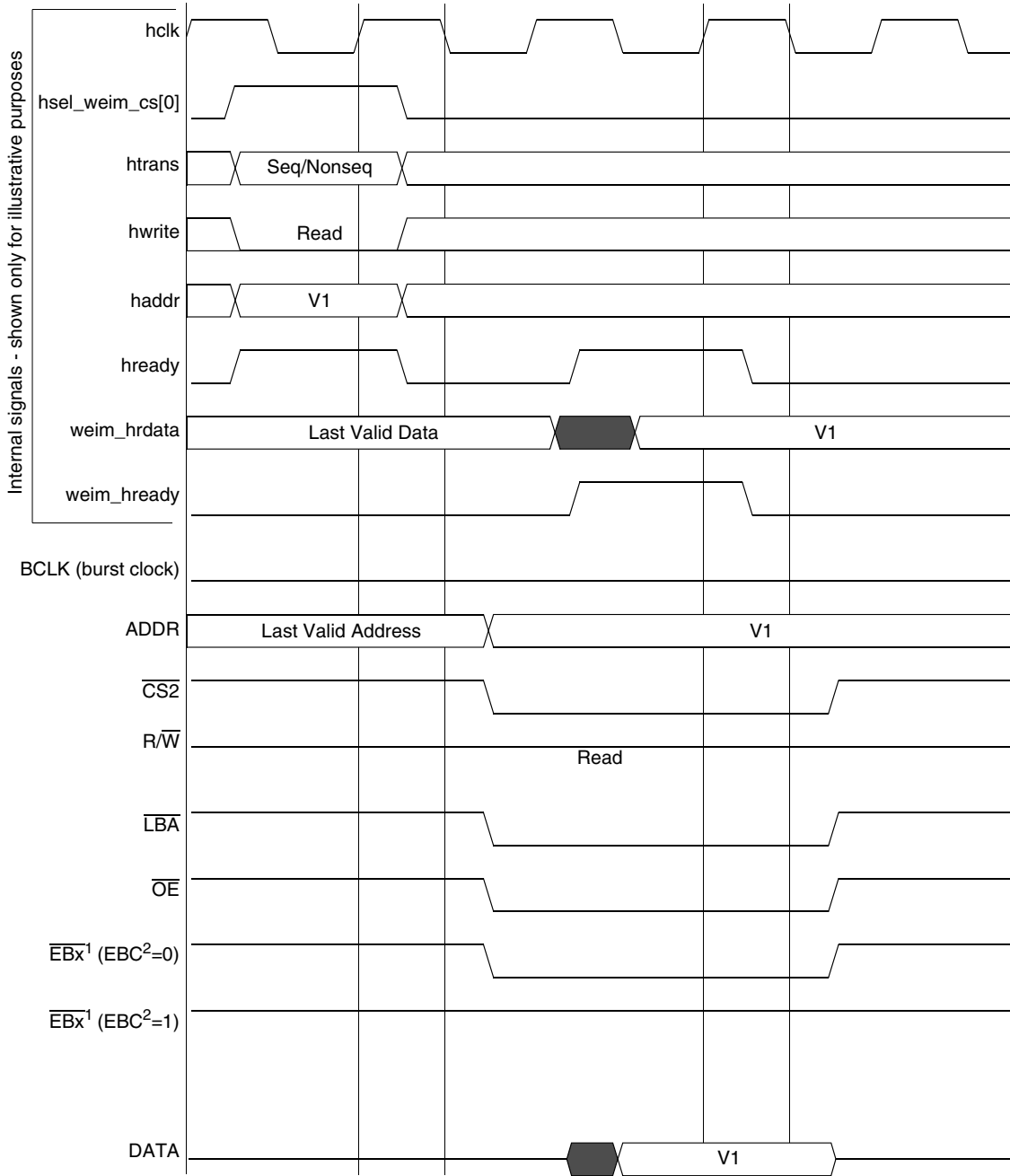
| Number | Characteristic   | 3.0 ± 0.3 V |           | Unit |
|--------|--|-------------|-----------|------|
|        |  | Minimum     | Maximum   |      |
| 1      | $\overline{CS5}$ assertion time                            | See note 2  | –         | ns   |
| 2      | $\overline{EB}$ assertion time                             | See note 2  | –         | ns   |
| 3      | $\overline{CS5}$ pulse width                               | 3T          | –         | ns   |
| 4      | $\overline{RW}$ negated before $\overline{CS5}$ is negated | 2.5T-3.63   | 2.5T-1.16 | ns   |
| 5      | Address inactivated after $\overline{CS}$ negated          | –           | 0.09      | ns   |
| 6      | Wait asserted after $\overline{CS5}$ asserted              | –           | 1020T     | ns   |
| 7      | Wait asserted to $\overline{RW}$ negated                   | T+2.66      | 2T+7.96   | ns   |
| 8      | Data hold timing after $\overline{RW}$ negated             | 2T+0.03     | –         | ns   |
| 9      | Data ready after $\overline{CS5}$ is asserted              | –           | T         | ns   |
| 10     | $\overline{CS}$ deactive to next $\overline{CS}$ active    | T           | –         | ns   |
| 11     | $\overline{EB}$ negate after $\overline{CS}$ negate        | 0.5T        | 0.5T+0.5  |      |
| 12     | Wait becomes low after $\overline{CS5}$ asserted           | 0           | 1019T     | ns   |
| 13     | Wait pulse width   | 1T          | 1020T     | ns   |

**Note:**

1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2.  $\overline{CS5}$  assertion can be controlled by CSA bits.  $\overline{EB}$  assertion also can be programmable by WEA bits in CS5L register.
3. Address becomes valid and  $\overline{RW}$  asserts at the start of write access cycle.
4. The external wait input requirement is eliminated when  $\overline{CS5}$  is programmed to use internal wait state.

### 4.4.3 EIM External Bus Timing

The External Interface Module (EIM) is the interface to devices external to the i.MXS, including generation of chip-selects for external peripherals and memory. The timing diagram for the EIM is shown in Figure 5, and Table 12 defines the parameters of signals.



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 10. WSC = 1, A.HALF/E.HALF**

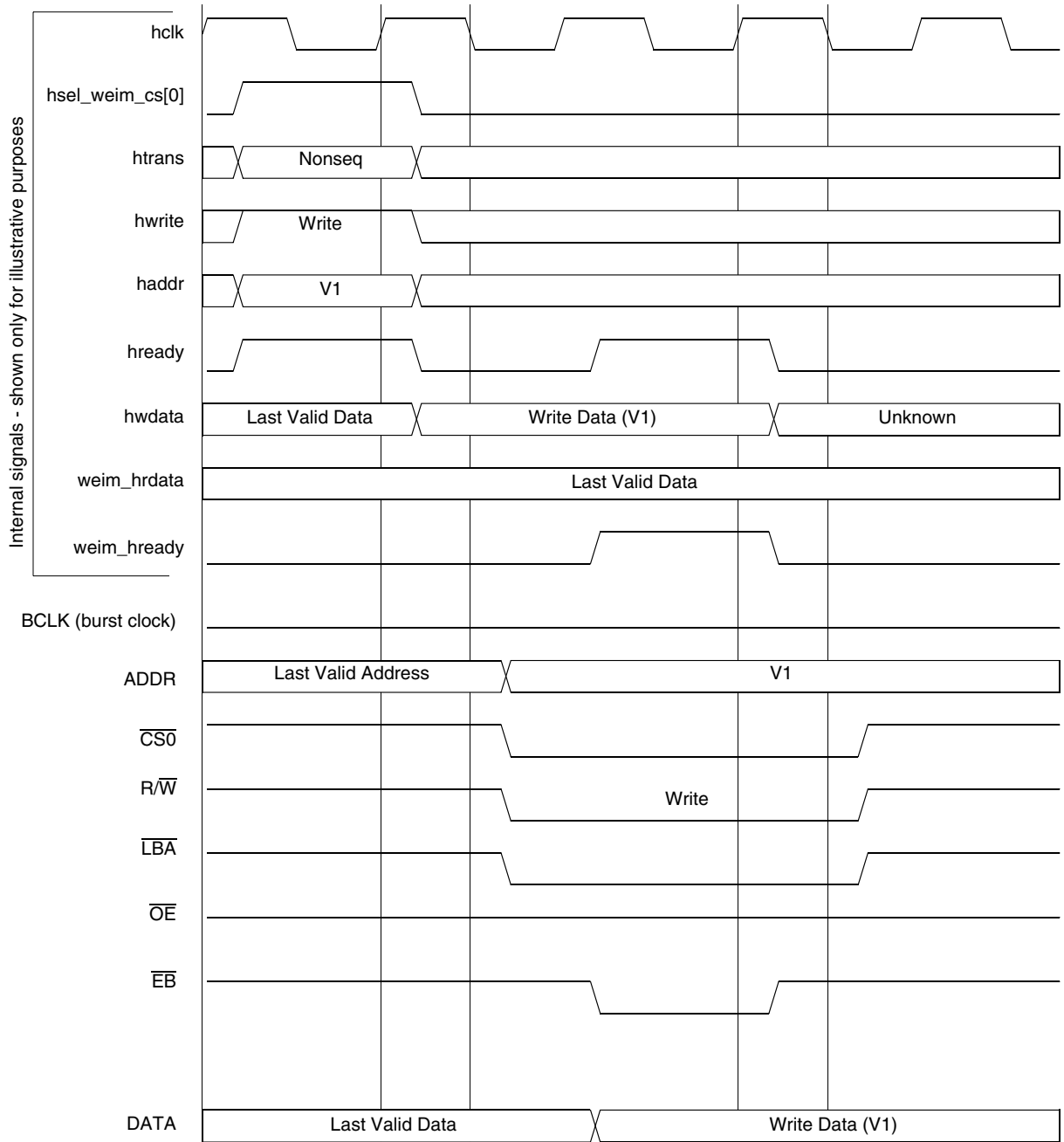
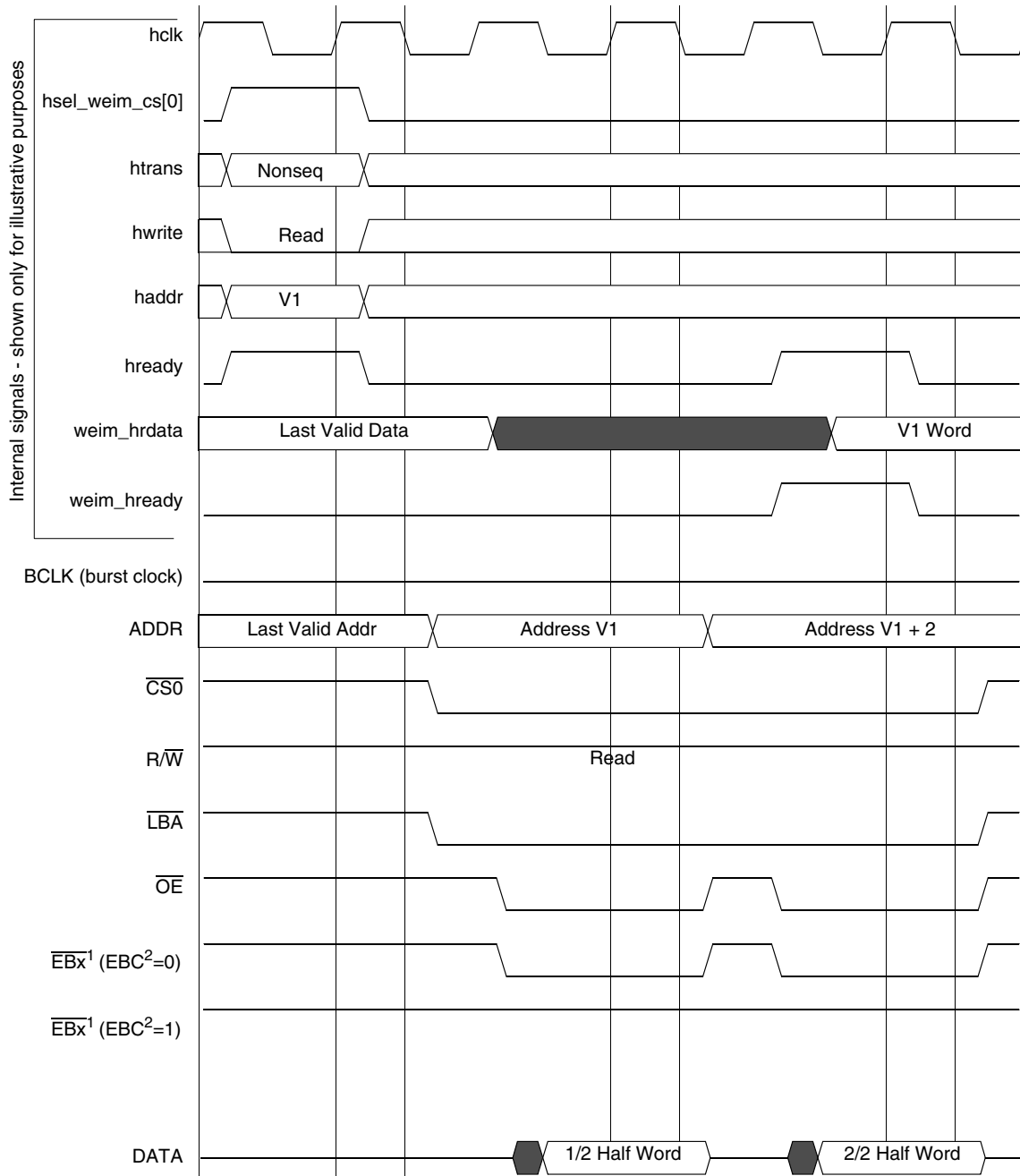


Figure 11. WSC = 1, WEA = 1, WEN = 1, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 12. WSC = 1, OEA = 1, A.WORD/E.HALF**



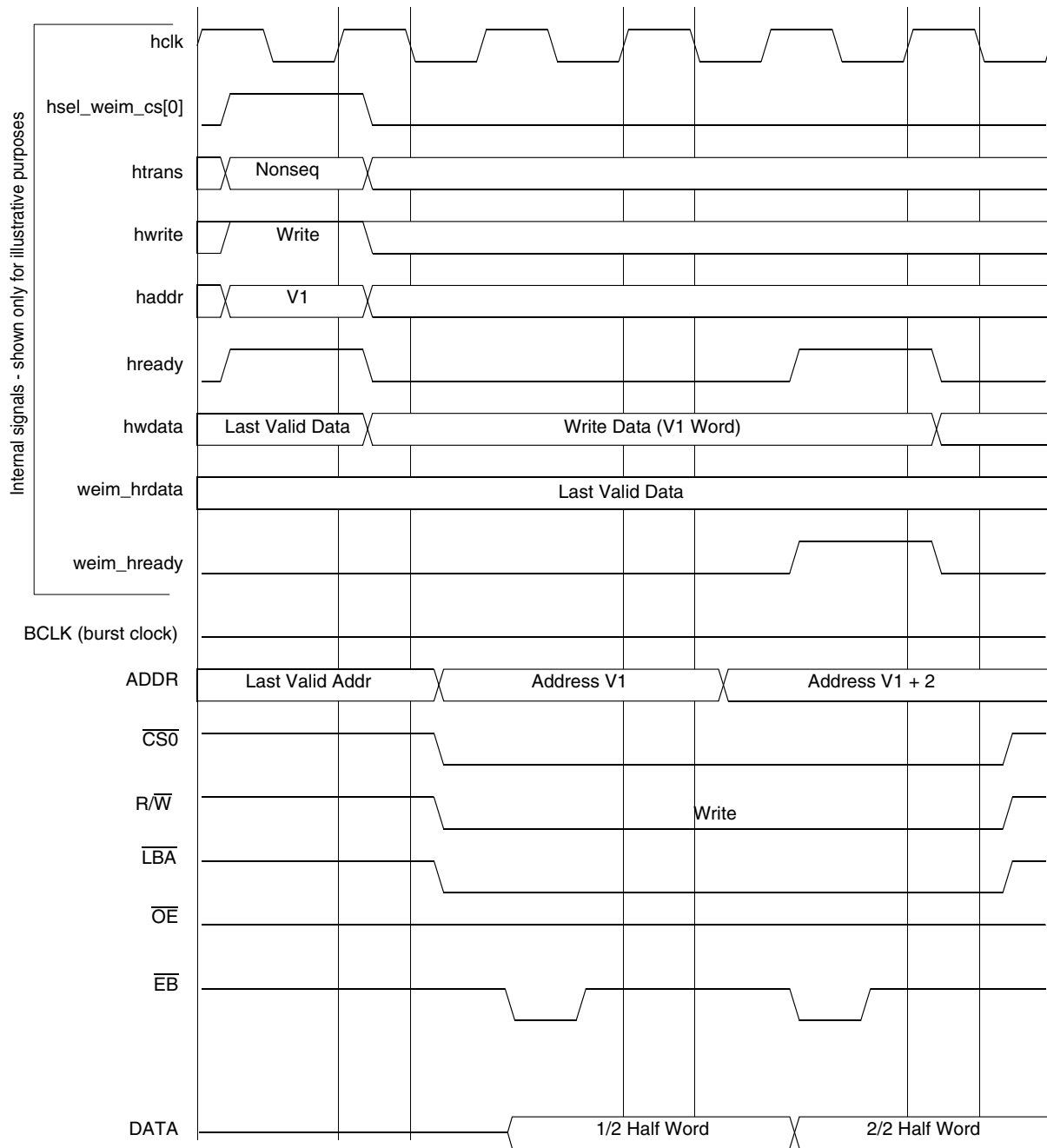
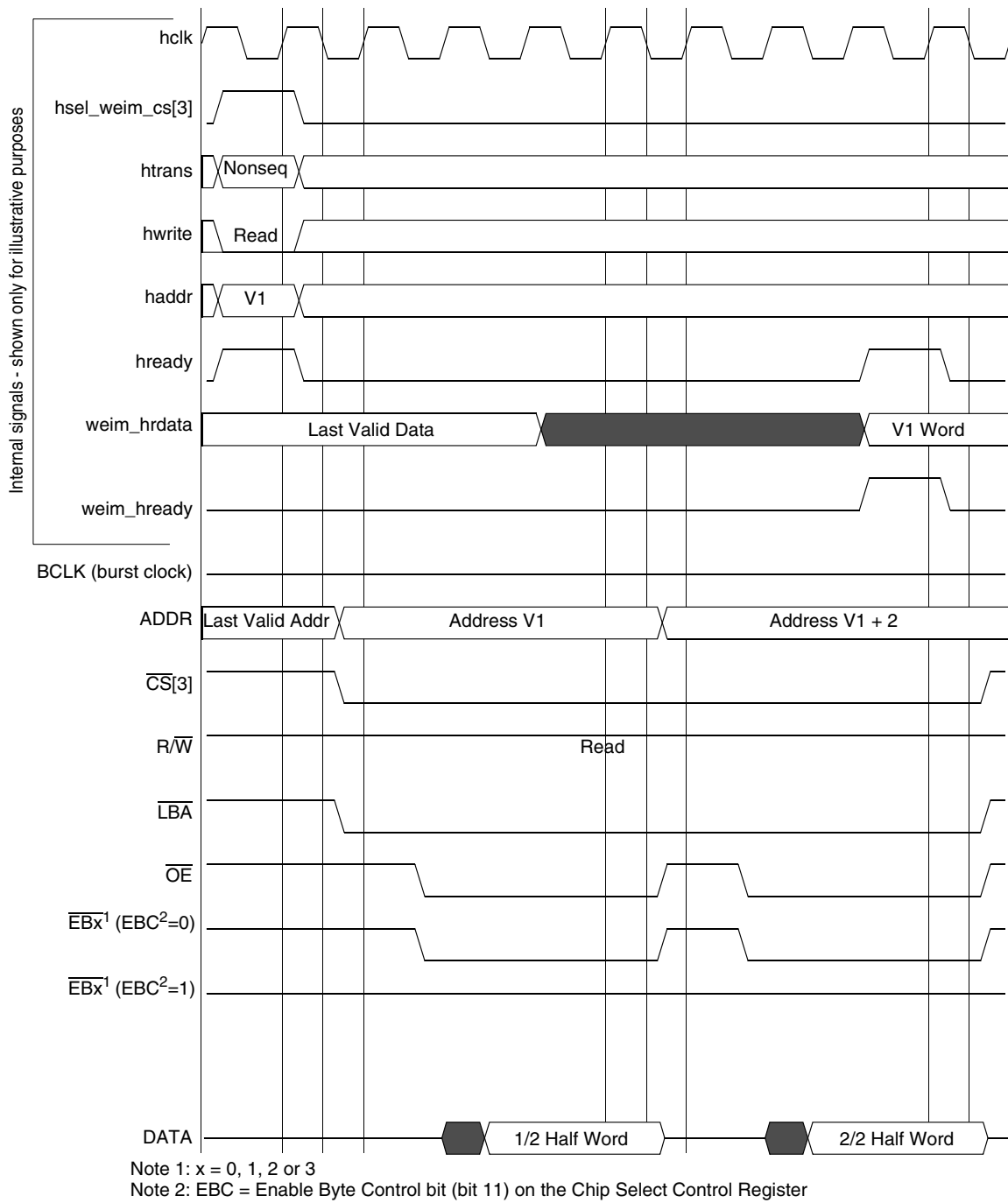


Figure 13. WSC = 1, WEA = 1, WEN = 2, A.WORD/E.HALF



**Figure 14. WSC = 3, OEA = 2, A.WORD/E.HALF**

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: i.MXS Product Family

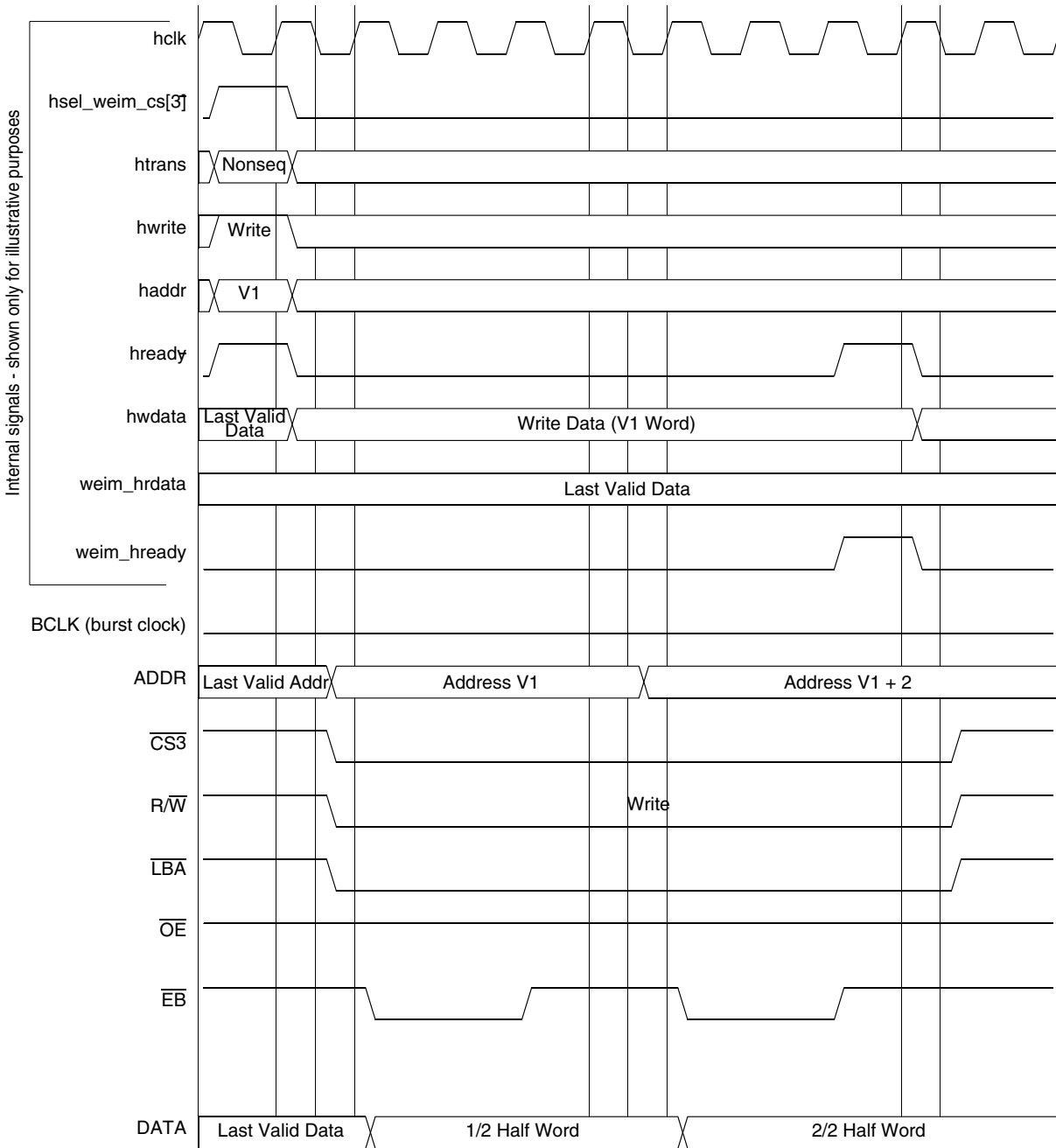
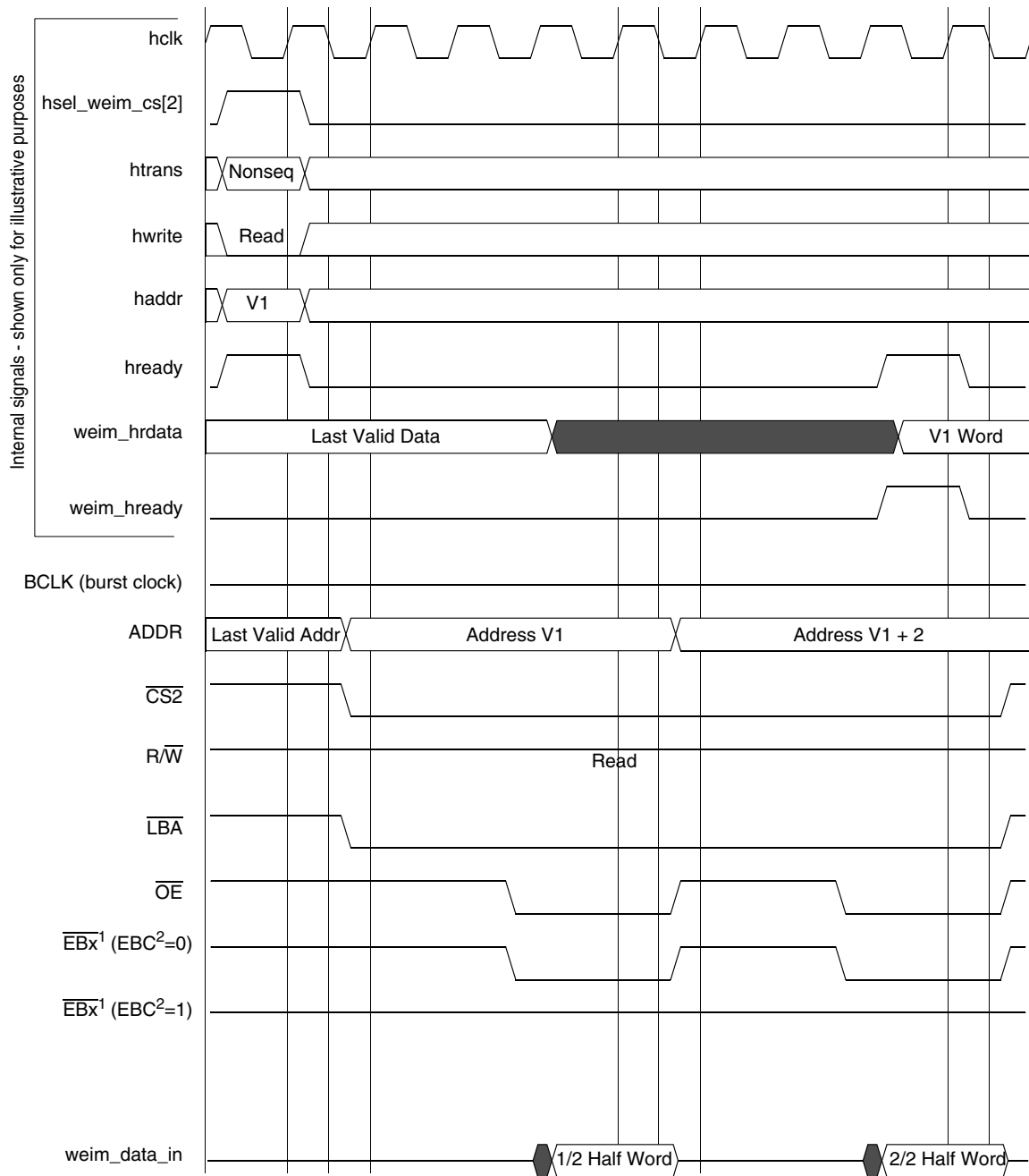


Figure 15. WSC = 3, WEA = 1, WEN = 3, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 16. WSC = 3, OEA = 4, A.WORD/E.HALF**

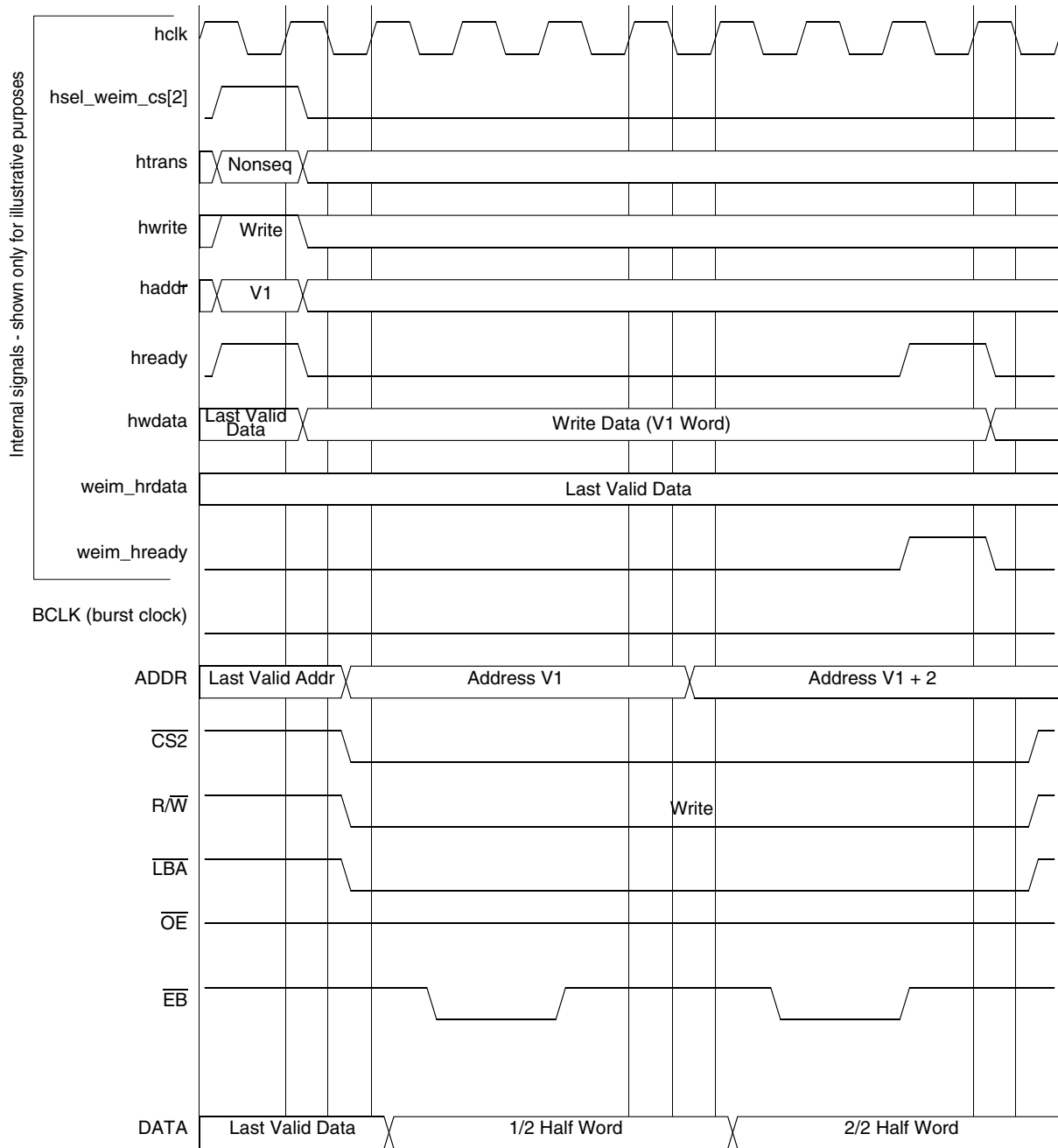
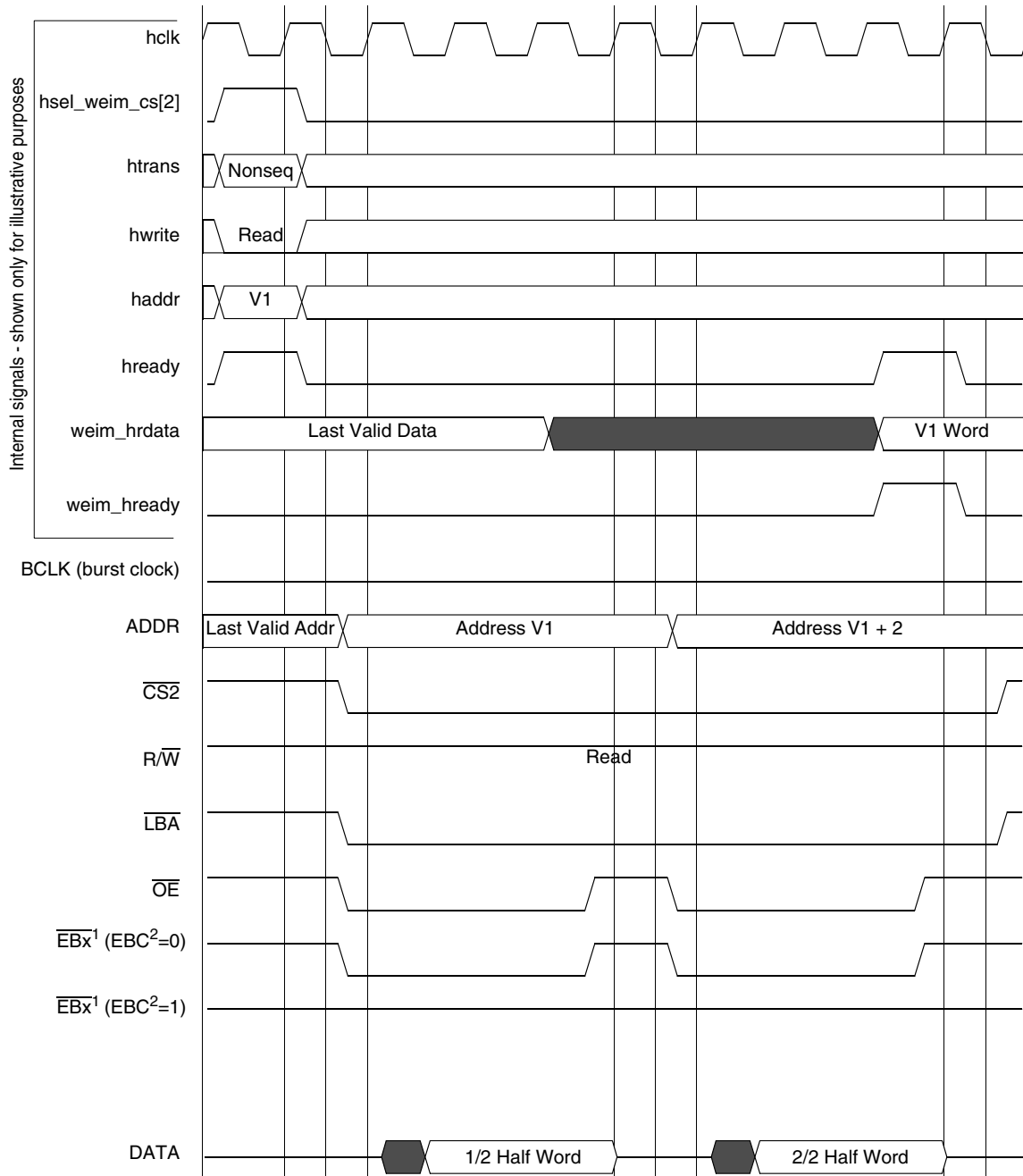


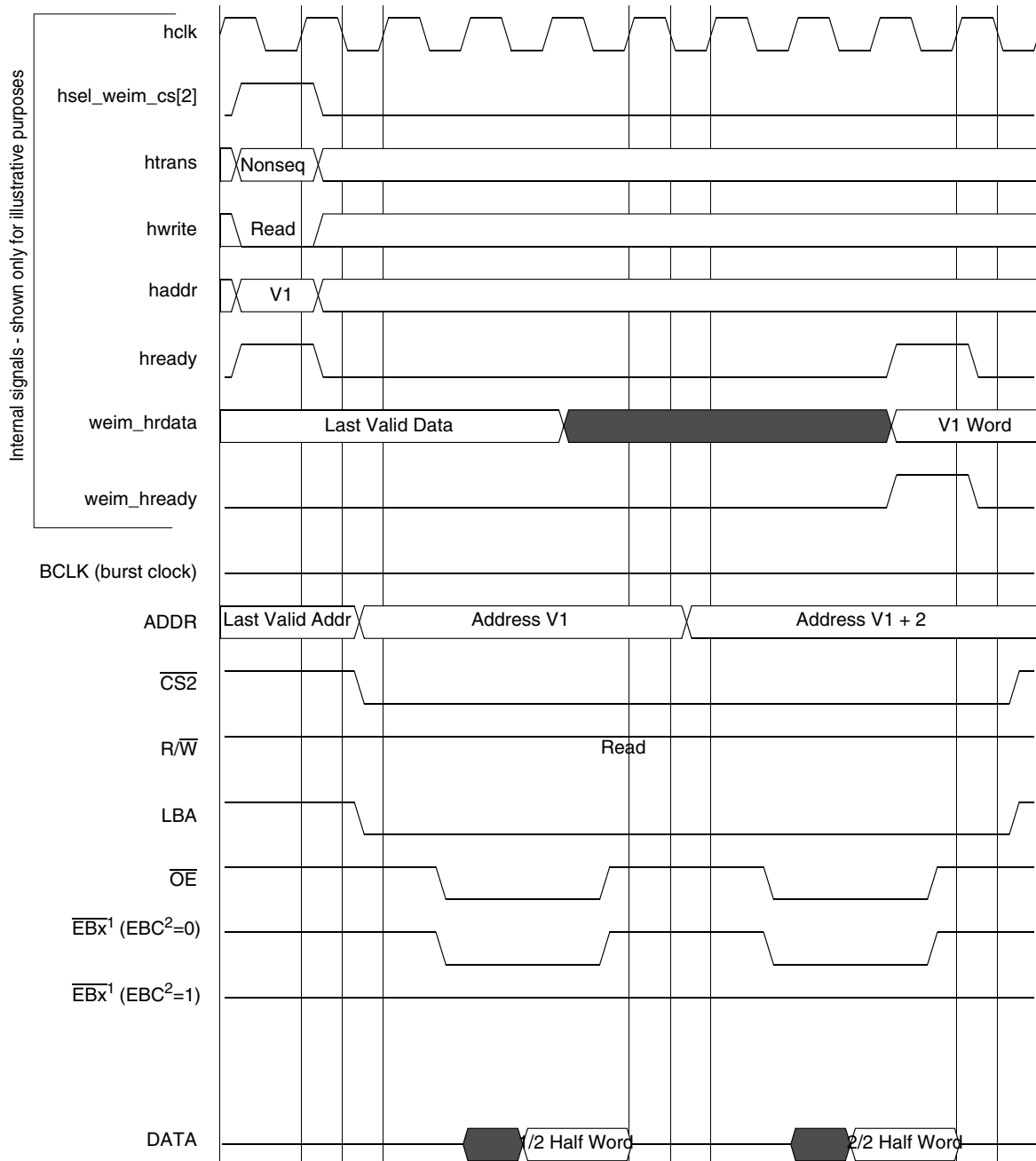
Figure 17. WSC = 3, WEA = 2, WEN = 3, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 18. WSC = 3, OEN = 2, A.WORD/E.HALF**



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 19. WSC = 3, OEA = 2, OEN = 2, A.WORD/E.HALF**

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: i.MXS Product Family

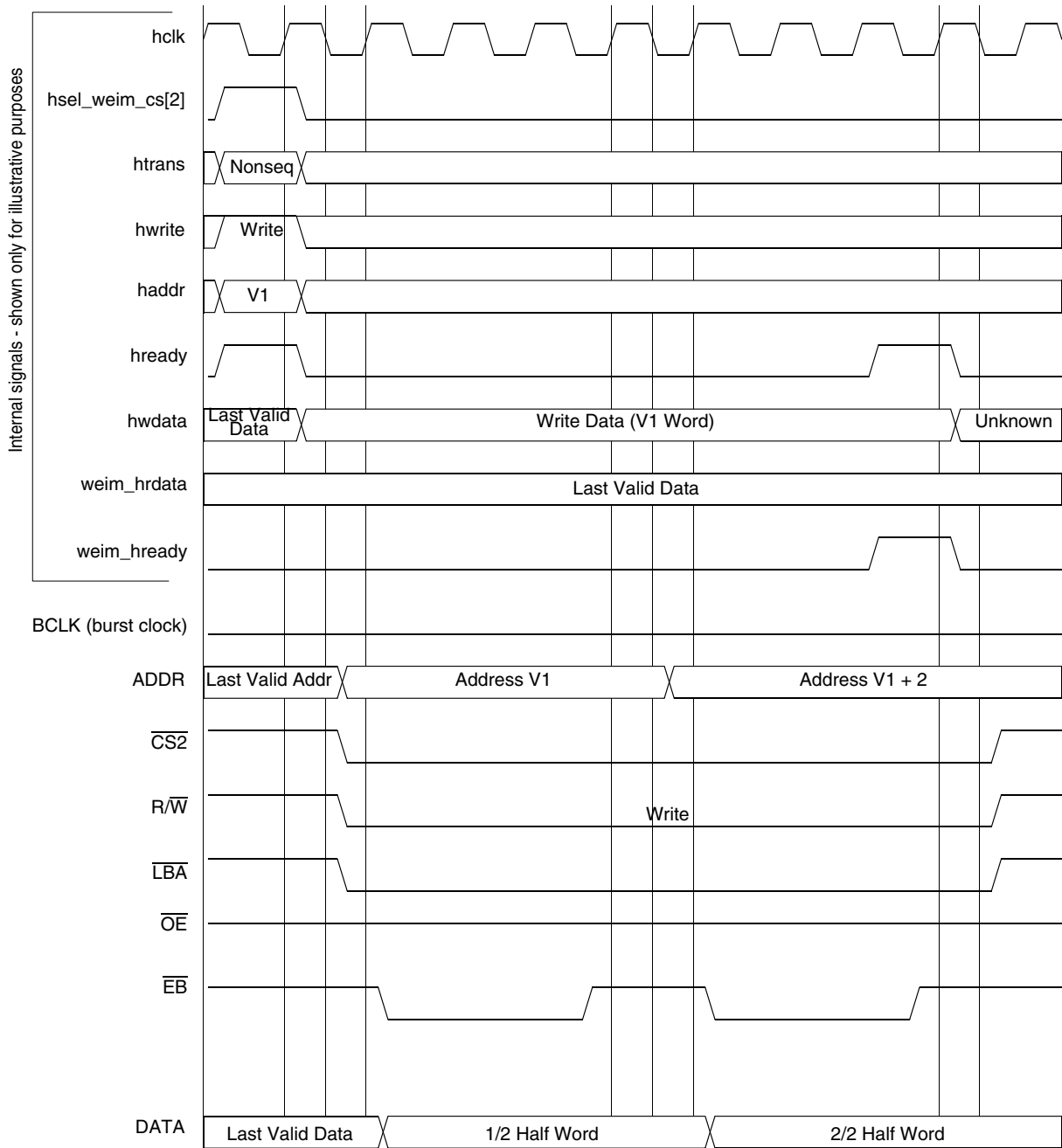


Figure 20. WSC = 2, WWS = 1, WEA = 1, WEN = 2, A.WORD/E.HALF



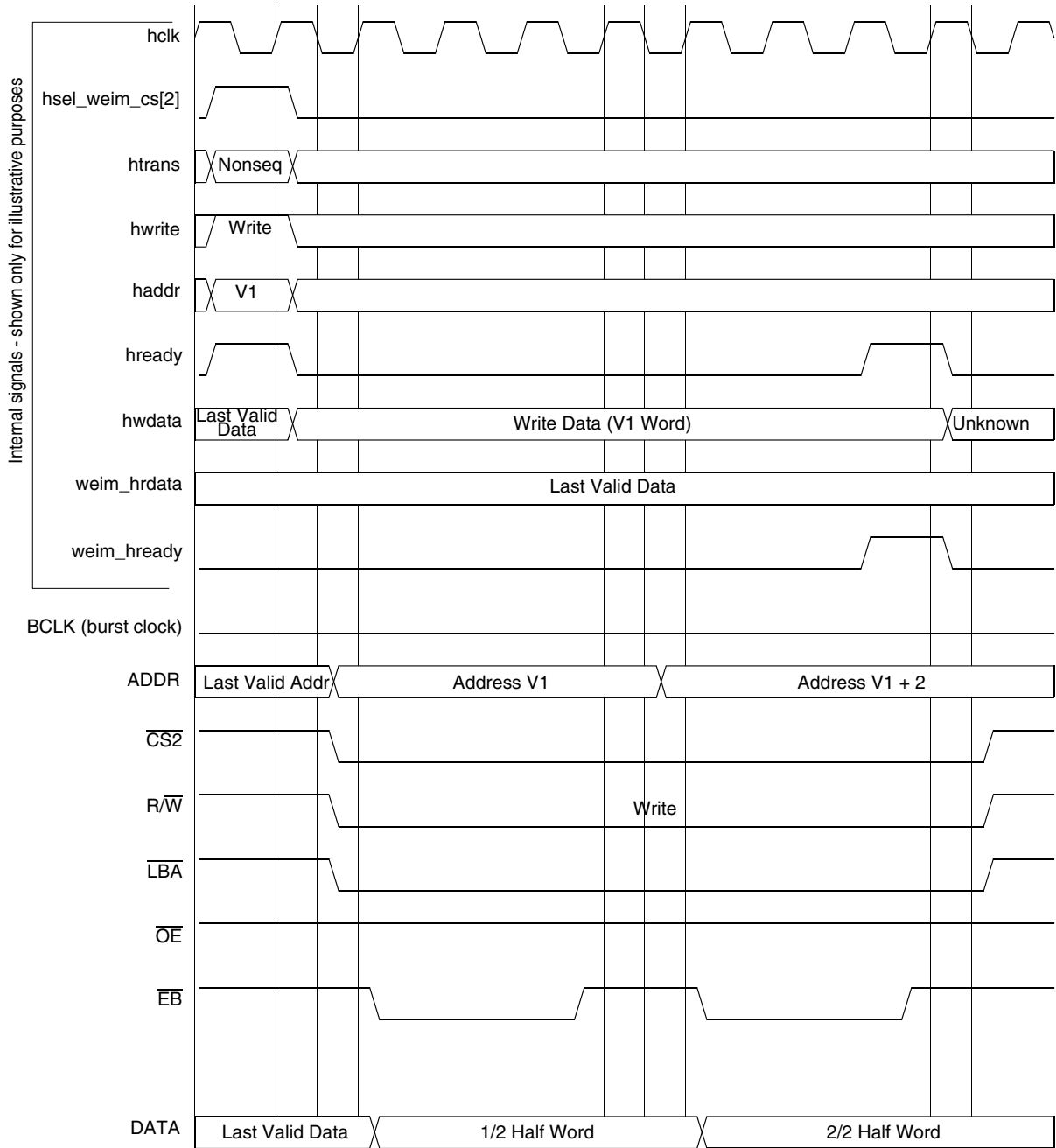
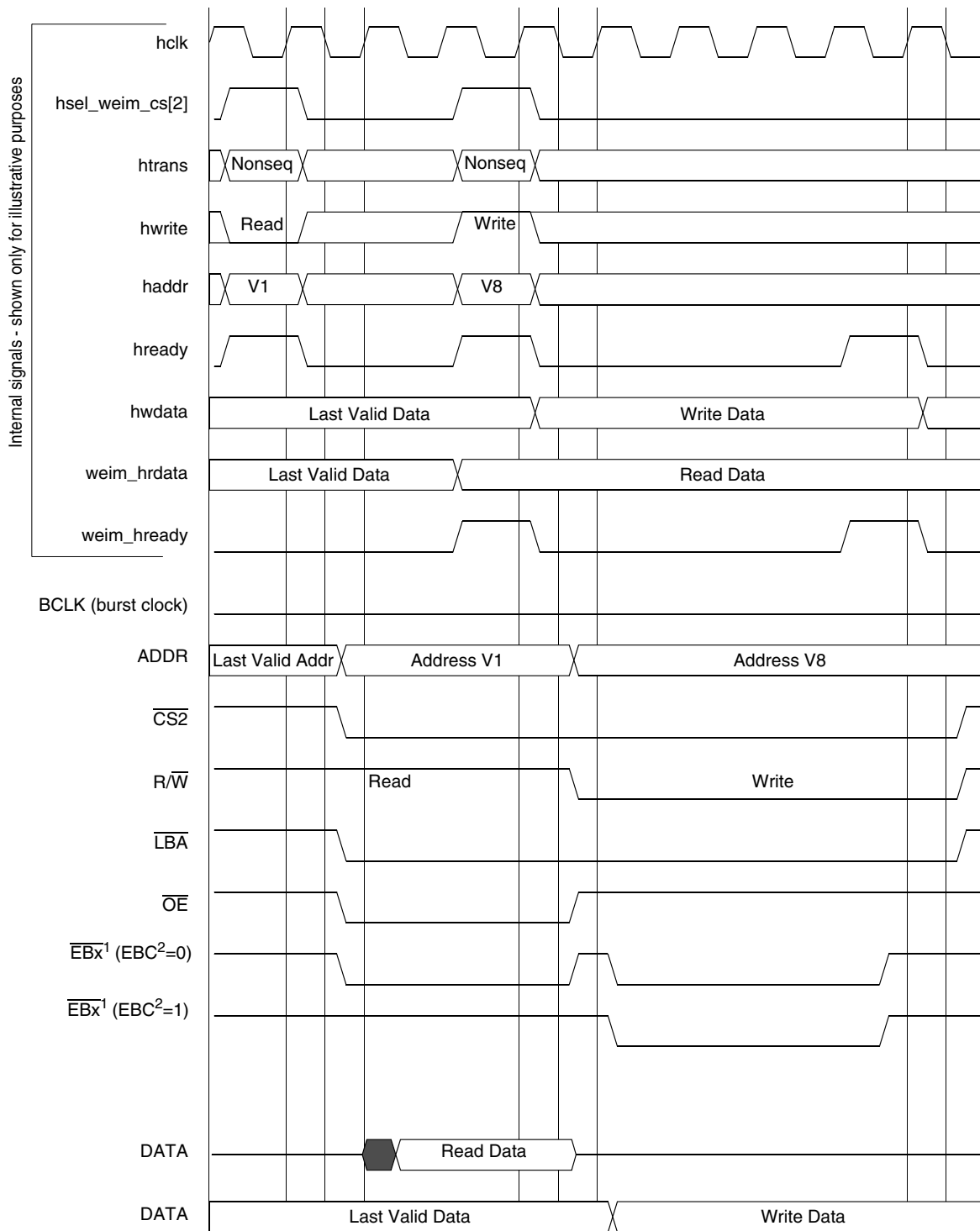


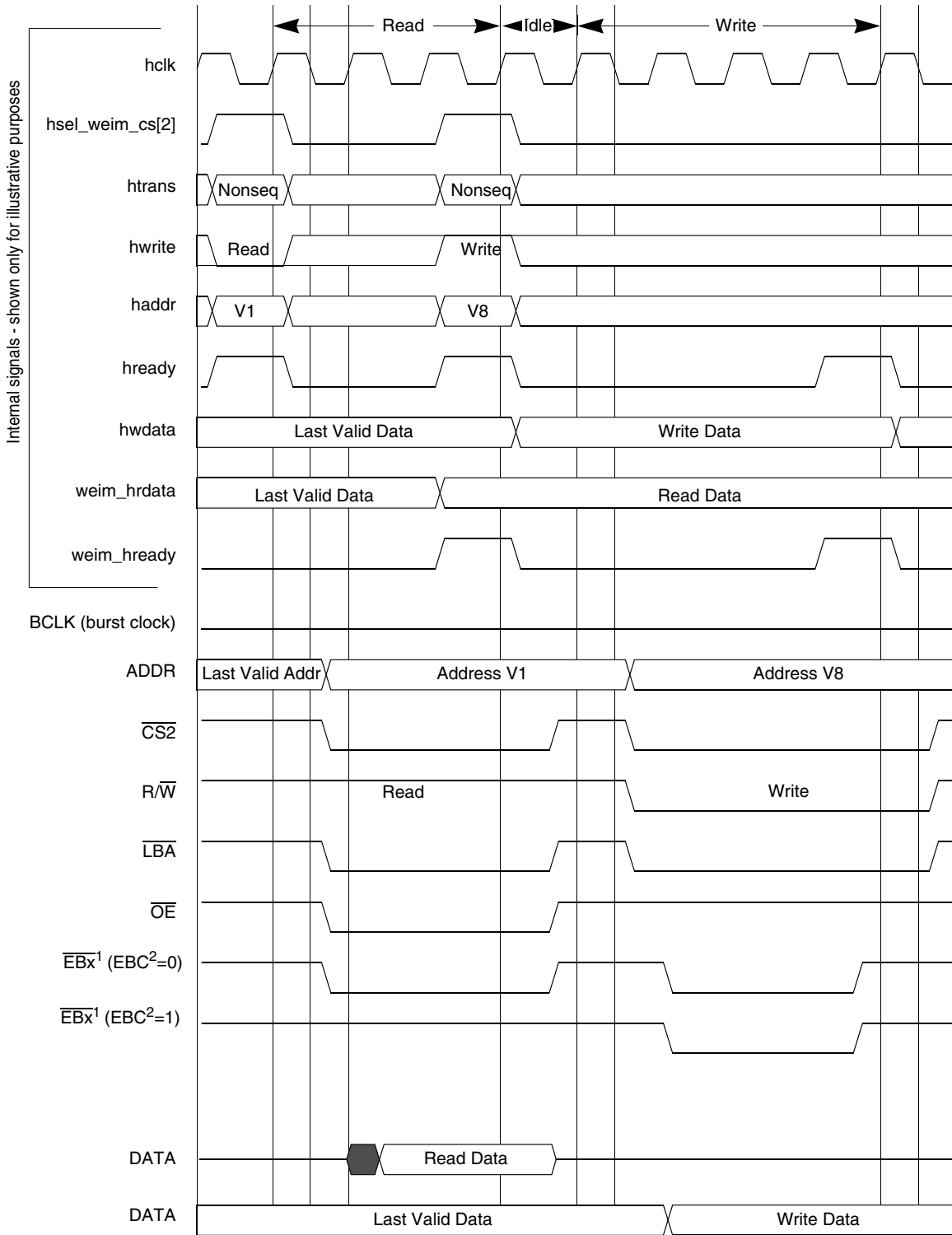
Figure 21. WSC = 1, WWS = 2, WEA = 1, WEN = 2, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 22. WSC = 2, WWS = 2, WEA = 1, WEN = 2, A.HALF/E.HALF**



Note 1: x = 0, 1, 2 or 3  
 Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 23. WSC = 2, WWS = 1, WEA = 1, WEN = 2, EDC = 1, A.HALF/E.HALF**

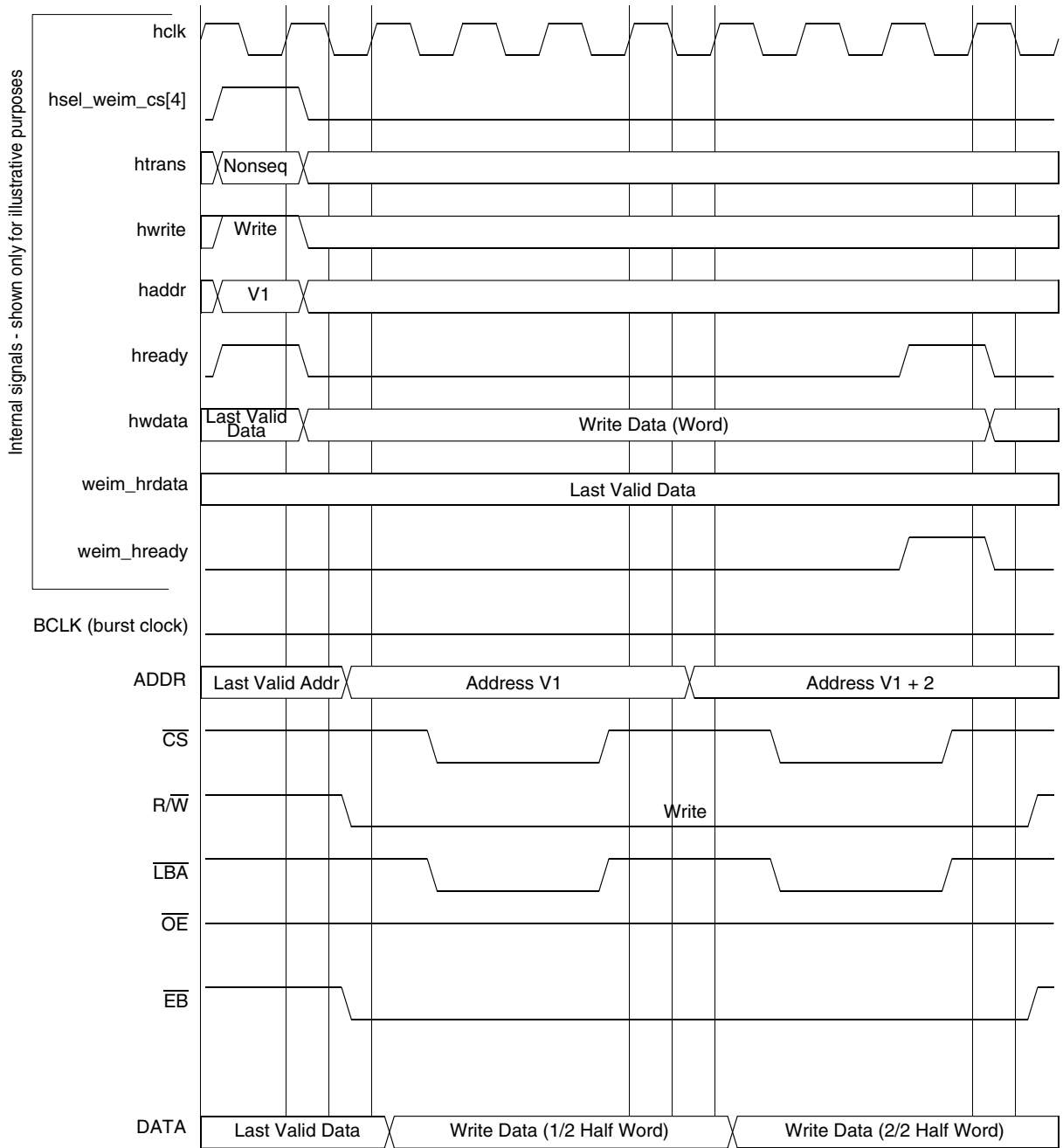
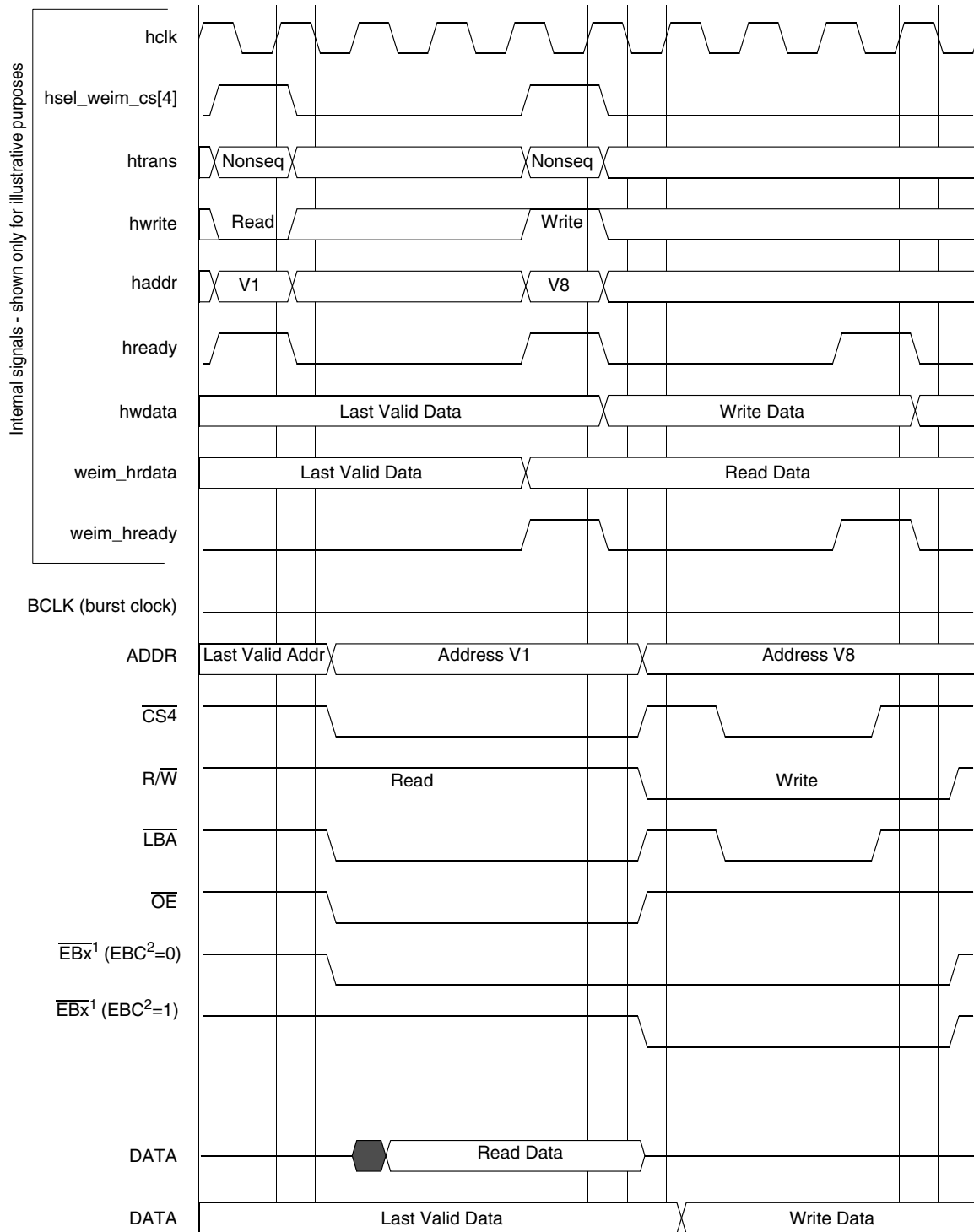
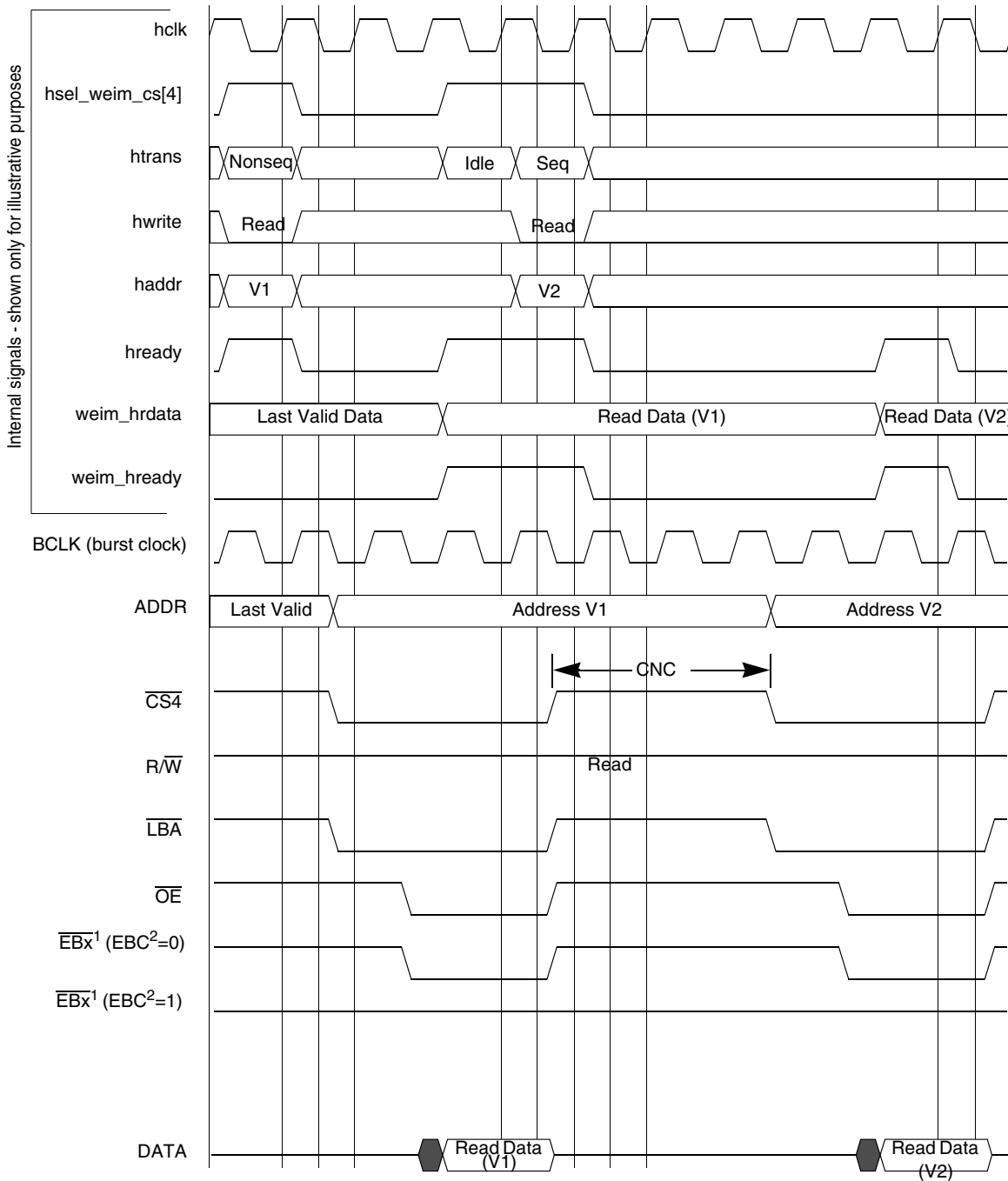


Figure 24. WSC = 2, CSA = 1, WWS = 1, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3  
 Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 25. WSC = 3, CSA = 1, A.HALF/E.HALF**

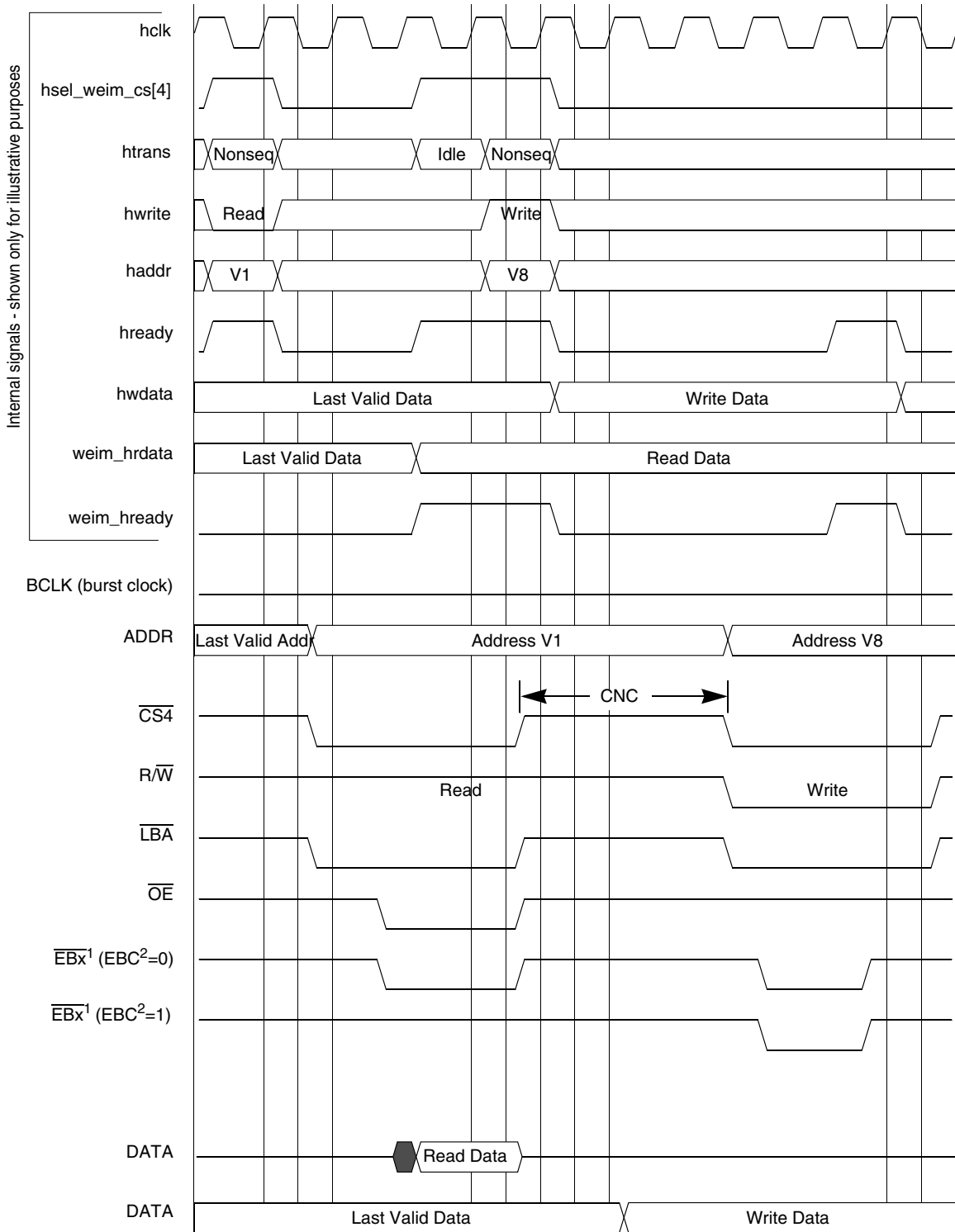


Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 26. WSC = 2, OEA = 2, CNC = 3, BCM = 1, A.HALF/E.HALF**

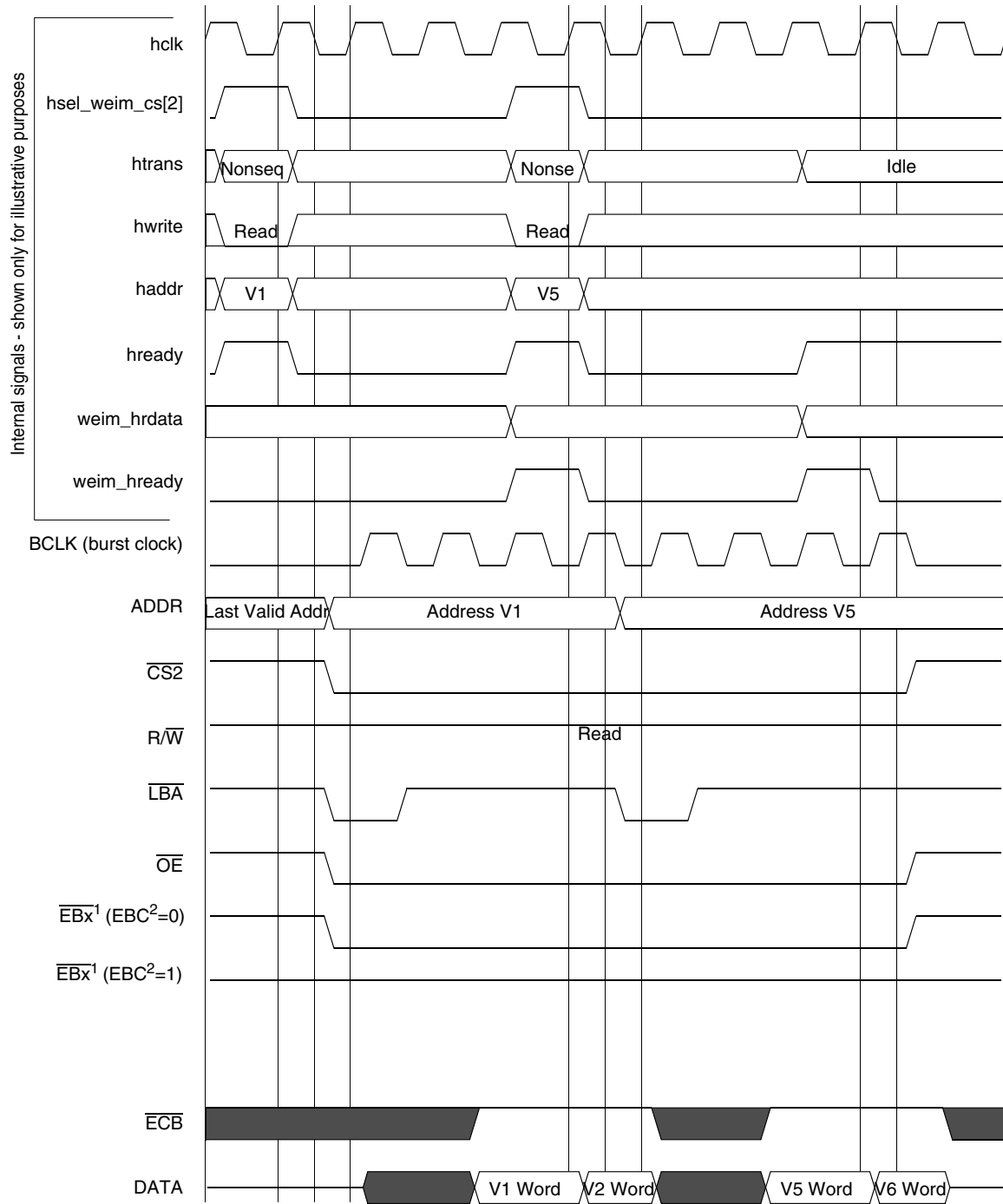
Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: i.MXS Product Family



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

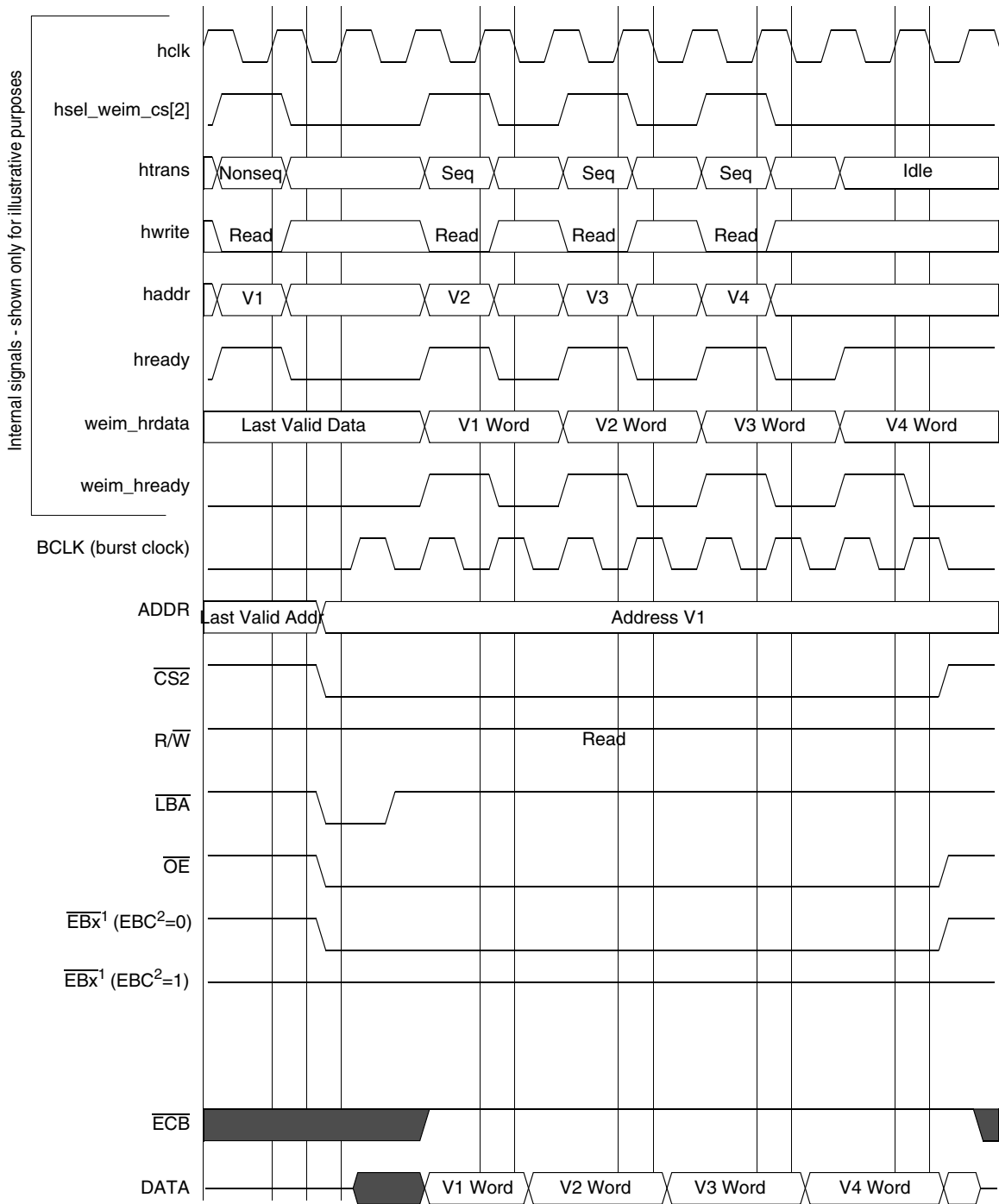
**Figure 27. WSC = 2, OEA = 2, WEA = 1, WEN = 2, CNC = 3, A.HALF/E.HALF**



Note 1: x = 0, 1, 2 or 3  
 Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

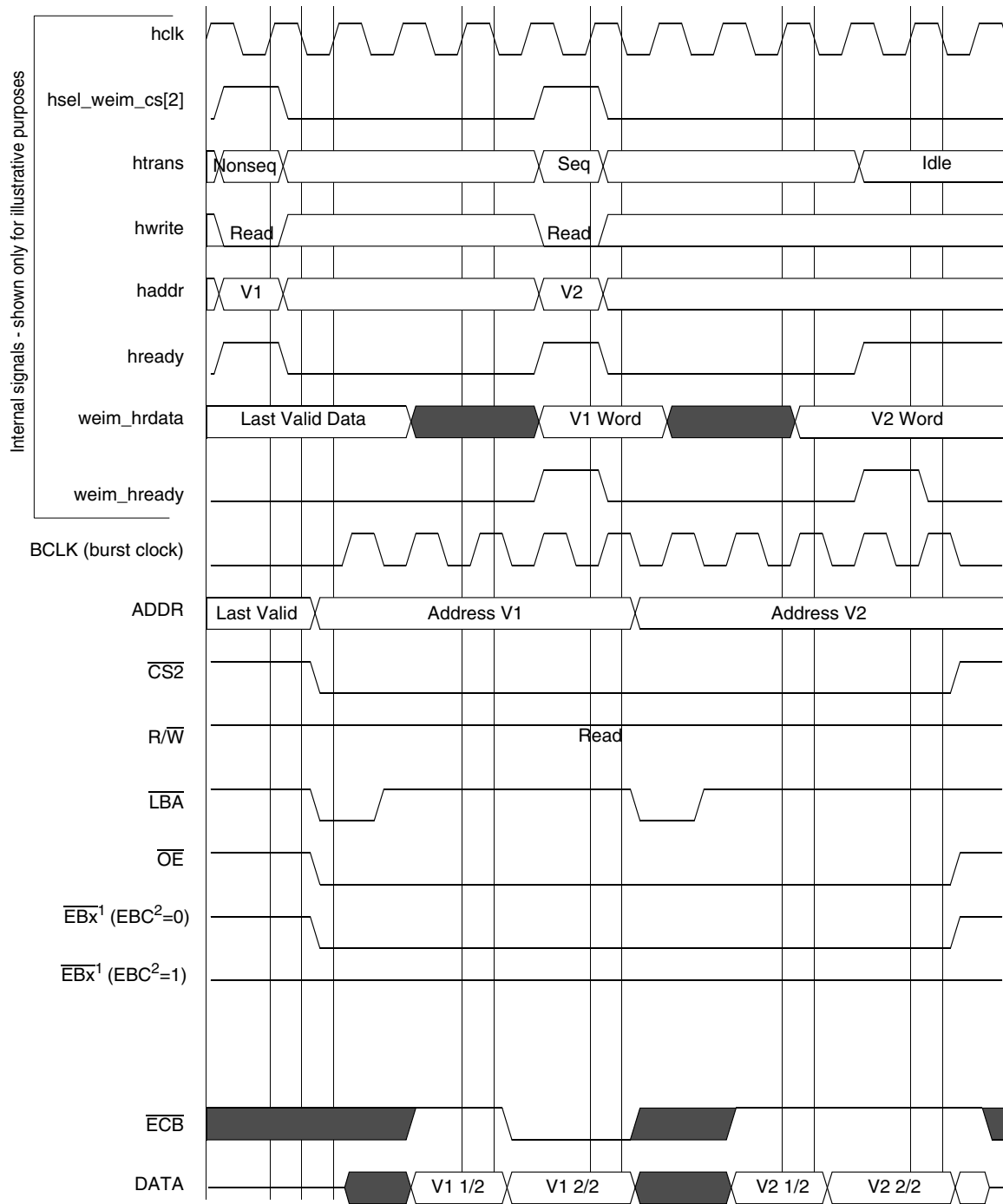
**Figure 28. WSC = 3, SYNC = 1, A.HALF/E.HALF**





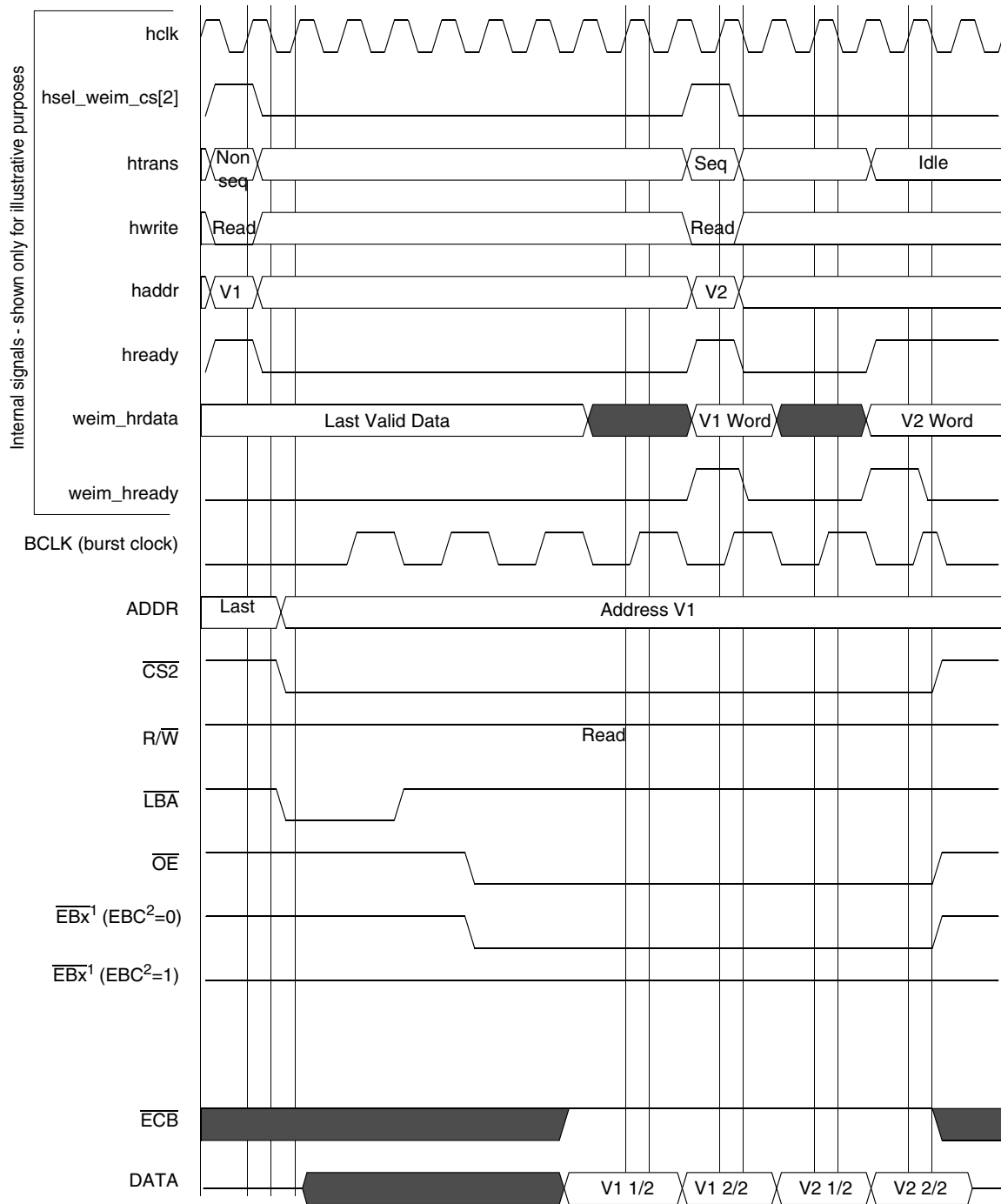
Note 1: x = 0, 1, 2 or 3  
 Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 29. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.WORD**



Note 1: x = 0, 1, 2 or 3  
 Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

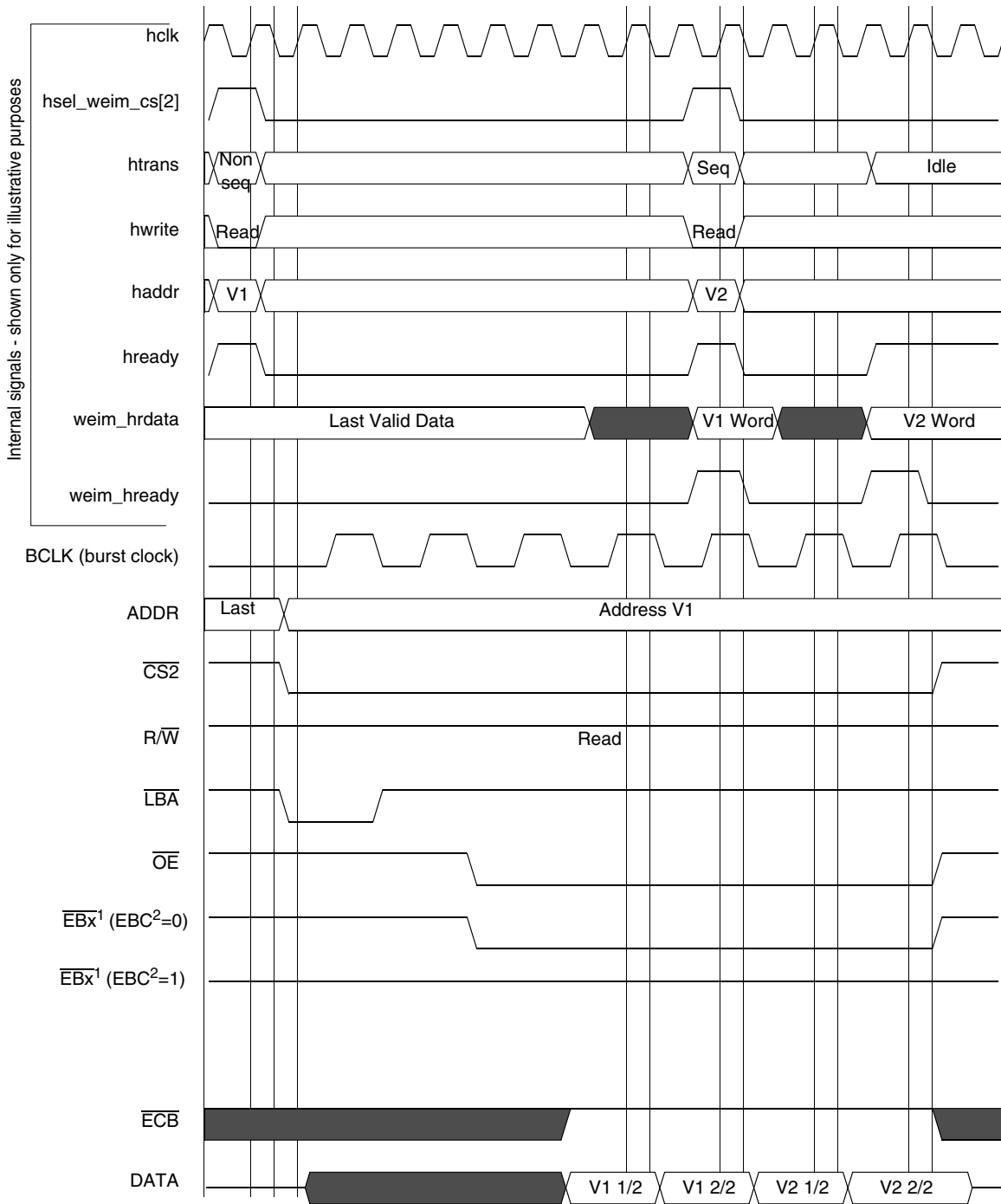
**Figure 30. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.HALF**



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 31. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 2, A.WORD/E.HALF**



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 32. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 1, A.WORD/E.HALF**

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: i.MXS Product Family

#### 4.4.4 Non-TFT Panel Timing

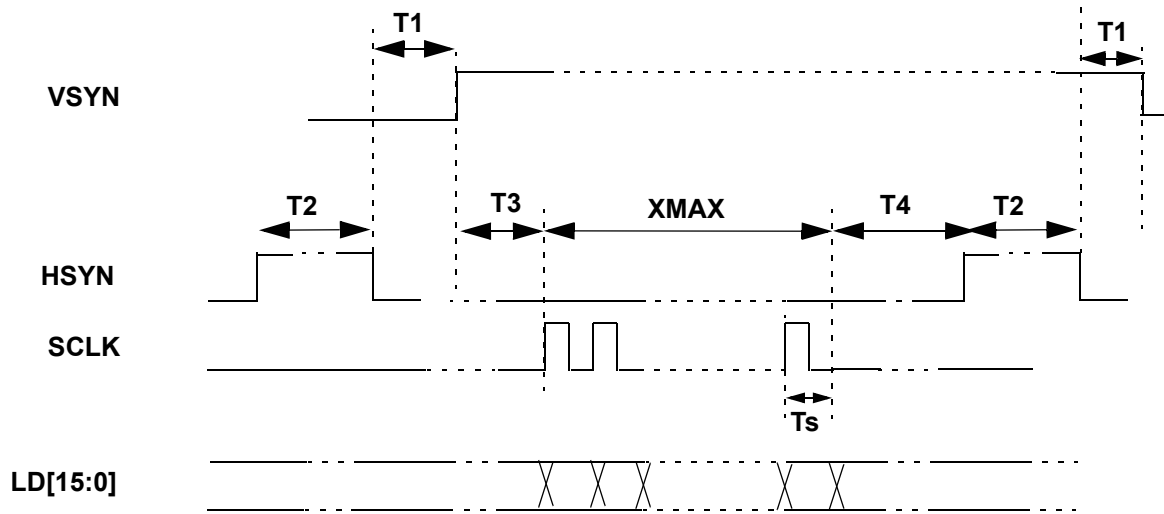


Figure 33. Non-TFT Panel Timing

Table 17. Non TFT Panel Timing Diagram

| Symbol | Parameter                       | Allowed Register Minimum Value <sup>1, 2</sup> | Actual Value          | Unit              |
|--------|---------------------------------|--|-----------------------|-------------------|
| T1     | HSYN to VSYN delay <sup>3</sup> | 0  | HWAIT2+2              | Tpix <sup>4</sup> |
| T2     | HSYN pulse width                | 0  | HWIDTH+1              | Tpix              |
| T3     | VSYN to SCLK                    | –  | $0 \leq T3 \leq Ts^5$ | –                 |
| T4     | SCLK to HSYN                    | 0  | HWAIT1+1              | Tpix              |

<sup>1</sup> Maximum frequency of LCDC\_CLK is 48 MHz, which is controlled by Peripheral Clock Divider Register.

<sup>2</sup> Maximum frequency of SCLK is HCLK / 5, otherwise LD output will be wrong.

<sup>3</sup> VSYN, HSYN and SCLK can be programmed as active high or active low. In the above timing diagram, all these 3 signals are active high.

<sup>4</sup> Tpix is the pixel clock period which equals LCDC\_CLK period \* (PCD + 1).

<sup>5</sup> Ts is the shift clock period. Ts = Tpix \* (panel data bus width).

#### 4.5 SPI Timing Diagrams

To use the internal transmit (TX) and receive (RX) data FIFOs when the SPI module is configured as a master, two control signals are used for data transfer rate control: the  $\overline{SS}$  signal (output) and the  $\overline{SPI\_RDY}$  signal (input). The SPI1 Sample Period Control Register (PERIODREG1) can also be programmed to a fixed data transfer rate. When the SPI module is configured as a slave, the user can configure the SPI1 Control Register (CONTROLREG1) to match the external SPI master's timing. In this configuration,  $\overline{SS}$  becomes an input signal, and is used to latch data into or load data out to the internal data shift registers, as well as to increment the data FIFO. Figure 34 through Figure 38 show the timing relationship of the master SPI using different triggering mechanisms.

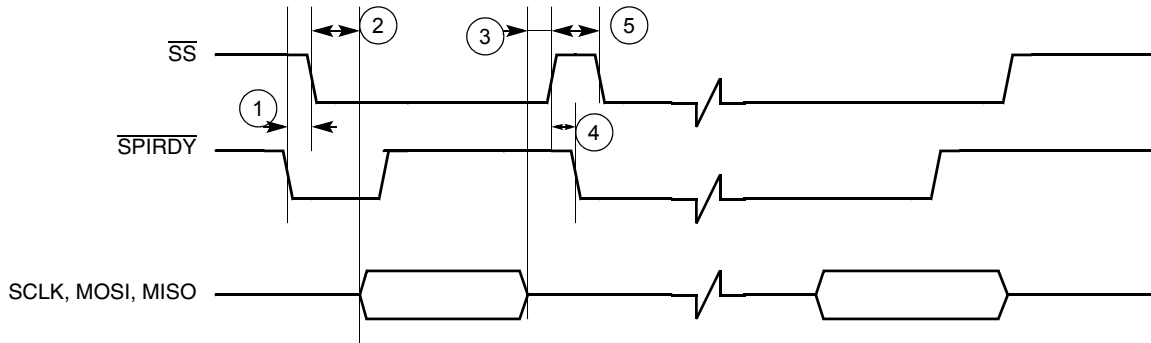


Figure 34. Master SPI Timing Diagram Using  $\overline{\text{SPI\_RDY}}$  Edge Trigger

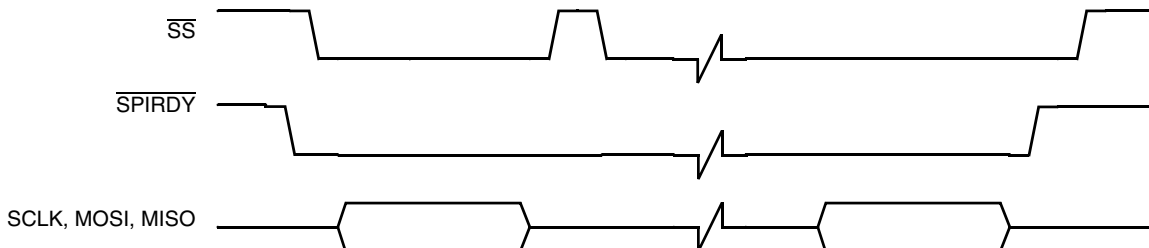


Figure 35. Master SPI Timing Diagram Using  $\overline{\text{SPI\_RDY}}$  Level Trigger

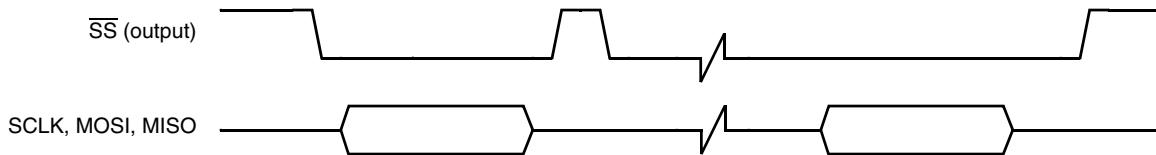


Figure 36. Master SPI Timing Diagram Ignore  $\overline{\text{SPI\_RDY}}$  Level Trigger

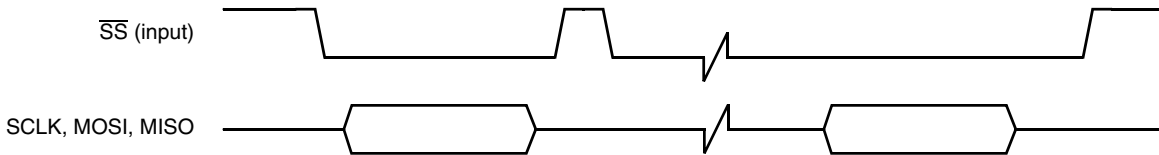


Figure 37. Slave SPI Timing Diagram FIFO Advanced by BIT COUNT

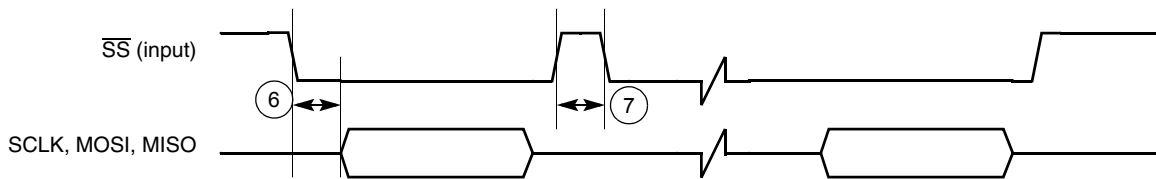


Figure 38. Slave SPI Timing Diagram FIFO Advanced by  $\overline{\text{SS}}$  Rising Edge

Table 18. Timing Parameter Table for Figure 34 through Figure 38

| Ref No. | Parameter  | 3.0 ± 0.3 V                       |         | Unit |
|---------|--|-----------------------------------|---------|------|
|         |  | Minimum                           | Maximum |      |
| 1       | $\overline{\text{SPI\_RDY}}$ to $\overline{\text{SS}}$ output low      | $2T^1$                            | –       | ns   |
| 2       | $\overline{\text{SS}}$ output low to first SCLK edge                   | $3 \cdot T_{\text{sclk}}^2$       | –       | ns   |
| 3       | Last SCLK edge to $\overline{\text{SS}}$ output high                   | $2 \cdot T_{\text{sclk}}$         | –       | ns   |
| 4       | $\overline{\text{SS}}$ output high to $\overline{\text{SPI\_RDY}}$ low | 0                                 | –       | ns   |
| 5       | $\overline{\text{SS}}$ output pulse width                              | $T_{\text{sclk}} + \text{WAIT}^3$ | –       | ns   |
| 6       | $\overline{\text{SS}}$ input low to first SCLK edge                    | T                                 | –       | ns   |
| 7       | $\overline{\text{SS}}$ input pulse width                               | T                                 | –       | ns   |

<sup>1</sup> T = CSPI system clock period (PERCLK2).

<sup>2</sup>  $T_{\text{sclk}}$  = Period of SCLK.

<sup>3</sup> WAIT = Number of bit clocks (SCLK) or 32.768 kHz clocks per Sample Period Control Register.

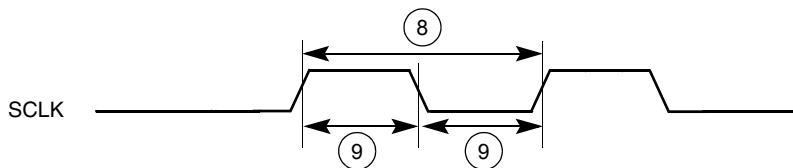


Figure 39. SPI SCLK Timing Diagram

Table 19. Timing Parameter Table for SPI SCLK

| Ref No. | Parameter        | 3.0 ± 0.3 V |         | Unit |
|---------|------------------|-------------|---------|------|
|         |                  | Minimum     | Maximum |      |
| 8       | SCLK frequency   | 0           | 10      | MHz  |
| 9       | SCLK pulse width | 100         | –       | ns   |

## 4.6 LCD Controller

This section includes timing diagrams for the LCD controller. For detailed timing diagrams of the LCD controller with various display configurations, refer to the LCD controller chapter of the *MC9328MXS Reference Manual*.

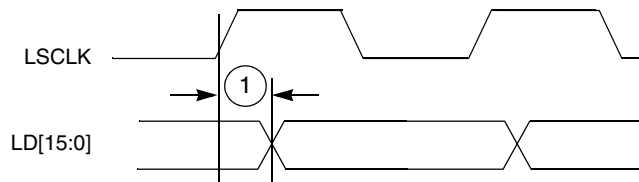
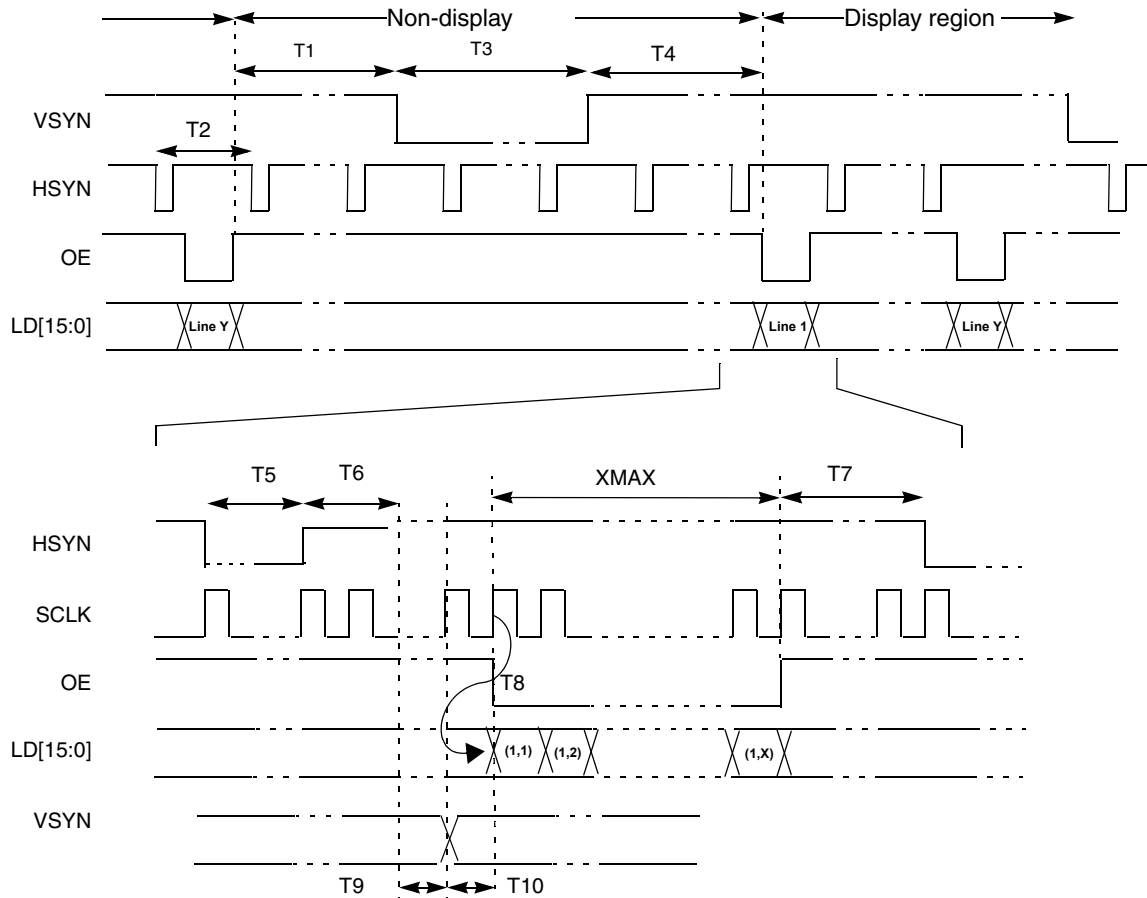


Figure 40. SCLK to LD Timing Diagram

**Table 20. LCDC SCLK Timing Parameter Table**

| Ref No. | Parameter        | 3.0 ± 0.3 V |         | Unit |
|---------|------------------|-------------|---------|------|
|         |                  | Minimum     | Maximum |      |
| 1       | SCLK to LD valid | –           | 2       | ns   |



**Figure 41. 4/8/16 Bit/Pixel TFT Color Mode Panel Timing**

**Table 21. 4/8/16 Bit/Pixel TFT Color Mode Panel Timing**

| Symbol | Description                    | Minimum       | Corresponding Register Value | Unit |
|--------|--------------------------------|---------------|------------------------------|------|
| T1     | End of OE to beginning of VSYN | $T5+T6+T7+T9$ | $(VWAIT1-T2)+T5+T6+T7+T9$    | Ts   |
| T2     | HSYN period                    | $XMAX+5$      | $XMAX+T5+T6+T7+T9+T10$       | Ts   |
| T3     | VSYN pulse width               | T2            | $VWIDTH \cdot (T2)$          | Ts   |
| T4     | End of VSYN to beginning of OE | 2             | $VWAIT2 \cdot (T2)$          | Ts   |
| T5     | HSYN pulse width               | 1             | $HWIDTH+1$                   | Ts   |
| T6     | End of HSYN to beginning to T9 | 1             | $HWAIT2+1$                   | Ts   |
| T7     | End of OE to beginning of HSYN | 1             | $HWAIT1+1$                   | Ts   |



Table 21. 4/8/16 Bit/Pixel TFT Color Mode Panel Timing (Continued)

| Symbol | Description  | Minimum | Corresponding Register Value | Unit |
|--------|--|---------|------------------------------|------|
| T8     | SCLK to valid LD data                                      | -3      | 3                            | ns   |
| T9     | End of HSYN idle2 to VSYN edge<br>(for non-display region) | 2       | 2                            | Ts   |
| T9     | End of HSYN idle2 to VSYN edge<br>(for Display region)     | 1       | 1                            | Ts   |
| T10    | VSYN to OE active (Sharp = 0) when VWAIT2 = 0              | 1       | 1                            | Ts   |
| T10    | VSYN to OE active (Sharp = 1) when VWAIT2 = 0              | 2       | 2                            | Ts   |

**Note:**

- Ts is the SCLK period which equals  $LCDC\_CLK / (PCD + 1)$ . Normally  $LCDC\_CLK = 15ns$ .
- VSYN, HSYN and OE can be programmed as active high or active low. In Figure 41, all 3 signals are active low.
- The polarity of SCLK and LD[15:0] can also be programmed.
- SCLK can be programmed to be deactivated during the VSYN pulse or the OE deasserted period. In Figure 41, SCLK is always active.
- For T9 non-display region, VSYN is non-active. It is used as an reference.
- XMAX is defined in pixels.

## 4.7 Pulse-Width Modulator

The PWM can be programmed to select one of two clock signals as its source frequency. The selected clock signal is passed through a divider and a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin. Its timing diagram is shown in Figure 42 and the parameters are listed in Table 22.

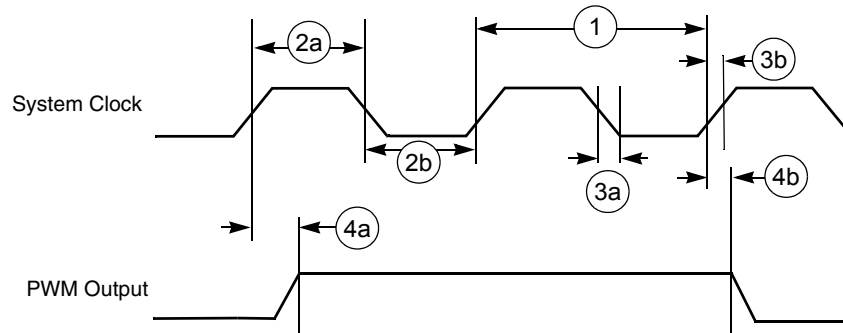


Figure 42. PWM Output Timing Diagram

Table 22. PWM Output Timing Parameter Table

| Ref No. | Parameter                         | 1.8 ± 0.1 V |         | 3.0 ± 0.3 V |         | Unit |
|---------|-----------------------------------|-------------|---------|-------------|---------|------|
|         |                                   | Minimum     | Maximum | Minimum     | Maximum |      |
| 1       | System CLK frequency <sup>1</sup> | 0           | 87      | 0           | 100     | MHz  |
| 2a      | Clock high time <sup>1</sup>      | 3.3         | –       | 5/10        | –       | ns   |
| 2b      | Clock low time <sup>1</sup>       | 7.5         | –       | 5/10        | –       | ns   |
| 3a      | Clock fall time <sup>1</sup>      | –           | 5       | –           | 5/10    | ns   |
| 3b      | Clock rise time <sup>1</sup>      | –           | 6.67    | –           | 5/10    | ns   |
| 4a      | Output delay time <sup>1</sup>    | 5.7         | –       | 5           | –       | ns   |
| 4b      | Output setup time <sup>1</sup>    | 5.7         | –       | 5           | –       | ns   |

<sup>1</sup> C<sub>L</sub> of PWMO = 30 pF

## 4.8 SDRAM Controller

This section shows timing diagrams and parameters associated with the SDRAM (synchronous dynamic random access memory) Controller.

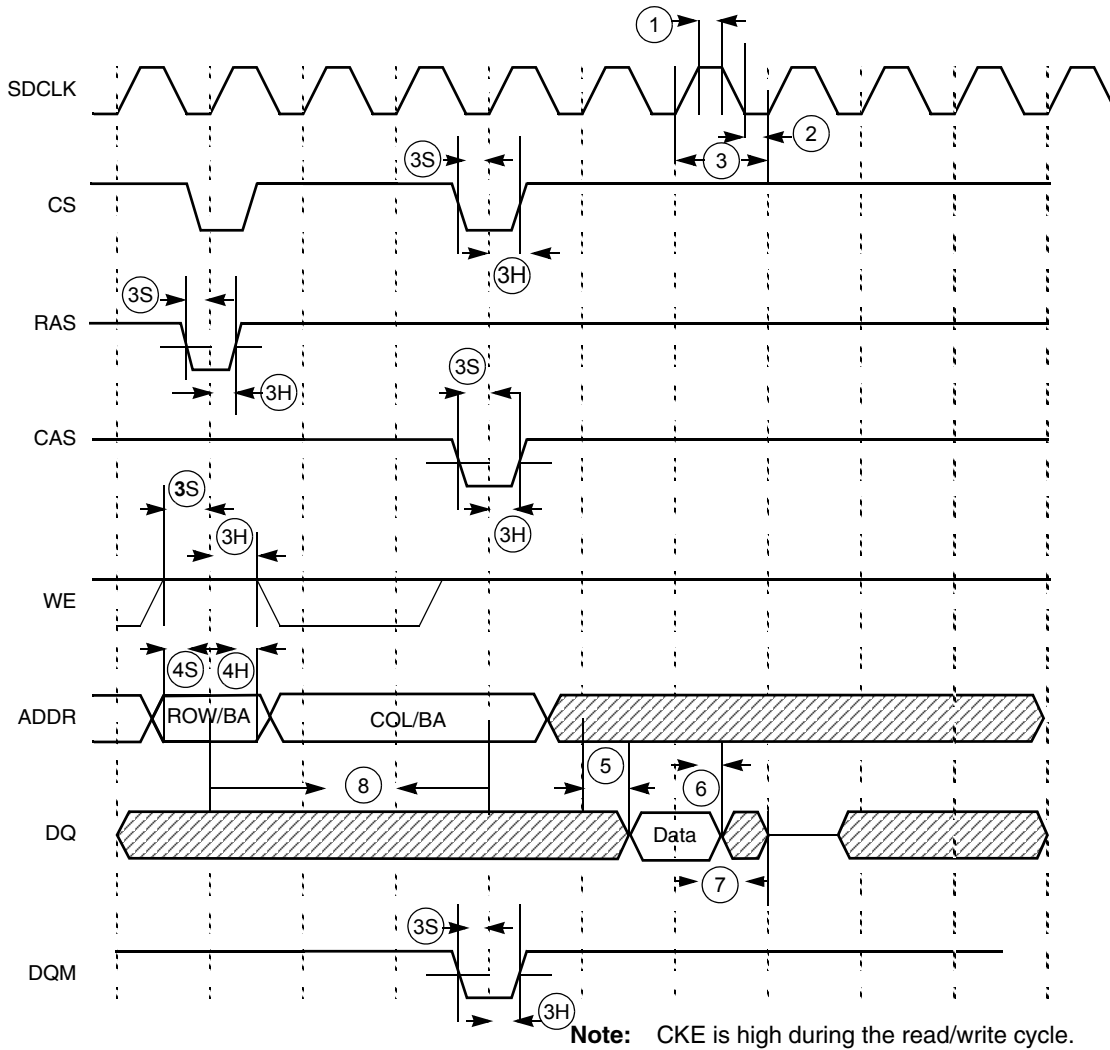


Figure 43. SDRAM Read Cycle Timing Diagram

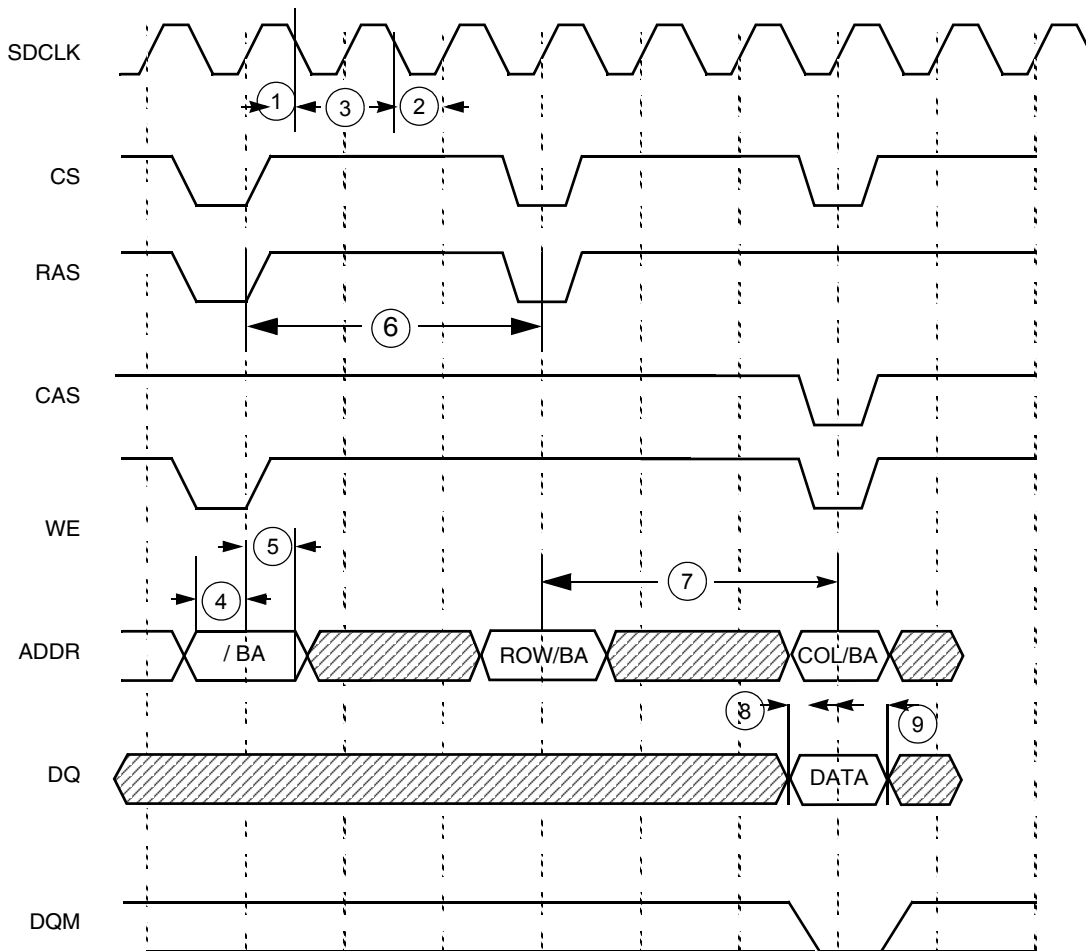
Table 23. SDRAM Read Timing Parameter Table

| Ref No. | Parameter                        | 1.8 ± 0.1 V |         | 3.0 ± 0.3 V |         | Unit |
|---------|----------------------------------|-------------|---------|-------------|---------|------|
|         |                                  | Minimum     | Maximum | Minimum     | Maximum |      |
| 1       | SDRAM clock high-level width     | 2.67        | –       | 4           | –       | ns   |
| 2       | SDRAM clock low-level width      | 6           | –       | 4           | –       | ns   |
| 3       | SDRAM clock cycle time           | 11.4        | –       | 10          | –       | ns   |
| 3S      | CS, RAS, CAS, WE, DQM setup time | 3.42        | –       | 3           | –       | ns   |
| 3H      | CS, RAS, CAS, WE, DQM hold time  | 2.28        | –       | 2           | –       | ns   |
| 4S      | Address setup time               | 3.42        | –       | 3           | –       | ns   |
| 4H      | Address hold time                | 2.28        | –       | 2           | –       | ns   |
| 5       | SDRAM access time (CL = 3)       | –           | 6.84    | –           | 6       | ns   |

**Table 23. SDRAM Read Timing Parameter Table (Continued)**

| Ref No. | Parameter                                    | 1.8 ± 0.1 V |         | 3.0 ± 0.3 V |         | Unit |
|---------|--|-------------|---------|-------------|---------|------|
|         |  | Minimum     | Maximum | Minimum     | Maximum |      |
| 5       | SDRAM access time (CL = 2)                   | –           | 6.84    | –           | 6       | ns   |
| 5       | SDRAM access time (CL = 1)                   | –           | 22      | –           | 22      | ns   |
| 6       | Data out hold time                           | 2.85        | –       | 2.5         | –       | ns   |
| 7       | Data out high-impedance time (CL = 3)        | –           | 6.84    | –           | 6       | ns   |
| 7       | Data out high-impedance time (CL = 2)        | –           | 6.84    | –           | 6       | ns   |
| 7       | Data out high-impedance time (CL = 1)        | –           | 22      | –           | 22      | ns   |
| 8       | Active to read/write command period (RC = 1) | $t_{RCD}^1$ | –       | $t_{RCD1}$  | –       | ns   |

<sup>1</sup>  $t_{RCD}$  = SDRAM clock cycle time. This settings can be found in the *MC9328MXS reference manual*.



**Figure 44. SDRAM Write Cycle Timing Diagram**

Table 24. SDRAM Write Timing Parameter Table

| Ref No. | Parameter                           | 1.8 ± 0.1 V           |         | 3.0 ± 0.3 V |         | Unit |
|---------|-------------------------------------|-----------------------|---------|-------------|---------|------|
|         |                                     | Minimum               | Maximum | Minimum     | Maximum |      |
| 1       | SDRAM clock high-level width        | 2.67                  | –       | 4           | –       | ns   |
| 2       | SDRAM clock low-level width         | 6                     | –       | 4           | –       | ns   |
| 3       | SDRAM clock cycle time              | 11.4                  | –       | 10          | –       | ns   |
| 4       | Address setup time                  | 3.42                  | –       | 3           | –       | ns   |
| 5       | Address hold time                   | 2.28                  | –       | 2           | –       | ns   |
| 6       | Precharge cycle period <sup>1</sup> | $t_{RP}$ <sup>2</sup> | –       | $t_{RP2}$   | –       | ns   |
| 7       | Active to read/write command delay  | $t_{RCD2}$            | –       | $t_{RCD2}$  | –       | ns   |
| 8       | Data setup time                     | 4.0                   | –       | 2           | –       | ns   |
| 9       | Data hold time                      | 2.28                  | –       | 2           | –       | ns   |

<sup>1</sup> Precharge cycle timing is included in the write timing diagram.

<sup>2</sup>  $t_{RP}$  and  $t_{RCD}$  = SDRAM clock cycle time. These settings can be found in the *MC9328MXS reference manual*.

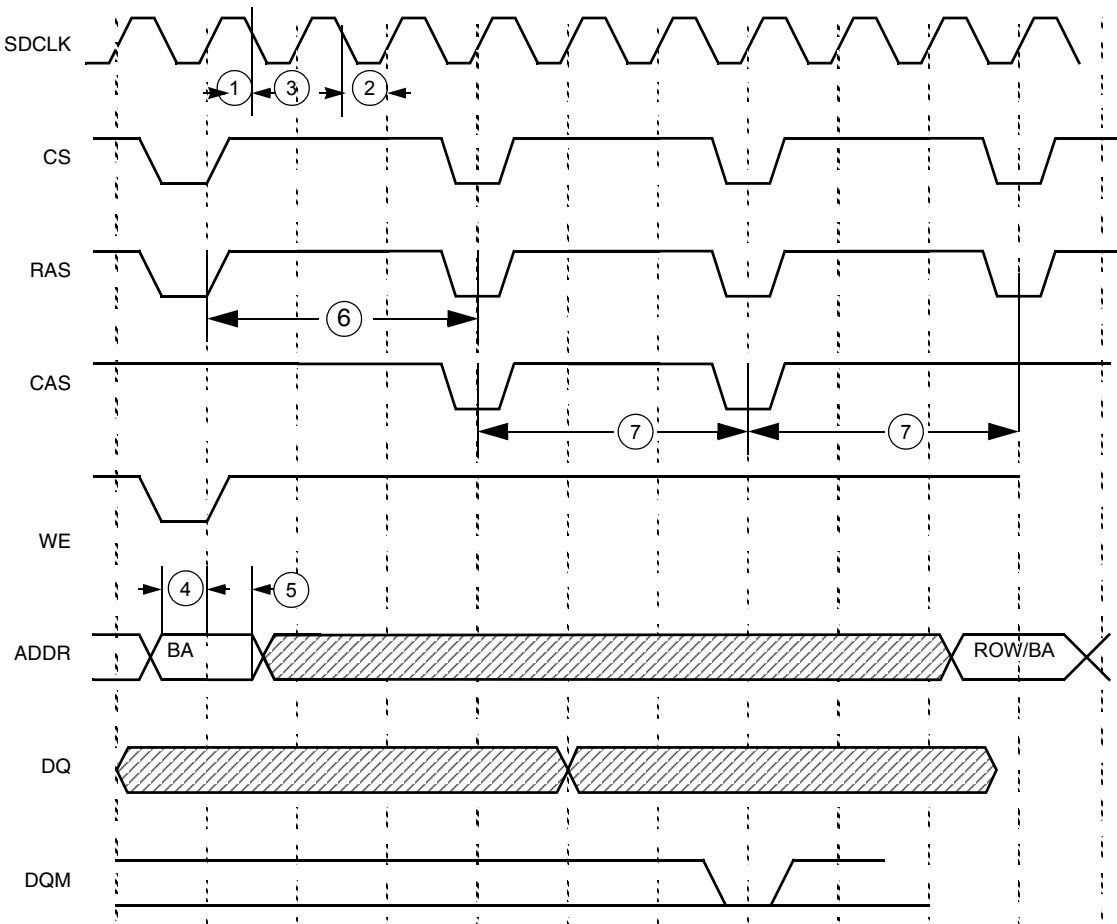
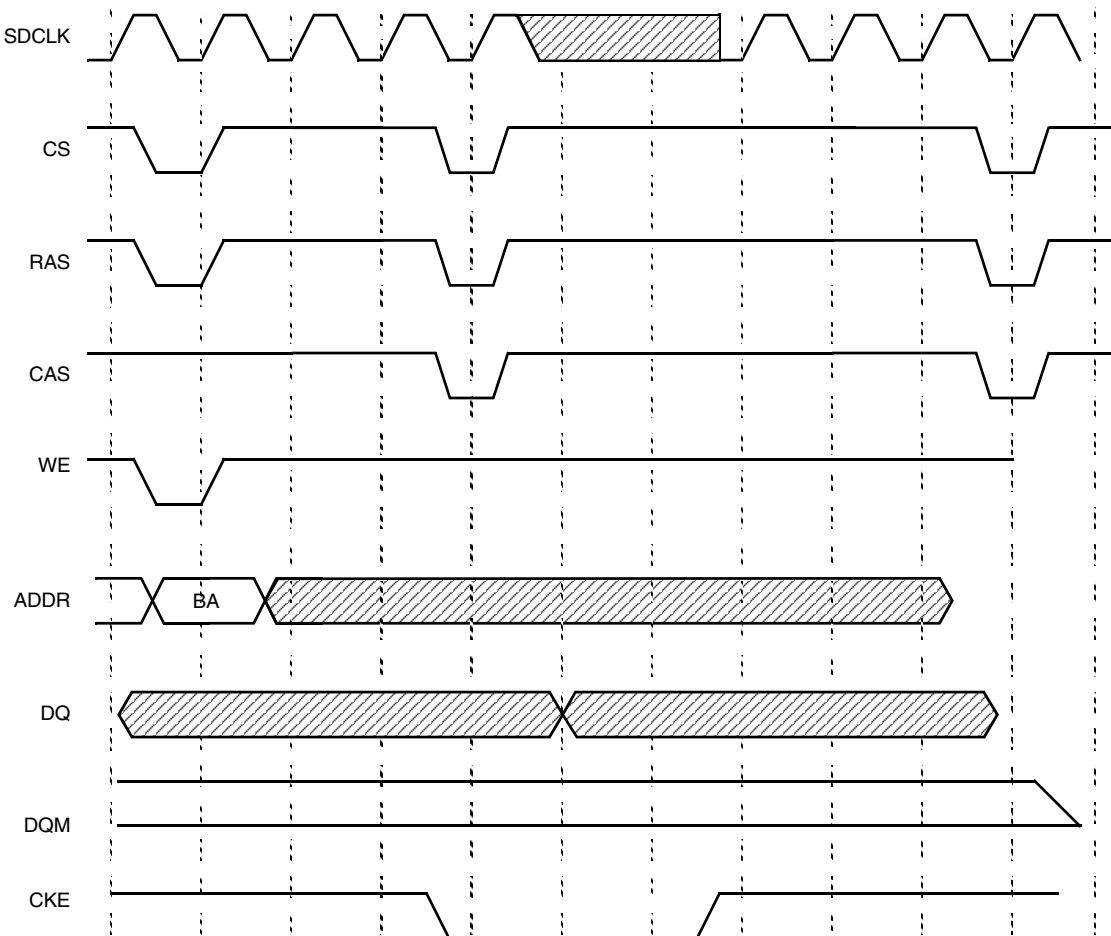


Figure 45. SDRAM Refresh Timing Diagram

**Table 25. SDRAM Refresh Timing Parameter Table**

| Ref No. | Parameter                     | 1.8 ± 0.1 V |         | 3.0 ± 0.3 V |         | Unit |
|---------|-------------------------------|-------------|---------|-------------|---------|------|
|         |                               | Minimum     | Maximum | Minimum     | Maximum |      |
| 1       | SDRAM clock high-level width  | 2.67        | –       | 4           | –       | ns   |
| 2       | SDRAM clock low-level width   | 6           | –       | 4           | –       | ns   |
| 3       | SDRAM clock cycle time        | 11.4        | –       | 10          | –       | ns   |
| 4       | Address setup time            | 3.42        | –       | 3           | –       | ns   |
| 5       | Address hold time             | 2.28        | –       | 2           | –       | ns   |
| 6       | Precharge cycle period        | $t_{RP}^1$  | –       | $t_{RP1}$   | –       | ns   |
| 7       | Auto precharge command period | $t_{RC1}$   | –       | $t_{RC1}$   | –       | ns   |

<sup>1</sup>  $t_{RP}$  and  $t_{RC}$  = SDRAM clock cycle time. These settings can be found in the *MC9328MXS reference manual*.



**Figure 46. SDRAM Self-Refresh Cycle Timing Diagram**

## 4.9 USB Device Port

Four types of data transfer modes exist for the USB module: control transfers, bulk transfers, isochronous transfers, and interrupt transfers. From the perspective of the USB module, the interrupt transfer type is identical to the bulk data transfer mode, and no additional hardware is supplied to support it. This section covers the transfer modes and how they work from the ground up.

Data moves across the USB in packets. Groups of packets are combined to form data transfers. The same packet transfer mechanism applies to bulk, interrupt, and control transfers. Isochronous data is also moved in the form of packets, however, because isochronous pipes are given a fixed portion of the USB bandwidth at all times, there is no end-of-transfer.

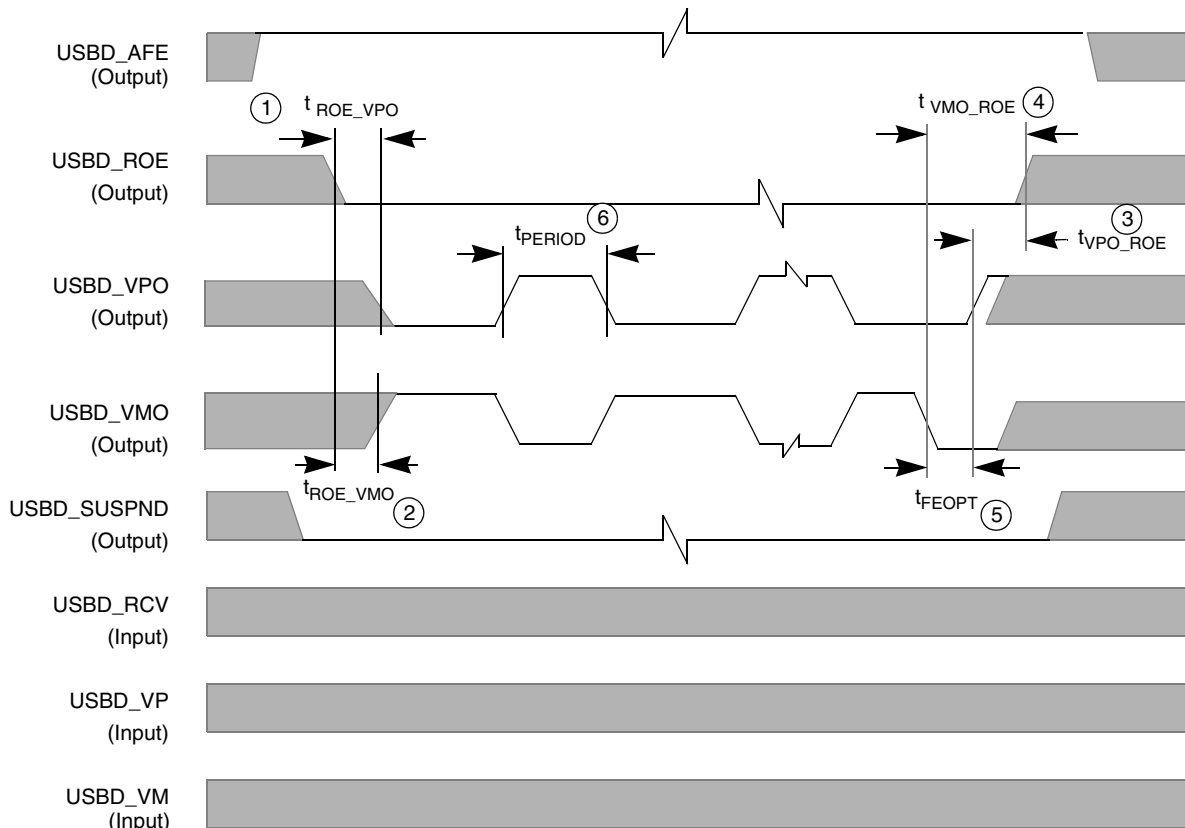


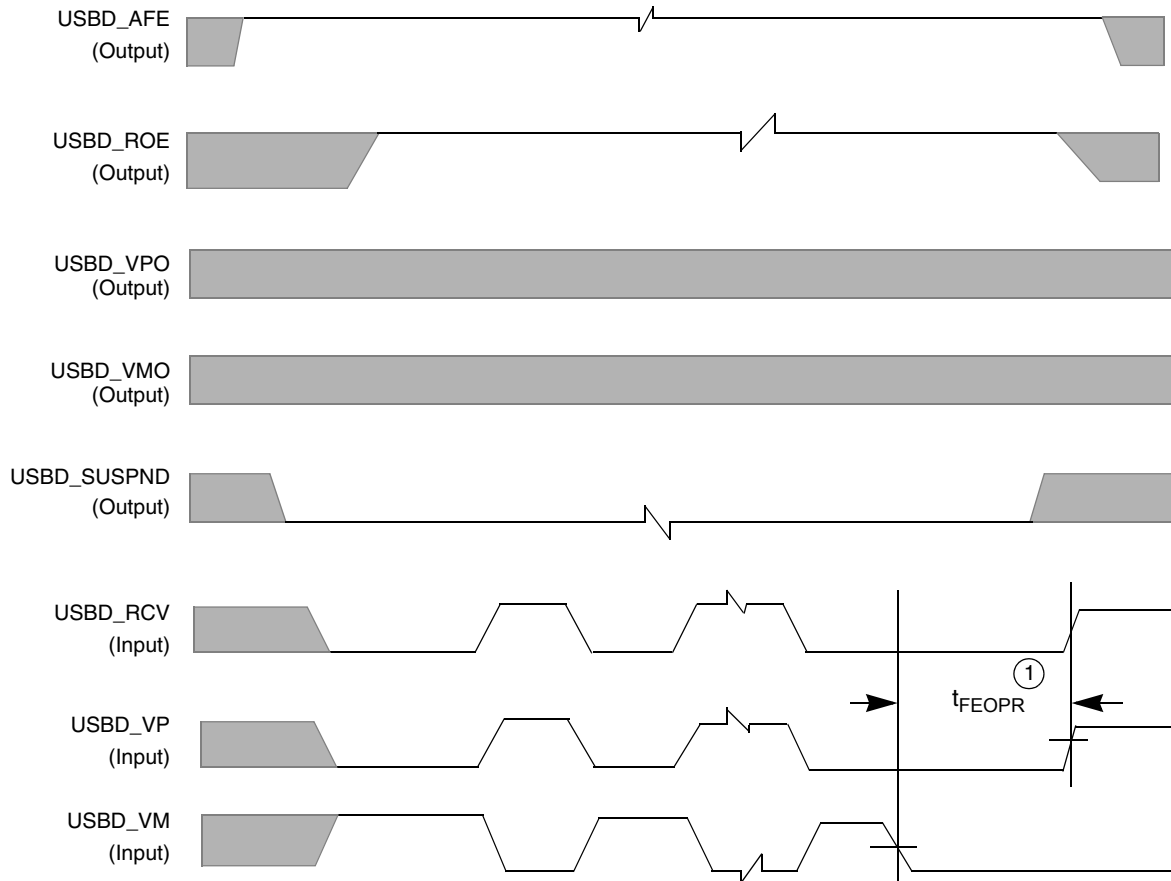
Figure 47. USB Device Timing Diagram for Data Transfer to USB Transceiver (TX)

Table 26. USB Device Timing Parameters for Data Transfer to USB Transceiver (TX)

| Ref No. | Parameter  | 3.0 ± 0.3 V |         | Unit |
|---------|--|-------------|---------|------|
|         |  | Minimum     | Maximum |      |
| 1       | $t_{ROE\_VPO}$ : USBD_ROE active to USBD_VPO low                     | 83.14       | 83.47   | ns   |
| 2       | $t_{ROE\_VMO}$ : USBD_ROE active to USBD_VMO high                    | 81.55       | 81.98   | ns   |
| 3       | $t_{VPO\_ROE}$ : USBD_VPO high to USBD_ROE deactivated               | 83.54       | 83.80   | ns   |
| 4       | $t_{VMO\_ROE}$ : USBD_VMO low to USBD_ROE deactivated (includes SE0) | 248.90      | 249.13  | ns   |

**Table 26. USB Device Timing Parameters for Data Transfer to USB Transceiver (TX) (Continued)**

| Ref No. | Parameter                         | 3.0 ± 0.3 V |         | Unit |
|---------|-----------------------------------|-------------|---------|------|
|         |                                   | Minimum     | Maximum |      |
| 5       | $t_{FEOPT}$ ; SE0 interval of EOP | 160.00      | 175.00  | ns   |
| 6       | $t_{PERIOD}$ ; Data transfer rate | 11.97       | 12.03   | Mb/s |



**Figure 48. USB Device Timing Diagram for Data Transfer from USB Transceiver (RX)**

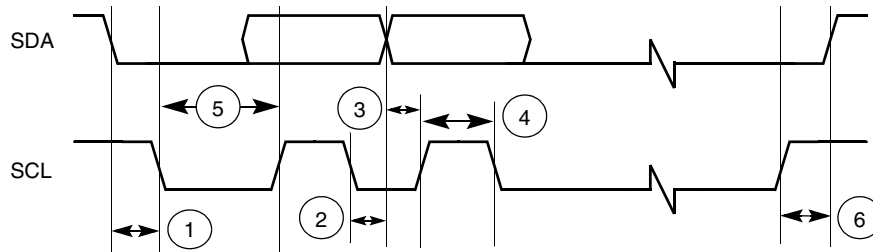
**Table 27. USB Device Timing Parameter Table for Data Transfer from USB Transceiver (RX)**

| Ref No. | Parameter                                  | 3.0 ± 0.3 V |         | Unit |
|---------|--|-------------|---------|------|
|         |  | Minimum     | Maximum |      |
| 1       | $t_{FEOPR}$ ; Receiver SE0 interval of EOP | 82          | –       | ns   |

## 4.10 I<sup>2</sup>C Module

The I<sup>2</sup>C communication protocol consists of seven elements: START, Data Source/Recipient, Data Direction, Slave Acknowledge, Data, Data Acknowledge, and STOP.



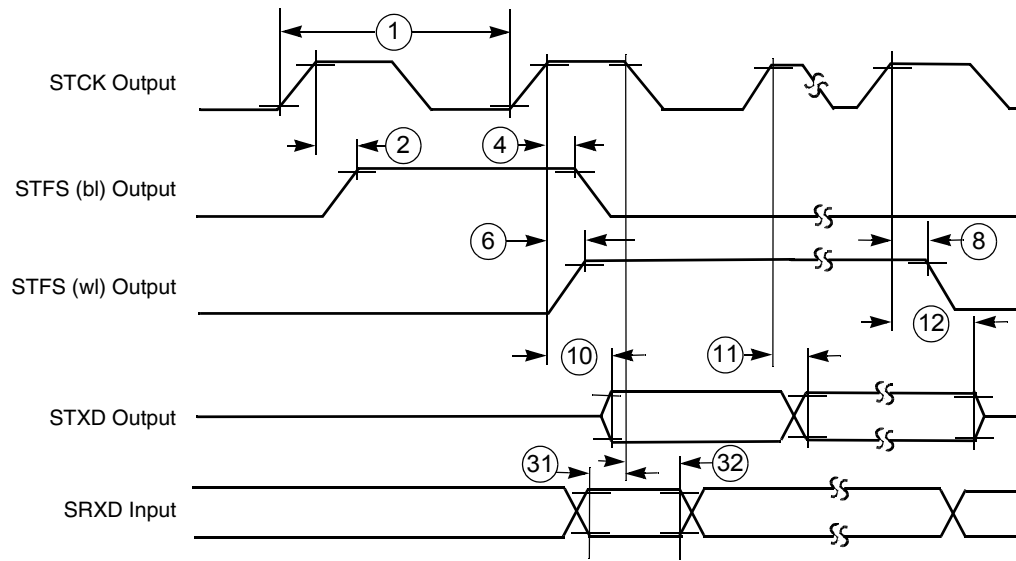
Figure 49. Definition of Bus Timing for I<sup>2</sup>CTable 28. I<sup>2</sup>C Bus Timing Parameter Table

| Ref No. | Parameter                            | 1.8 ± 0.1 V |         | 3.0 ± 0.3 V |         | Unit |
|---------|--------------------------------------|-------------|---------|-------------|---------|------|
|         |                                      | Minimum     | Maximum | Minimum     | Maximum |      |
| 1       | Hold time (repeated) START condition | 182         | –       | 160         | –       | ns   |
| 2       | Data hold time                       | 0           | 171     | 0           | 150     | ns   |
| 3       | Data setup time                      | 11.4        | –       | 10          | –       | ns   |
| 4       | HIGH period of the SCL clock         | 80          | –       | 120         | –       | ns   |
| 5       | LOW period of the SCL clock          | 480         | –       | 320         | –       | ns   |
| 6       | Setup time for STOP condition        | 182.4       | –       | 160         | –       | ns   |

## 4.11 Synchronous Serial Interface

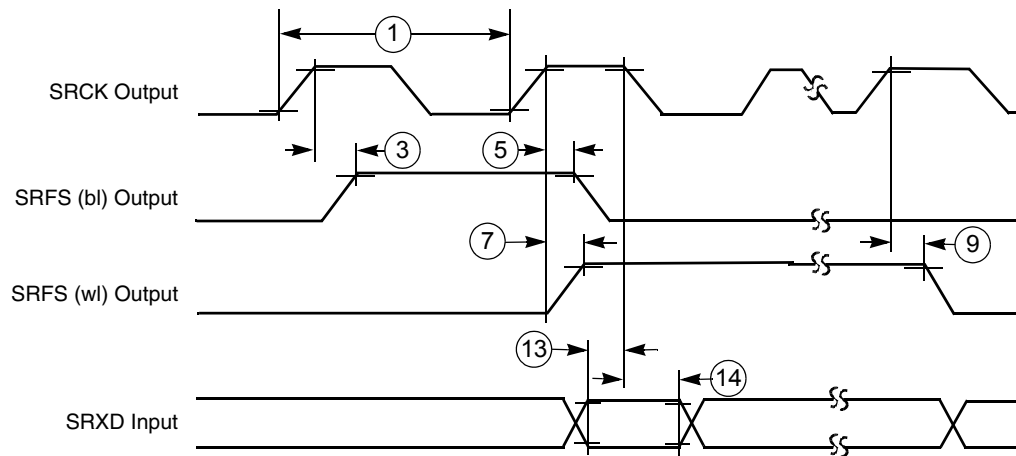
The transmit and receive sections of the SSI can be synchronous or asynchronous. In synchronous mode, the transmitter and the receiver use a common clock and frame synchronization signal. In asynchronous mode, the transmitter and receiver each have their own clock and frame synchronization signals. Continuous or gated clock mode can be selected. In continuous mode, the clock runs continuously. In gated clock mode, the clock functions only during transmission. The internal and external clock timing diagrams are shown in Figure 51 through Figure 53.

Normal or network mode can also be selected. In normal mode, the SSI functions with one data word of I/O per frame. In network mode, a frame can contain between 2 and 32 data words. Network mode is typically used in star or ring-time division multiplex networks with other processors or codecs, allowing interface to time division multiplexed networks without additional logic. Use of the gated clock is not allowed in network mode. These distinctions result in the basic operating modes that allow the SSI to communicate with a wide variety of devices.



**Note:** SRXD input in synchronous mode only.

**Figure 50. SSI Transmitter Internal Clock Timing Diagram**



**Figure 51. SSI Receiver Internal Clock Timing Diagram**

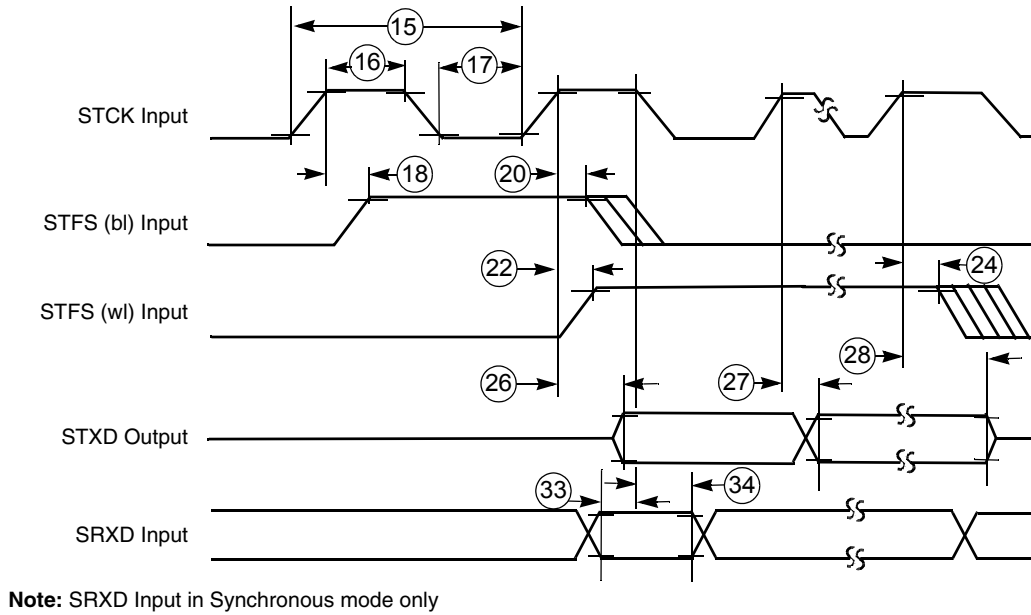


Figure 52. SSI Transmitter External Clock Timing Diagram

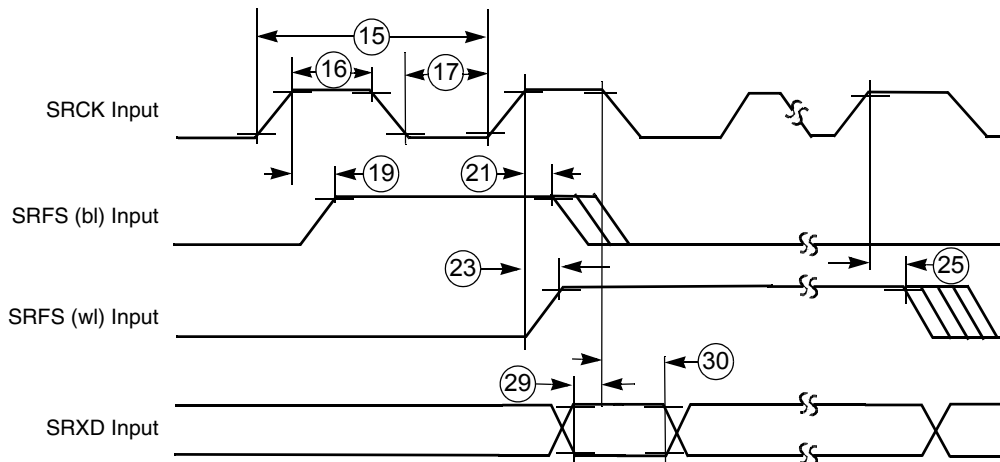


Figure 53. SSI Receiver External Clock Timing Diagram

Table 29. SSI (Port C Primary Function) Timing Parameter Table

| Ref No.   | Parameter                                | 1.8 ± 0.1 V |         | 3.0 ± 0.3 V |         | Unit |
|---|--|-------------|---------|-------------|---------|------|
|   |  | Minimum     | Maximum | Minimum     | Maximum |      |
| <b>Internal Clock Operation<sup>1</sup> (Port C Primary Function<sup>2</sup>)</b> |  |             |         |             |         |      |
| 1   | STCK/SRCK clock period <sup>1</sup>      | 95          | –       | 83.3        | –       | ns   |
| 2   | STCK high to STFS (bl) high <sup>3</sup> | 1.5         | 4.5     | 1.3         | 3.9     | ns   |
| 3   | SRCK high to SRFS (bl) high <sup>3</sup> | -1.2        | -1.7    | -1.1        | -1.5    | ns   |
| 4   | STCK high to STFS (bl) low <sup>3</sup>  | 2.5         | 4.3     | 2.2         | 3.8     | ns   |
| 5   | SRCK high to SRFS (bl) low <sup>3</sup>  | 0.1         | -0.8    | 0.1         | -0.8    | ns   |

Table 29. SSI (Port C Primary Function) Timing Parameter Table (Continued)

| Ref No.   | Parameter                                   | 1.8 ± 0.1 V |         | 3.0 ± 0.3 V |         | Unit |
|---|---|-------------|---------|-------------|---------|------|
|   |   | Minimum     | Maximum | Minimum     | Maximum |      |
| 6   | STCK high to STFS (wl) high <sup>3</sup>    | 1.48        | 4.45    | 1.3         | 3.9     | ns   |
| 7   | SRCK high to SRFS (wl) high <sup>3</sup>    | -1.1        | -1.5    | -1.1        | -1.5    | ns   |
| 8   | STCK high to STFS (wl) low <sup>3</sup>     | 2.51        | 4.33    | 2.2         | 3.8     | ns   |
| 9   | SRCK high to SRFS (wl) low <sup>3</sup>     | 0.1         | -0.8    | 0.1         | -0.8    | ns   |
| 10  | STCK high to STXD valid from high impedance | 14.25       | 15.73   | 12.5        | 13.8    | ns   |
| 11a   | STCK high to STXD high                      | 0.91        | 3.08    | 0.8         | 2.7     | ns   |
| 11b   | STCK high to STXD low                       | 0.57        | 3.19    | 0.5         | 2.8     | ns   |
| 12  | STCK high to STXD high impedance            | 12.88       | 13.57   | 11.3        | 11.9    | ns   |
| 13  | SRXD setup time before SRCK low             | 21.1        | –       | 18.5        | –       | ns   |
| 14  | SRXD hold time after SRCK low               | 0           | –       | 0           | –       | ns   |
| <b>External Clock Operation (Port C Primary Function<sup>2</sup>)</b>             |   |             |         |             |         |      |
| 15  | STCK/SRCK clock period <sup>1</sup>         | 92.8        | –       | 81.4        | –       | ns   |
| 16  | STCK/SRCK clock high period                 | 27.1        | –       | 40.7        | –       | ns   |
| 17  | STCK/SRCK clock low period                  | 61.1        | –       | 40.7        | –       | ns   |
| 18  | STCK high to STFS (bl) high <sup>3</sup>    | –           | 92.8    | 0           | 81.4    | ns   |
| 19  | SRCK high to SRFS (bl) high <sup>3</sup>    | –           | 92.8    | 0           | 81.4    | ns   |
| 20  | STCK high to STFS (bl) low <sup>3</sup>     | –           | 92.8    | 0           | 81.4    | ns   |
| 21  | SRCK high to SRFS (bl) low <sup>3</sup>     | –           | 92.8    | 0           | 81.4    | ns   |
| 22  | STCK high to STFS (wl) high <sup>3</sup>    | –           | 92.8    | 0           | 81.4    | ns   |
| 23  | SRCK high to SRFS (wl) high <sup>3</sup>    | –           | 92.8    | 0           | 81.4    | ns   |
| 24  | STCK high to STFS (wl) low <sup>3</sup>     | –           | 92.8    | 0           | 81.4    | ns   |
| 25  | SRCK high to SRFS (wl) low <sup>3</sup>     | –           | 92.8    | 0           | 81.4    | ns   |
| 26  | STCK high to STXD valid from high impedance | 18.01       | 28.16   | 15.8        | 24.7    | ns   |
| 27a   | STCK high to STXD high                      | 8.98        | 18.13   | 7.0         | 15.9    | ns   |
| 27b   | STCK high to STXD low                       | 9.12        | 18.24   | 8.0         | 16.0    | ns   |
| 28  | STCK high to STXD high impedance            | 18.47       | 28.5    | 16.2        | 25.0    | ns   |
| 29  | SRXD setup time before SRCK low             | 1.14        | –       | 1.0         | –       | ns   |
| 30  | SRXD hold time after SRCK low               | 0           | –       | 0           | –       | ns   |
| <b>Synchronous Internal Clock Operation (Port C Primary Function<sup>2</sup>)</b> |   |             |         |             |         |      |
| 31  | SRXD setup before STCK falling              | 15.4        | –       | 13.5        | –       | ns   |
| 32  | SRXD hold after STCK falling                | 0           | –       | 0           | –       | ns   |

**Table 29. SSI (Port C Primary Function) Timing Parameter Table (Continued)**

| Ref No.   | Parameter                      | 1.8 ± 0.1 V |         | 3.0 ± 0.3 V |         | Unit |
|---|--------------------------------|-------------|---------|-------------|---------|------|
|   |                                | Minimum     | Maximum | Minimum     | Maximum |      |
| <b>Synchronous External Clock Operation (Port C Primary Function<sup>2</sup>)</b> |                                |             |         |             |         |      |
| 33  | SRXD setup before STCK falling | 1.14        | –       | 1.0         | –       | ns   |
| 34  | SRXD hold after STCK falling   | 0           | –       | 0           | –       | ns   |

<sup>1</sup> All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

<sup>2</sup> There are 2 sets of I/O signals for the SSI module. They are from Port C primary function (pad 257 to pad 261) and Port B alternate function (pad 283 to pad 288). When SSI signals are configured as outputs, they can be viewed both at Port C primary function and Port B alternate function. When SSI signals are configured as input, the SSI module selects the input based on status of the FMCR register bits in the Clock controller module (CRM). By default, the input are selected from Port C primary function.

<sup>3</sup> bl = bit length; wl = word length.

**Table 30. SSI (Port B Alternate Function) Timing Parameter Table**

| Ref No.   | Parameter                                   | 1.8 ± 0.1 V |         | 3.0 ± 0.3 V |         | Unit |
|---|---|-------------|---------|-------------|---------|------|
|   |   | Minimum     | Maximum | Minimum     | Maximum |      |
| <b>Internal Clock Operation<sup>1</sup> (Port B Alternate Function<sup>2</sup>)</b> |   |             |         |             |         |      |
| 1   | STCK/SRCK clock period <sup>1</sup>         | 95          | –       | 83.3        | –       | ns   |
| 2   | STCK high to STFS (bl) high <sup>3</sup>    | 1.7         | 4.8     | 1.5         | 4.2     | ns   |
| 3   | SRCK high to SRFS (bl) high <sup>3</sup>    | -0.1        | 1.0     | -0.1        | 1.0     | ns   |
| 4   | STCK high to STFS (bl) low <sup>3</sup>     | 3.08        | 5.24    | 2.7         | 4.6     | ns   |
| 5   | SRCK high to SRFS (bl) low <sup>3</sup>     | 1.25        | 2.28    | 1.1         | 2.0     | ns   |
| 6   | STCK high to STFS (wl) high <sup>3</sup>    | 1.71        | 4.79    | 1.5         | 4.2     | ns   |
| 7   | SRCK high to SRFS (wl) high <sup>3</sup>    | -0.1        | 1.0     | -0.1        | 1.0     | ns   |
| 8   | STCK high to STFS (wl) low <sup>3</sup>     | 3.08        | 5.24    | 2.7         | 4.6     | ns   |
| 9   | SRCK high to SRFS (wl) low <sup>3</sup>     | 1.25        | 2.28    | 1.1         | 2.0     | ns   |
| 10  | STCK high to STXD valid from high impedance | 14.93       | 16.19   | 13.1        | 14.2    | ns   |
| 11a   | STCK high to STXD high                      | 1.25        | 3.42    | 1.1         | 3.0     | ns   |
| 11b   | STCK high to STXD low                       | 2.51        | 3.99    | 2.2         | 3.5     | ns   |
| 12  | STCK high to STXD high impedance            | 12.43       | 14.59   | 10.9        | 12.8    | ns   |
| 13  | SRXD setup time before SRCK low             | 20          | –       | 17.5        | –       | ns   |
| 14  | SRXD hold time after SRCK low               | 0           | –       | 0           | –       | ns   |

Table 30. SSI (Port B Alternate Function) Timing Parameter Table (Continued)

| Ref No.   | Parameter                                   | 1.8 ± 0.1 V |         | 3.0 ± 0.3 V |         | Unit |
|---|---|-------------|---------|-------------|---------|------|
|   |   | Minimum     | Maximum | Minimum     | Maximum |      |
| <b>External Clock Operation (Port B Alternate Function<sup>2</sup>)</b>             |   |             |         |             |         |      |
| 15  | STCK/SRCK clock period <sup>1</sup>         | 92.8        | –       | 81.4        | –       | ns   |
| 16  | STCK/SRCK clock high period                 | 27.1        | –       | 40.7        | –       | ns   |
| 17  | STCK/SRCK clock low period                  | 61.1        | –       | 40.7        | –       | ns   |
| 18  | STCK high to STFS (bl) high <sup>3</sup>    | –           | 92.8    | 0           | 81.4    | ns   |
| 19  | SRCK high to SRFS (bl) high <sup>3</sup>    | –           | 92.8    | 0           | 81.4    | ns   |
| 20  | STCK high to STFS (bl) low <sup>3</sup>     | –           | 92.8    | 0           | 81.4    | ns   |
| 21  | SRCK high to SRFS (bl) low <sup>3</sup>     | –           | 92.8    | 0           | 81.4    | ns   |
| 22  | STCK high to STFS (wl) high <sup>3</sup>    | –           | 92.8    | 0           | 81.4    | ns   |
| 23  | SRCK high to SRFS (wl) high <sup>3</sup>    | –           | 92.8    | 0           | 81.4    | ns   |
| 24  | STCK high to STFS (wl) low <sup>3</sup>     | –           | 92.8    | 0           | 81.4    | ns   |
| 25  | SRCK high to SRFS (wl) low <sup>3</sup>     | –           | 92.8    | 0           | 81.4    | ns   |
| 26  | STCK high to STXD valid from high impedance | 18.9        | 29.07   | 16.6        | 25.5    | ns   |
| 27a   | STCK high to STXD high                      | 9.23        | 20.75   | 8.1         | 18.2    | ns   |
| 27b   | STCK high to STXD low                       | 10.60       | 21.32   | 9.3         | 18.7    | ns   |
| 28  | STCK high to STXD high impedance            | 17.90       | 29.75   | 15.7        | 26.1    | ns   |
| 29  | SRXD setup time before SRCK low             | 1.14        | –       | 1.0         | –       | ns   |
| 30  | SRXD hold time after SRCK low               | 0           | –       | 0           | –       | ns   |
| <b>Synchronous Internal Clock Operation (Port B Alternate Function<sup>2</sup>)</b> |   |             |         |             |         |      |
| 31  | SRXD setup before STCK falling              | 18.81       | –       | 16.5        | –       | ns   |
| 32  | SRXD hold after STCK falling                | 0           | –       | 0           | –       | ns   |
| <b>Synchronous External Clock Operation (Port B Alternate Function<sup>2</sup>)</b> |   |             |         |             |         |      |
| 33  | SRXD setup before STCK falling              | 1.14        | –       | 1.0         | –       | ns   |
| 34  | SRXD hold after STCK falling                | 0           | –       | 0           | –       | ns   |

<sup>1</sup> All the timings for the SSI are given for a non-inverted serial clock polarity (TSCCKP/RSCCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

<sup>2</sup> There are 2 set of I/O signals for the SSI module. They are from Port C primary function (pad 257 to pad 261) and Port B alternate function (pad 283 to pad 288). When SSI signals are configured as outputs, they can be viewed both at Port C primary function and Port B alternate function. When SSI signals are configured as inputs, the SSI module selects the input based on FMCR register bits in the Clock controller module (CRM). By default, the input are selected from Port C primary function.

<sup>3</sup> bl = bit length; wl = word length.

## 5 Pin-Out and Package Information

Table 31 illustrates the package pin assignments for the 225-contact MAPBGA package. For a complete listing of signals, see the Signal Multiplexing Table 3 on page 8.

**Table 31. i.MXS 225 MAPBGA Pin Assignments**

|          | 1    | 2    | 3    | 4            | 5               | 6            | 7             | 8             | 9                 | 10            | 11                     | 12    | 13             | 14            | 15                    |          |
|----------|------|------|------|--------------|-----------------|--------------|---------------|---------------|-------------------|---------------|------------------------|-------|----------------|---------------|-----------------------|----------|
| <b>A</b> | PB13 | PB15 | PB19 | USBD_<br>ROE | USBD_<br>SUSPND | USBD_VM      | SSL_<br>RXFS  | SSL_<br>TXCLK | SPI1_SPI_<br>RDY  | SPI1_<br>SCLK | REV                    | PS    | LD2            | LD4           | LD5                   | <b>A</b> |
| <b>B</b> | PB11 | PB12 | PB16 | USBD_<br>AFE | USBD_<br>RCV    | USBD_<br>VMO | SSL_<br>RXDAT | UART1_<br>TXD | SPI1_<br>SS       | LSCLK         | SPL_<br>SPR            | LD0   | LD3            | LD6           | LD7                   | <b>B</b> |
| <b>C</b> | D31  | PB8  | PB14 | PB18         | PB10            | USBD_<br>VPO | UART2_<br>RXD | SSL_<br>TXFS  | UART1_<br>RTS     | CONTRAST      | FLM/VS <sub>YN</sub> C | LD8   | LD9            | LD12          | NVDD2                 | <b>C</b> |
| <b>D</b> | A23  | A24  | PB9  | PB17         | NVDD1           | USBD_<br>VP  | QVDD4         | UART2_<br>TXD | NVDD3             | SPI1_<br>MOSI | LP/HS <sub>YN</sub> C  | LD1   | LD11           | TMR2OUT       | LD13                  | <b>D</b> |
| <b>E</b> | A21  | A22  | D30  | D29          | NVDD1           | QVSS         | UART2_<br>RTS | UART1_<br>RXD | UART1_<br>CTS     | SPI1_<br>MISO | ACD/OE                 | LD10  | TIN            | PA4           | PA3                   | <b>E</b> |
| <b>F</b> | A20  | A19  | D28  | D27          | NVDD1           | NVDD1        | UART2_<br>CTS | SSL_<br>RXCLK | SSL_<br>TXDAT     | CLS           | QVDD3                  | LD14  | LD15           | PA6           | PA8                   | <b>F</b> |
| <b>G</b> | A17  | A18  | D26  | D25          | NVDD1           | NVSS         | NVDD4         | NVSS          | NVSS              | QVSS          | PWMO                   | PA7   | PA11           | PA13          | PA9                   | <b>G</b> |
| <b>H</b> | A15  | A16  | D23  | D24          | D22             | NVSS         | NVSS          | NVSS          | NVSS              | NVDD2         | PA5                    | PA12  | PA14           | I2C_SDA       | TMS                   | <b>H</b> |
| <b>J</b> | A14  | A12  | D21  | D20          | NVDD1           | NVSS         | NVSS          | QVDD1         | NVSS              | PA10          | I2C_SCL                | TCK   | TDO            | BOOT1         | BOOT0                 | <b>J</b> |
| <b>K</b> | A13  | A11  | CS2  | D19          | NVDD1           | NVSS         | QVSS          | NVDD1         | NVSS              | D1            | BOOT2                  | TDI   | BIG_<br>ENDIAN | RESET_<br>OUT | XTAL32K               | <b>K</b> |
| <b>L</b> | A10  | A9   | D17  | D18          | NVDD1           | NVDD1        | CS5           | D2            | ECB               | NVSS          | NVSS                   | POR   | QVSS           | XTAL16M       | EXTAL32K              | <b>L</b> |
| <b>M</b> | D16  | D15  | D13  | D10          | EB3             | NVDD1        | CS4           | CS1           | BCLK <sup>1</sup> | RW            | NVSS                   | BOOT3 | QVDD2          | RESET_IN      | EXTAL16M              | <b>M</b> |
| <b>N</b> | A8   | A7   | D12  | EB0          | D9              | D8           | CS3           | CS0           | PA17              | D0            | DQM2                   | DQM0  | SDCKE0         | TRISTATE      | TRST                  | <b>N</b> |
| <b>P</b> | D14  | A5   | A4   | A3           | A2              | A1           | D6            | D5            | MA10              | MA11          | DQM1                   | RAS   | SDCKE1         | CLKO          | RESET_SF <sup>2</sup> | <b>P</b> |
| <b>R</b> | A6   | D11  | EB1  | EB2          | OE              | D7           | A0            | SDCLK         | D4                | LBA           | D3                     | DQM3  | CAS            | SDWE          | AVDD1                 | <b>R</b> |
|          | 1    | 2    | 3    | 4            | 5               | 6            | 7             | 8             | 9                 | 10            | 11                     | 12    | 13             | 14            | 15                    |          |

<sup>1</sup> Burst Clock

<sup>2</sup> This signal is not used and should be floated in an actual application.

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: i.MXS Product Family

# 5.1 MAPBGA 225 Package Dimensions

Figure 54 illustrates the 225 MAPBGA 13 mm × 13 mm package.

## Case Outline 1304B

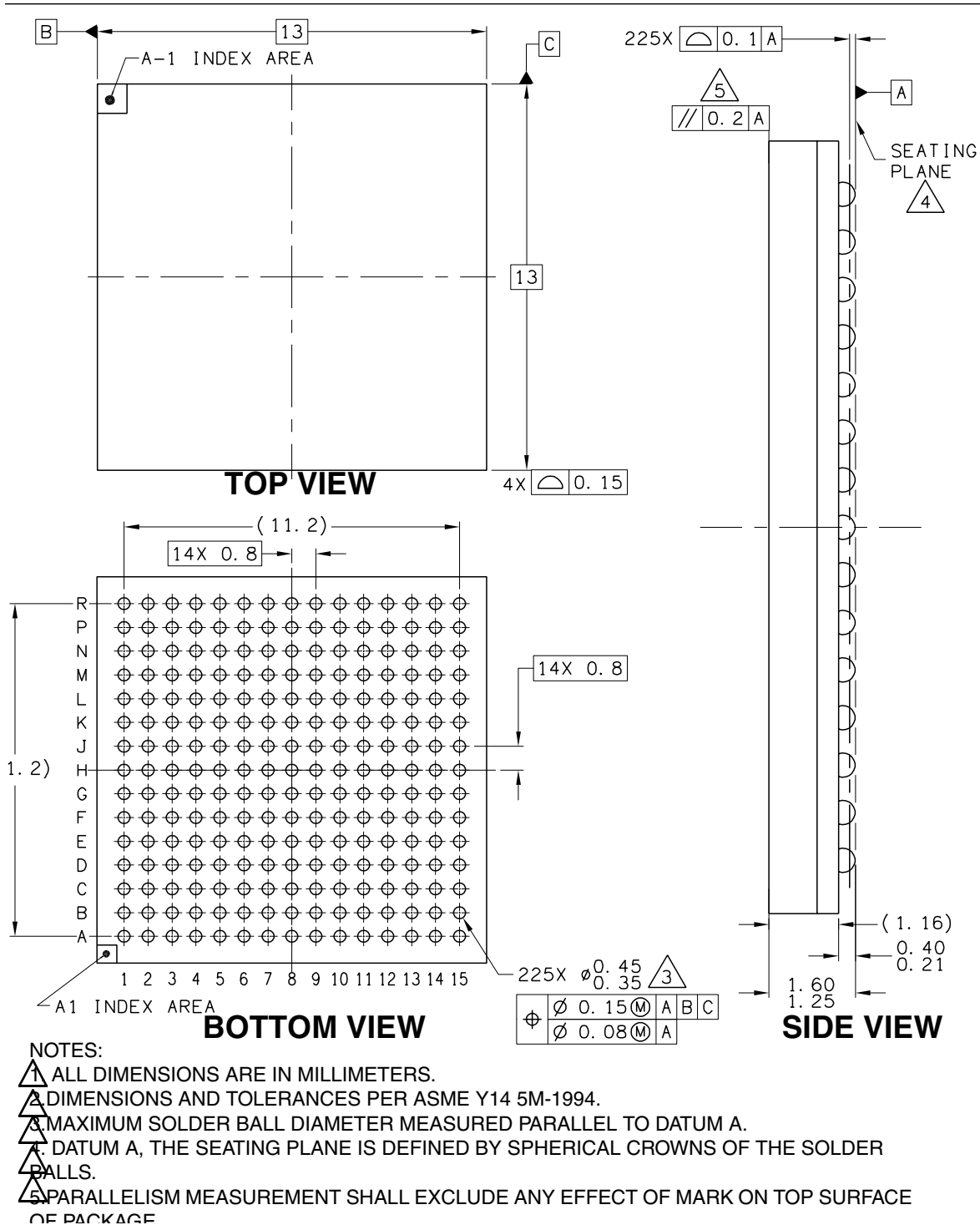


Figure 54. i.MXS 225 MAPBGA Mechanical Drawing



## 6 Product Documentation

### 6.1 Revision History

Table 32 provides revision history for this release. This history includes technical content revisions only and not stylistic or grammatical changes.

**Table 32. i.MXS Data Sheet Revision History Rev. 3**

| Location   | Revision   |
|--|--|
| Table 2 on page 4<br>Signal Names and Descriptions | <ul style="list-style-type: none"> <li>Added the DMA_REQ signal to table.</li> <li>Corrected signal name from <math>\overline{\text{USBD\_OE}}</math> to <math>\overline{\text{USBD\_ROE}}</math></li> </ul> |
| Table 3 on page 8<br>Signal Multiplex Table i.MXS  | Added Signal Multiplex table from Reference Manual with the following changes: <ul style="list-style-type: none"> <li>Corrected BGA pin assignments.</li> </ul>  |
| Table 10 on page 20                                | Changed first and second parameters descriptions:<br>From: Reference Clock freq range, To: DPLL input clock freq range<br>From: Double clock freq range, To: DPLL output freq range                          |

### 6.2 Reference Documents

The following documents are required for a complete description of the MC9328MXS and are necessary to design properly with the device. Especially for those not familiar with the ARM920T processor or previous i.MX processor products, the following documents are helpful when used in conjunction with this document.

*ARM Architecture Reference Manual* (ARM Ltd., order number ARM DDI 0100)

*ARM9DTI Data Sheet Manual* (ARM Ltd., order number ARM DDI 0029)

*ARM Technical Reference Manual* (ARM Ltd., order number ARM DDI 0151C)

*EMT9 Technical Reference Manual* (ARM Ltd., order number DDI O157E)

*MC9328MXS Product Brief* (order number MC9328MXSP)

*MC9328MXS Reference Manual* (order number MC9328MXSRM)

The Freescale manuals are available on the Freescale Semiconductors Web site at <http://www.freescale.com/imx>. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. The ARM Ltd. documentation is available from <http://www.arm.com>.

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