# DDR2 SDRAM SODIMM

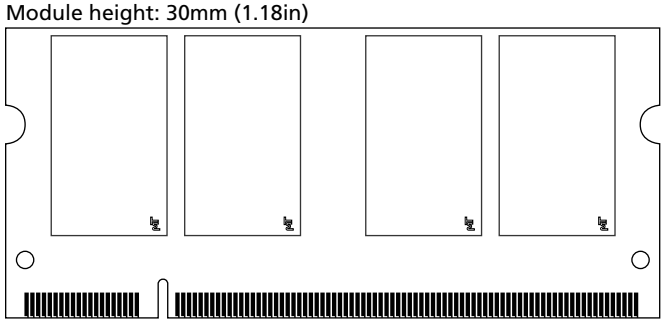
## MT8HTF3264HDY – 256MB
## MT8HTF6464HDY – 512MB
## MT8HTF12864HDY – 1GB

## Features

- 200-pin, small-outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC2-3200, PC2-4200, PC2-5300, or PC2-6400
- 256MB (32 Meg x 64), 512MB (64 Meg x 64), or 1GB (128 Meg x 64)
- $V_{DD}$ = 1.8V
- $V_{DDSPD}$ = 1.7–3.6V
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4*n*-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 $^{t}$CK
- Programmable burst lengths (BL): 4 or 8
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- On-die termination (ODT)
- Serial presence detect (SPD) with EEPROM
- Gold edge contacts
- Dual rank

**Figure 1: 200-Pin SODIMM (MO-224 R/C A)**

Module height: 30mm (1.18in)



## Options — Marking

- Operating temperature
  - Commercial (0°C ≤ $T_A$ ≤ +70°C) — D
  - Industrial (–40°C ≤ $T_A$ ≤ +85°C)[1] — T
- Package
  - 200-pin DIMM (lead-free) — Y
- Frequency/CL2
  - 2.5ns @ CL = 5 (DDR2-800) — -80E
  - 2.5ns @ CL = 6 (DDR2-800) — -800
  - 3.0ns @ CL = 5 (DDR2-667) — -667
  - 3.75ns @ CL = 4 (DDR2-553)[3] — -53E
  - 5.0ns @ CL = 3 (DDR2-400)[3] — -40E

Notes:
1. Contact Micron for industrial temperature module offerings.
2. CL = CAS (READ) latency.
3. Not recommended for new designs.

**Table 1: Key Timing Parameters**

| Speed Grade | Industry Nomenclature | Data Rate (MT/s) | | | | $^{t}$RCD (ns) | $^{t}$RP (ns) | $^{t}$RC (ns) |
|---|---|---|---|---|---|---|---|---|
| | | CL = 6 | CL = 5 | CL = 4 | CL = 3 | | | |
| -80E | PC2-6400 | 800 | 800 | 533 | 400 | 12.5 | 12.5 | 55 |
| -800 | PC2-6400 | 800 | 667 | 533 | 400 | 15 | 15 | 55 |
| -667 | PC2-5300 | – | 667 | 553 | 400 | 15 | 15 | 55 |
| -53E | PC2-4200 | – | – | 553 | 400 | 15 | 15 | 55 |
| -40E | PC2-3200 | – | – | 400 | 400 | 15 | 15 | 55 |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## Table 2: Addressing

| Parameter | 256MB | 512MB | 1GB |
|---|---|---|---|
| Refresh count | 8K | 8K | 8K |
| Row address | 8K A[12:0] | 8K A[12:0] | 8K A[12:0] |
| Device bank address | 4 BA[1:0] | 4 BA[1:0] | 8 BA[2:0] |
| Device configuration | 256Mb (16 Meg x 16) | 512Mb (32 Meg x 16) | 1Gb (64 Meg x 16) |
| Column address | 512 A[8:0] | 1K A[9:0] | 1K A[9:0] |
| Module rank address | 2 S#[1:0] | 2 S#[1:0] | 2 S#[1:0] |

## Table 3: Part Numbers and Timing Parameters – 256MB Modules

Base device: MT47H16M16,[1] 256Mb DDR2 SDRAM

| Part Number[2] | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Clock Cycles (CL-$^{t}$RCD-$^{t}$RP) |
|---|---|---|---|---|---|
| MT8HTF3264HDY-667__ | 256MB | 32 Meg x 64 | 5.3 GB/s | 3.0ns/667 MT/s | 5-5-5 |
| MT8HTF3264HTY-667__ | 256MB | 32 Meg x 64 | 5.3 GB/s | 3.0ns/667 MT/s | 5-5-5 |
| MT8HTF3264HDY-53E__ | 256MB | 32 Meg x 64 | 4.3 GB/s | 3.75ns/533 MT/s | 4-4-4 |
| MT8HTF3264HTY-53E__ | 256MB | 32 Meg x 64 | 4.3 GB/s | 3.75ns/533 MT/s | 4-4-4 |
| MT8HTF3264HDY-40E__ | 256MB | 32 Meg x 64 | 3.2 GB/s | 5.0ns/400 MT/s | 3-3-3 |
| MT8HTF3264HTY-40E__ | 256MB | 32 Meg x 64 | 3.2 GB/s | 5.0ns/400 MT/s | 3-3-3 |

## Table 4: Part Numbers and Timing Parameters – 512MB Modules

Base device: MT47H32M16,[1] 512Mb DDR2 SDRAM

| Part Number[2] | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Clock Cycles (CL-$^{t}$RCD-$^{t}$RP) |
|---|---|---|---|---|---|
| MT8HTF6464HDY-80E__ | 512MB | 64 Meg x 64 | 6.4 GB/s | 2.5ns/800 MT/s | 5-5-5 |
| MT8HTF6464HTY-80E__ | 512MB | 64 Meg x 64 | 6.4 GB/s | 2.5ns/800 MT/s | 5-5-5 |
| MT8HTF6464HDY-800__ | 512MB | 64 Meg x 64 | 6.4 GB/s | 2.5ns/800 MT/s | 6-6-6 |
| MT8HTF6464HTY-800__ | 512MB | 64 Meg x 64 | 6.4 GB/s | 2.5ns/800 MT/s | 6-6-6 |
| MT8HTF6464HDY-667__ | 512MB | 64 Meg x 64 | 5.3 GB/s | 3.0ns/667 MT/s | 5-5-5 |
| MT8HTF6464HTY-667__ | 512MB | 64 Meg x 64 | 5.3 GB/s | 3.0ns/667 MT/s | 5-5-5 |
| MT8HTF6464HDY-53E__ | 512MB | 64 Meg x 64 | 4.3 GB/s | 3.75ns/533 MT/s | 4-4-4 |
| MT8HTF6464HTY-53E__ | 512MB | 64 Meg x 64 | 4.3 GB/s | 3.75ns/533 MT/s | 4-4-4 |
| MT8HTF6464HDY-40E__ | 512MB | 64 Meg x 64 | 3.2 GB/s | 5.0ns/400 MT/s | 3-3-3 |
| MT8HTF6464HTY-40E__ | 512MB | 64 Meg x 64 | 3.2 GB/s | 5.0ns/400 MT/s | 3-3-3 |


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## Table 5: Part Numbers and Timing Parameters – 1GB Modules

Base device: MT47H64M16,[1] 1Gb DDR2 SDRAM

| Part Number[2] | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Clock Cycles (CL-$^{t}$RCD-$^{t}$RP) |
|---|---|---|---|---|---|
| MT8HTF12864HDY-80E__ | 1GB | 128 Meg x 64 | 6.4 GB/s | 2.5ns/800 MT/s | 5-5-5 |
| MT8HTF12864HTY-80E__ | 1GB | 128 Meg x 64 | 6.4 GB/s | 2.5ns/800 MT/s | 5-5-5 |
| MT8HTF12864HDY-800__ | 1GB | 128 Meg x 64 | 6.4 GB/s | 2.5ns/800 MT/s | 6-6-6 |
| MT8HTF12864HTY-800__ | 1GB | 128 Meg x 64 | 6.4 GB/s | 2.5ns/800 MT/s | 6-6-6 |
| MT8HTF12864HDY-667__ | 1GB | 128 Meg x 64 | 5.3 GB/s | 3.0ns/667 MT/s | 5-5-5 |
| MT8HTF12864HTY-667__ | 1GB | 128 Meg x 64 | 5.3 GB/s | 3.0ns/667 MT/s | 5-5-5 |
| MT8HTF12864HDY-53E__ | 1GB | 128 Meg x 64 | 4.3 GB/s | 3.75ns/533 MT/s | 4-4-4 |
| MT8HTF12864HTY-53E__ | 1GB | 128 Meg x 64 | 4.3 GB/s | 3.75ns/533 MT/s | 4-4-4 |
| MT8HTF12864HDY-40E__ | 1GB | 128 Meg x 64 | 3.2 GB/s | 5.0ns/400 MT/s | 3-3-3 |
| MT8HTF12864HTY-40E__ | 1GB | 128 Meg x 64 | 3.2 GB/s | 5.0ns/400 MT/s | 3-3-3 |

Notes:
1. The data sheet for the base device can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT8HTF6464HDY-667D3.



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# Pin Assignments and Descriptions

### Table 6: Pin Assignments

| 200-Pin DDR2 SODIMM Front | | | | | | | | 200-Pin DDR2 SODIMM Back | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 1 | $V_{REF}$ | 51 | DQS2 | 101 | A1 | 151 | DQ42 | 2 | $V_{SS}$ | 52 | DM2 | 102 | A0 | 152 | DQ46 |
| 3 | $V_{SS}$ | 53 | $V_{SS}$ | 103 | $V_{DD}$ | 153 | DQ43 | 4 | DQ4 | 54 | $V_{SS}$ | 104 | $V_{DD}$ | 154 | DQ47 |
| 5 | DQ0 | 55 | DQ18 | 105 | A10 | 155 | $V_{SS}$ | 6 | DQ5 | 56 | DQ22 | 106 | BA1 | 156 | $V_{SS}$ |
| 7 | DQ1 | 57 | DQ19 | 107 | BA0 | 157 | DQ48 | 8 | $V_{SS}$ | 58 | DQ23 | 108 | RAS# | 158 | DQ52 |
| 9 | $V_{SS}$ | 59 | $V_{SS}$ | 109 | WE# | 159 | DQ49 | 10 | DM0 | 60 | $V_{SS}$ | 110 | S0# | 160 | DQ53 |
| 11 | DQS0# | 61 | DQ24 | 111 | $V_{DD}$ | 161 | $V_{SS}$ | 12 | $V_{SS}$ | 62 | DQ28 | 112 | $V_{DD}$ | 162 | $V_{SS}$ |
| 13 | DQS0 | 63 | DQ25 | 113 | CAS# | 163 | NC | 14 | DQ6 | 64 | DQ29 | 114 | ODT0 | 164 | CK1 |
| 15 | $V_{SS}$ | 65 | $V_{SS}$ | 115 | S1# | 165 | $V_{SS}$ | 16 | DQ7 | 66 | $V_{SS}$ | 116 | NC | 166 | CK1# |
| 17 | DQ2 | 67 | DM3 | 117 | $V_{DD}$ | 167 | DQS6# | 18 | $V_{SS}$ | 68 | DQS3# | 118 | $V_{DD}$ | 168 | $V_{SS}$ |
| 19 | DQ3 | 69 | NC | 119 | ODT1 | 169 | DQS6 | 20 | DQ12 | 70 | DQS3 | 120 | NC | 170 | DM6 |
| 21 | $V_{SS}$ | 71 | $V_{SS}$ | 121 | $V_{SS}$ | 171 | $V_{SS}$ | 22 | DQ13 | 72 | $V_{SS}$ | 122 | $V_{SS}$ | 172 | $V_{SS}$ |
| 23 | DQ8 | 73 | DQ26 | 123 | DQ32 | 173 | DQ50 | 24 | $V_{SS}$ | 74 | DQ30 | 124 | DQ36 | 174 | DQ54 |
| 25 | DQ9 | 75 | DQ27 | 125 | DQ33 | 175 | DQ51 | 26 | DM1 | 76 | DQ31 | 126 | DQ37 | 176 | DQ55 |
| 27 | $V_{SS}$ | 77 | $V_{SS}$ | 127 | $V_{SS}$ | 177 | $V_{SS}$ | 28 | $V_{SS}$ | 78 | $V_{SS}$ | 128 | $V_{SS}$ | 178 | $V_{SS}$ |
| 29 | DQS1# | 79 | CKE0 | 129 | DQS4# | 179 | DQ56 | 30 | CK0 | 80 | CKE1 | 130 | DM4 | 180 | DQ60 |
| 31 | DQS1 | 81 | $V_{DD}$ | 131 | DQS4 | 181 | DQ57 | 32 | CK0# | 82 | $V_{DD}$ | 132 | $V_{SS}$ | 182 | DQ61 |
| 33 | $V_{SS}$ | 83 | NC | 133 | $V_{SS}$ | 183 | $V_{SS}$ | 34 | $V_{SS}$ | 84 | NC | 134 | DQ38 | 184 | $V_{SS}$ |
| 35 | DQ10 | 85 | NC/BA2[1] | 135 | DQ34 | 185 | DM7 | 36 | DQ14 | 86 | NC | 136 | DQ39 | 186 | DQS7# |
| 37 | DQ11 | 87 | $V_{DD}$ | 137 | DQ35 | 187 | $V_{SS}$ | 38 | DQ15 | 88 | $V_{DD}$ | 138 | $V_{SS}$ | 188 | DQS7 |
| 39 | $V_{SS}$ | 89 | A12 | 139 | $V_{SS}$ | 189 | DQ58 | 40 | $V_{SS}$ | 90 | A11 | 140 | DQ44 | 190 | $V_{SS}$ |
| 41 | $V_{SS}$ | 91 | A9 | 141 | DQ40 | 191 | DQ59 | 42 | $V_{SS}$ | 92 | A7 | 142 | DQ45 | 192 | DQ62 |
| 43 | DQ16 | 93 | A8 | 143 | DQ41 | 193 | $V_{SS}$ | 44 | DQ20 | 94 | A6 | 144 | $V_{SS}$ | 194 | DQ63 |
| 45 | DQ17 | 95 | $V_{DD}$ | 145 | $V_{SS}$ | 195 | SDA | 46 | DQ21 | 96 | $V_{DD}$ | 146 | DQS5# | 196 | $V_{SS}$ |
| 47 | $V_{SS}$ | 97 | A5 | 147 | DM5 | 197 | SCL | 48 | $V_{SS}$ | 98 | A4 | 148 | DQS5 | 198 | SA0 |
| 49 | DQS2# | 99 | A3 | 149 | $V_{SS}$ | 199 | $V_{DDSPD}$ | 50 | NC | 100 | A2 | 150 | $V_{SS}$ | 200 | SA1 |

Note: 1. Pin 85 is NC for 256MB and 512MB or BA2 for 1GB.



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# Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR2 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

**Table 7: Pin Descriptions**

| Symbol | Type | Description |
|---|---|---|
| Ax | Input | **Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments Table for density-specific addressing information. |
| BAx | Input | **Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, and MR3) is loaded during the LOAD MODE command. |
| CKx, CK#x | Input | **Clock:** Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. |
| CKEx | Input | **Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DDR2 SDRAM. |
| DMx, | Input | **Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins. |
| ODTx | Input | **On-die termination:** Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR2 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command. |
| Par_In | Input | **Parity input:** Parity bit for Ax, RAS#, CAS#, and WE#. |
| RAS#, CAS#, WE# | Input | **Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered. |
| RESET# | Input | **Reset:** Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQ are High-Z. |
| S#x | Input | **Chip select:** Enables (registered LOW) and disables (registered HIGH) the command decoder. |
| SAx | Input | **Serial address inputs:** Used to configure the SPD EEPROM address range on the $I^2C$ bus. |
| SCL | Input | **Serial clock for SPD EEPROM:** Used to synchronize communication to and from the SPD EEPROM on the $I^2C$ bus. |
| CBx | I/O | **Check bits.** Used for system error detection and correction. |
| DQx | I/O | **Data input/output:** Bidirectional data bus. |
| DQSx, DQS#x | I/O | **Data strobe:** Travels with the DQ and is used to capture DQ at the DRAM or the controller. Output with read data; input with write data for source synchronous operation. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command. |



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**Table 7: Pin Descriptions (Continued)**

| Symbol | Type | Description |
|---|---|---|
| SDA | I/O | **Serial data:** Used to transfer addresses and data into and out of the SPD EEPROM on the $I^2C$ bus. |
| RDQSx, RDQS#x | Output | **Redundant data strobe (x8 devices only):** RDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When RDQS is enabled, RDQS is output with read data only and is ignored during write data. When RDQS is disabled, RDQS becomes data mask (see DMx). RDQS# is only used when RDQS is enabled and differential data strobe mode is enabled. |
| Err_Out# | Output (open drain) | **Parity error output:** Parity error found on the command and address bus. |
| $V_{DD}/V_{DDQ}$ | Supply | **Power supply:** 1.8V ±0.1V. The component $V_{DD}$ and $V_{DDQ}$ are connected to the module $V_{DD}$. |
| $V_{DDSPD}$ | Supply | **SPD EEPROM power supply:** 1.7–3.6V. |
| $V_{REF}$ | Supply | **Reference voltage:** $V_{DD}/2$. |
| $V_{SS}$ | Supply | Ground. |
| NC | – | **No connect:** These pins are not connected on the module. |
| NF | – | **No function:** These pins are connected within the module, but provide no functionality. |
| NU | – | **Not used:** These pins are not used in specific module configurations/operations. |
| RFU | – | Reserved for future use. |



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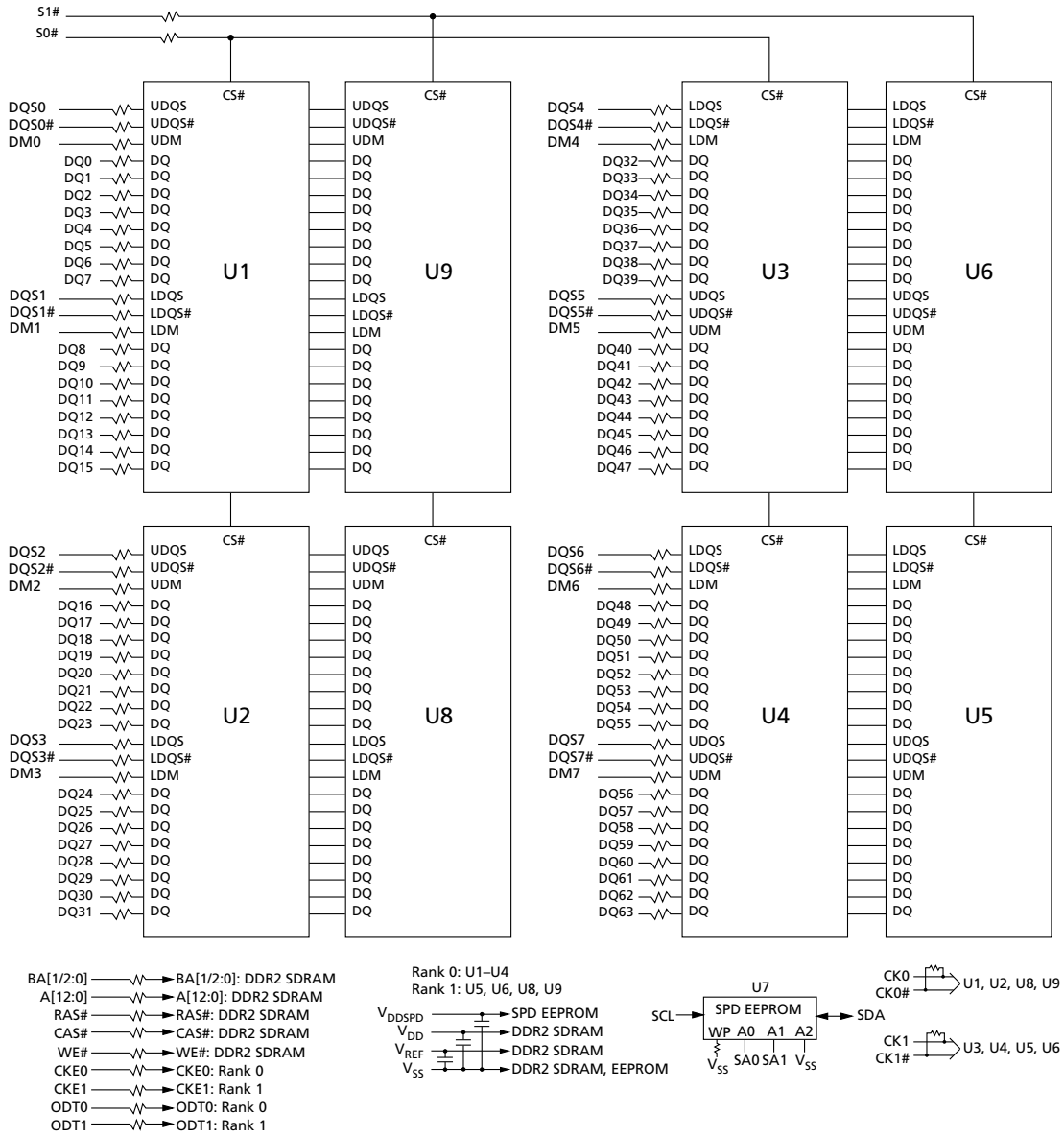
# Functional Block Diagram

### Figure 2: Functional Block Diagram





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# General Description

DDR2 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 4 or 8-bank DDR2 SDRAM devices. DDR2 SDRAM modules use DDR architecture to achieve high-speed operation. DDR2 architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR2 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals. A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

## Serial Presence-Detect EEPROM Operation

DDR2 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard $I^2C$ bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to $V_{SS}$, permanently disabling hardware write protection.



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# Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in the device data sheet are not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

**Table 8: Absolute Maximum Ratings**

| Symbol | Parameter | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$ supply voltage relative to $V_{SS}$ | | –0.5 | 2.3 | V |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin relative to $V_{SS}$ | | –0.5 | 2.3 | V |
| $I_I$ | Input leakage current; Any input 0V ≤ $V_{IN}$ ≤ $V_{DD}$; $V_{REF}$ input 0V ≤ $V_{IN}$ ≤ 0.95V; (All other pins not under test = 0V) | Address inputs, RAS#, CAS#, WE#, S#, CKE, ODT, BA | –40 | 40 | µA |
| | | CK, CK# | –20 | 20 | |
| | | DM | –10 | 10 | |
| $I_{OZ}$ | Output leakage current; 0V ≤ $V_{OUT}$ ≤ $V_{DDQ}$; DQ and ODT are disabled | DQ, DQS, DQS# | –10 | 10 | µA |
| $I_{VREF}$ | $V_{REF}$ leakage current; $V_{REF}$ = valid $V_{REF}$ level | | –16 | 16 | µA |
| $T_A$ | Module ambient operating temperature | Commercial | 0 | 70 | °C |
| | | Industrial | –40 | 85 | °C |
| $T_C$[1] | DDR2 SDRAM component operating temperature[2] | Commercial | 0 | 85 | °C |
| | | Industrial | –40 | 95 | °C |

Notes:
1. The refresh rate is required to double when $T_C$ exceeds 85°C.
2. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.



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# DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades.

### Table 9: Module and Component Speed Grades

DDR2 components may exceed the listed module speed grades; module may not be available in all listed speed grades

| Module Speed Grade | Component Speed Grade |
|---|---|
| -1GA | -187E |
| -80E | -25E |
| -800 | -25 |
| -667 | -3 |
| -53E | -37E |
| -40E | -5E |

# Design Considerations

### Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

### Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.



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# $I_{DD}$ Specifications

### Table 10: DDR2 $I_{DD}$ Specifications and Conditions – 256MB

Values shown for MT47H16M16 DDR2 SDRAM only and are computed from values specified in the 256Mb (16 Meg x 16) component data sheet

| Parameter | | Symbol | -667 | -53E | -40E | Units |
|---|---|---|---|---|---|---|
| **Operating one bank active-precharge current:** $^tCK = ^tCK (I_{DD})$, $^tRC = ^tRC (I_{DD})$, $^tRAS = ^tRAS$ MIN $(I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | | $I_{DD0}$[1] | 380 | 340 | 320 | mA |
| **Operating one bank active-read-precharge current:** $I_{OUT}$ = 0mA; BL = 4, CL = CL $(I_{DD})$, AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRC = ^tRC (I_{DD})$, $^tRAS = ^tRAS$ MIN $(I_{DD})$, $^tRCD = ^tRCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as $I_{DD4W}$ | | $I_{DD1}$[1] | 420 | 380 | 360 | mA |
| **Precharge power-down current:** All device banks idle; $^tCK = ^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | | $I_{DD2P}$[2] | 40 | 40 | 40 | mA |
| **Precharge quiet standby current:** All device banks idle; $^tCK = ^tCK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating | | $I_{DD2Q}$[2] | 400 | 280 | 200 | mA |
| **Precharge standby current:** All device banks idle; $^tCK = ^tCK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching | | $I_{DD2N}$[2] | 320 | 280 | 240 | mA |
| **Active power-down current:** All device banks open; $^tCK = ^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | Fast PDN exit MR[12] = 0 | $I_{DD3P}$[2] | 240 | 200 | 160 | mA |
| | Slow PDN exit MR[12] = 1 | | 48 | 48 | 48 | |
| **Active standby current:** All device banks open; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRAS$ MAX $(I_{DD})$, $^tRP = ^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | | $I_{DD3N}$[2] | 440 | 320 | 240 | mA |
| **Operating burst write current:** All device banks open; Continuous burst writes; BL = 4, CL = CL $(I_{DD})$, AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRAS$ MAX $(I_{DD})$, $^tRP = ^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | | $I_{DD4W}$[1] | 880 | 740 | 580 | mA |
| **Operating burst read current:** All device banks open; Continuous burst read, $I_{OUT}$ = 0mA; BL = 4, CL = CL $(I_{DD})$, AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRAS$ MAX $(I_{DD})$, $^tRP = ^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | | $I_{DD4R}$[1] | 780 | 660 | 500 | mA |
| **Burst refresh current:** $^tCK = ^tCK (I_{DD})$; REFRESH command at every $^tRFC (I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | | $I_{DD5}$[2] | 1440 | 1360 | 1320 | mA |
| **Self refresh current:** CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating | | $I_{DD6}$[2] | 40 | 40 | 40 | mA |



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**Table 10: DDR2 $I_{DD}$ Specifications and Conditions – 256MB (Continued)**

Values shown for MT47H16M16 DDR2 SDRAM only and are computed from values specified in the 256Mb (16 Meg x 16) component data sheet

| Parameter | Symbol | -667 | -53E | -40E | Units |
|---|---|---|---|---|---|
| **Operating bank interleave read current:** All device banks interleaving reads; $I_{OUT}$ = 0mA; BL = 4, CL = CL ($I_{DD}$), AL = $^{t}$RCD ($I_{DD}$) - 1 × $^{t}$CK ($I_{DD}$); $^{t}$CK = $^{t}$CK ($I_{DD}$), $^{t}$RC = $^{t}$RC ($I_{DD}$), $^{t}$RRD = $^{t}$RRD ($I_{DD}$), $^{t}$RCD = $^{t}$RCD ($I_{DD}$); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching | $I_{DD7}$[1] | 1020 | 980 | 940 | mA |

Notes:
1. Value calculated as one module rank in this operating condition; all other module ranks in $I_{DD2P}$ (CKE LOW) mode.
2. Value calculated reflects all module ranks in this operating condition.



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## Table 11: DDR2 $I_{DD}$ Specifications and Conditions – 512MB

Values shown for MT47H32M16 DDR2 SDRAM only and are computed from values specified in the 512Mb (32 Meg x 16) component data sheet

| Parameter | | Symbol | -80E/-800 | -667 | -53E | -40E | Units |
|---|---|---|---|---|---|---|---|
| **Operating one bank active-precharge current:** $^tCK = ^tCK (I_{DD})$, $^tRC = ^tRC (I_{DD})$, $^tRAS = ^tRAS$ MIN $(I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | | $I_{DD0}$[1] | 560 | 500 | 460 | 440 | mA |
| **Operating one bank active-read-precharge current:** $I_{OUT}$ = 0mA; BL = 4, CL = CL $(I_{DD})$, AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRC = ^tRC (I_{DD})$, $^tRAS = ^tRAS$ MIN $(I_{DD})$, $^tRCD = ^tRCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as $I_{DD4W}$ | | $I_{DD1}$[1] | 680 | 620 | 560 | 520 | mA |
| **Precharge power-down current:** All device banks idle; $^tCK = ^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | | $I_{DD2P}$[2] | 56 | 56 | 56 | 56 | mA |
| **Precharge quiet standby current:** All device banks idle; $^tCK = ^tCK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating | | $I_{DD2Q}$[2] | 520 | 440 | 360 | 320 | mA |
| **Precharge standby current:** All device banks idle; $^tCK = ^tCK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching | | $I_{DD2N}$[2] | 560 | 480 | 400 | 360 | mA |
| **Active power-down current:** All device banks open; $^tCK = ^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | Fast PDN exit MR[12] = 0 | $I_{DD3P}$[2] | 320 | 280 | 240 | 200 | mA |
| | Slow PDN exit MR[12] = 1 | | 96 | 96 | 96 | 96 | |
| **Active standby current:** All device banks open; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRAS$ MAX $(I_{DD})$, $^tRP = ^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | | $I_{DD3N}$[2] | 600 | 560 | 480 | 400 | mA |
| **Operating burst write current:** All device banks open; Continuous burst writes; BL = 4, CL = CL $(I_{DD})$, AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRAS$ MAX $(I_{DD})$, $^tRP = ^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | | $I_{DD4W}$[1] | 1200 | 1020 | 840 | 640 | mA |
| **Operating burst read current:** All device banks open; Continuous burst read, $I_{OUT}$ = 0mA; BL = 4, CL = CL $(I_{DD})$, AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRAS$ MAX $(I_{DD})$, $^tRP = ^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | | $I_{DD4R}$[1] | 1120 | 960 | 800 | 620 | mA |
| **Burst refresh current:** $^tCK = ^tCK (I_{DD})$; REFRESH command at every $^tRFC$ $(I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | | $I_{DD5}$[2] | 1840 | 1480 | 1400 | 1360 | mA |
| **Self refresh current:** CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating | | $I_{DD6}$[2] | 56 | 56 | 56 | 56 | mA |



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**Table 11: DDR2 $I_{DD}$ Specifications and Conditions – 512MB (Continued)**

Values shown for MT47H32M16 DDR2 SDRAM only and are computed from values specified in the 512Mb (32 Meg x 16) component data sheet

| Parameter | Symbol | -80E/-800 | -667 | -53E | -40E | Units |
|---|---|---|---|---|---|---|
| **Operating bank interleave read current:** All device banks interleaving reads; $I_{OUT}$ = 0mA; BL = 4, CL = CL ($I_{DD}$), AL = $^{t}$RCD ($I_{DD}$) - 1 × $^{t}$CK ($I_{DD}$); $^{t}$CK = $^{t}$CK ($I_{DD}$), $^{t}$RC = $^{t}$RC ($I_{DD}$), $^{t}$RRD = $^{t}$RRD ($I_{DD}$), $^{t}$RCD = $^{t}$RCD ($I_{DD}$); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching | $I_{DD7}$[1] | 1500 | 1420 | 1380 | 1360 | mA |



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## Table 12: DDR2 $I_{DD}$ Specifications and Conditions – 1GB (Die Revision A)

Values shown for MT47H64M16 DDR2 SDRAM only and are computed from values specified in the 1Gb (64 Meg x 16) component data sheet

| Parameter | | Symbol | -667 | -53E | -40E | Units |
|---|---|---|---|---|---|---|
| **Operating one bank active-precharge current:** $^tCK = {}^tCK (I_{DD})$, $^tRC = {}^tRC (I_{DD})$, $^tRAS = {}^tRAS$ MIN $(I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | | $I_{DD0}$[1] | 560 | 460 | 440 | mA |
| **Operating one bank active-read-precharge current:** $I_{OUT}$ = 0mA; BL = 4, CL = CL $(I_{DD})$, AL = 0; $^tCK = {}^tCK (I_{DD})$, $^tRC = {}^tRC (I_{DD})$, $^tRAS = {}^tRAS$ MIN $(I_{DD})$, $^tRCD = {}^tRCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as $I_{DD4W}$ | | $I_{DD1}$[1] | 540 | 500 | 460 | mA |
| **Precharge power-down current:** All device banks idle; $^tCK = {}^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | | $I_{DD2P}$[2] | 56 | 56 | 56 | mA |
| **Precharge quiet standby current:** All device banks idle; $^tCK = {}^tCK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating | | $I_{DD2Q}$[2] | 520 | 360 | 320 | mA |
| **Precharge standby current:** All device banks idle; $^tCK = {}^tCK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching | | $I_{DD2N}$[2] | 560 | 400 | 320 | mA |
| **Active power-down current:** All device banks open; $^tCK = {}^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | Fast PDN exit MR[12] = 0 | $I_{DD3P}$[2] | 320 | 280 | 280 | mA |
| | Slow PDN exit MR[12] = 1 | | 112 | 112 | 112 | |
| **Active standby current:** All device banks open; $^tCK = {}^tCK (I_{DD})$, $^tRAS = {}^tRAS$ MAX $(I_{DD})$, $^tRP = {}^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | | $I_{DD3N}$[2] | 600 | 480 | 440 | mA |
| **Operating burst write current:** All device banks open; Continuous burst writes; BL = 4, CL = CL $(I_{DD})$, AL = 0; $^tCK = {}^tCK (I_{DD})$, $^tRAS = {}^tRAS$ MAX $(I_{DD})$, $^tRP = {}^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | | $I_{DD4W}$[1] | 820 | 740 | 640 | mA |
| **Operating burst read current:** All device banks open; Continuous burst read, $I_{OUT}$ = 0mA; BL = 4, CL = CL $(I_{DD})$, AL = 0; $^tCK = {}^tCK (I_{DD})$, $^tRAS = {}^tRAS$ MAX $(I_{DD})$, $^tRP = {}^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | | $I_{DD4R}$[1] | 900 | 740 | 640 | mA |
| **Burst refresh current:** $^tCK = {}^tCK (I_{DD})$; REFRESH command at every $^tRFC (I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | | $I_{DD5}$[2] | 2160 | 2000 | 1920 | mA |
| **Self refresh current:** CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating | | $I_{DD6}$[2] | 24 | 24 | 24 | mA |
| **Operating bank interleave read current:** All device banks interleaving reads; $I_{OUT}$ = 0mA; BL = 4, CL = CL $(I_{DD})$, AL = $^tRCD (I_{DD})$ - 1 × $^tCK (I_{DD})$; $^tCK = {}^tCK (I_{DD})$, $^tRC = {}^tRC (I_{DD})$, $^tRRD = {}^tRRD (I_{DD})$, $^tRCD = {}^tRCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching | | $I_{DD7}$[1] | 1420 | 1380 | 1320 | mA |


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## Table 13: DDR2 $I_{DD}$ Specifications and Conditions – 1GB (Die Revision E and G)

Values shown for MT47H64M16 DDR2 SDRAM only and are computed from values specified in the 1Gb (64 Meg x 16) component data sheet

| Parameter | | Symbol | -80E/-800 | -667 | -53E | -40E | Units |
|---|---|---|---|---|---|---|---|
| **Operating one bank active-precharge current:** $^tCK = {}^tCK (I_{DD})$, $^tRC = {}^tRC (I_{DD})$, $^tRAS = {}^tRAS$ MIN $(I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | | $I_{DD0}$[1] | 628 | 568 | 468 | 468 | mA |
| **Operating one bank active-read-precharge current:** $I_{OUT}$ = 0mA; BL = 4, CL = CL $(I_{DD})$, AL = 0; $^tCK = {}^tCK (I_{DD})$, $^tRC = {}^tRC (I_{DD})$, $^tRAS = {}^tRAS$ MIN $(I_{DD})$, $^tRCD = {}^tRCD (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as $I_{DD4W}$ | | $I_{DD1}$[1] | 728 | 548 | 508 | 488 | mA |
| **Precharge power-down current:** All device banks idle; $^tCK = {}^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | | $I_{DD2P}$[2] | 56 | 56 | 56 | 56 | mA |
| **Precharge quiet standby current:** All device banks idle; $^tCK = {}^tCK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating | | $I_{DD2Q}$[2] | 600 | 520 | 360 | 320 | mA |
| **Precharge standby current:** All device banks idle; $^tCK = {}^tCK (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching | | $I_{DD2N}$[2] | 640 | 560 | 400 | 320 | mA |
| **Active power-down current:** All device banks open; $^tCK = {}^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | Fast PDN exit MR[12] = 0 | $I_{DD3P}$[2] | 320 | 240 | 240 | 240 | mA |
| | Slow PDN exit MR[12] = 1 | | 80 | 80 | 80 | 80 | |
| **Active standby current:** All device banks open; $^tCK = {}^tCK (I_{DD})$, $^tRAS = {}^tRAS$ MAX $(I_{DD})$, $^tRP = {}^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | | $I_{DD3N}$[2] | 680 | 600 | 480 | 440 | mA |
| **Operating burst write current:** All device banks open; Continuous burst writes; BL = 4, CL = CL $(I_{DD})$, AL = 0; $^tCK = {}^tCK (I_{DD})$, $^tRAS = {}^tRAS$ MAX $(I_{DD})$, $^tRP = {}^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | | $I_{DD4W}$[1] | 1288 | 828 | 748 | 668 | mA |
| **Operating burst read current:** All device banks open; Continuous burst read, $I_{OUT}$ = 0mA; BL = 4, CL = CL $(I_{DD})$, AL = 0; $^tCK = {}^tCK (I_{DD})$, $^tRAS = {}^tRAS$ MAX $(I_{DD})$, $^tRP = {}^tRP (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | | $I_{DD4R}$[1] | 1308 | 908 | 748 | 668 | mA |
| **Burst refresh current:** $^tCK = {}^tCK (I_{DD})$; REFRESH command at every $^tRFC (I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | | $I_{DD5}$[2] | 2240 | 2160 | 2000 | 1920 | mA |
| **Self refresh current:** CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating | | $I_{DD6}$[2] | 56 | 56 | 56 | 56 | mA |


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**Table 13: DDR2 $I_{DD}$ Specifications and Conditions – 1GB (Die Revision E and G) (Continued)**

Values shown for MT47H64M16 DDR2 SDRAM only and are computed from values specified in the 1Gb (64 Meg x 16) component data sheet

| Parameter | Symbol | -80E/-800 | -667 | -53E | -40E | Units |
|---|---|---|---|---|---|---|
| **Operating bank interleave read current:** All device banks interleaving reads; $I_{OUT}$ = 0mA; BL = 4, CL = CL ($I_{DD}$), AL = $^{t}$RCD ($I_{DD}$) - 1 × $^{t}$CK ($I_{DD}$); $^{t}$CK = $^{t}$CK ($I_{DD}$), $^{t}$RC = $^{t}$RC ($I_{DD}$), $^{t}$RRD = $^{t}$RRD ($I_{DD}$), $^{t}$RCD = $^{t}$RCD ($I_{DD}$); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching | $I_{DD7}$[1] | 1788 | 1428 | 1348 | 1228 | mA |



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# Serial Presence-Detect

For the latest SPD data, refer to Micron's SPD page: www.micron.com/SPD.

### Table 14: SPD EEPROM Operating Conditions

| Parameter/Condition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Supply voltage | $V_{DDSPD}$ | 1.7 | 3.6 | V |
| Input high voltage: logic 1; All inputs | $V_{IH}$ | $V_{DDSPD}$ × 0.7 | $V_{DDSPD}$ + 0.5 | V |
| Input low voltage: logic 0; All inputs | $V_{IL}$ | –0.6 | $V_{DDSPD}$ × 0.3 | V |
| Output low voltage: $I_{OUT}$ = 3mA | $V_{OL}$ | – | 0.4 | V |
| Input leakage current: $V_{IN}$ = GND to $V_{DD}$ | $I_{LI}$ | 0.1 | 3 | µA |
| Output leakage current: $V_{OUT}$ = GND to $V_{DD}$ | $I_{LO}$ | 0.05 | 3 | µA |
| Standby current | $I_{SB}$ | 1.6 | 4 | µA |
| Power supply current, READ: SCL clock frequency = 100 kHz | $I_{CCR}$ | 0.4 | 1 | mA |
| Power supply current, WRITE: SCL clock frequency = 100 kHz | $I_{CCW}$ | 2 | 3 | mA |

### Table 15: SPD EEPROM AC Operating Conditions

| Parameter/Condition | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| SCL LOW to SDA data-out valid | $^{t}AA$ | 0.2 | 0.9 | µs | 1 |
| Time bus must be free before a new transition can start | $^{t}BUF$ | 1.3 | – | µs | |
| Data-out hold time | $^{t}DH$ | 200 | – | ns | |
| SDA and SCL fall time | $^{t}F$ | – | 300 | ns | 2 |
| SDA and SCL rise time | $^{t}R$ | – | 300 | ns | 2 |
| Data-in hold time | $^{t}HD:DAT$ | 0 | – | µs | |
| Start condition hold time | $^{t}HD:STA$ | 0.6 | – | µs | |
| Clock HIGH period | $^{t}HIGH$ | 0.6 | – | µs | |
| Noise suppression time constant at SCL, SDA inputs | $^{t}I$ | – | 50 | µs | |
| Clock LOW period | $^{t}LOW$ | 1.3 | – | µs | |
| SCL clock frequency | $^{t}SCL$ | – | 400 | kHz | |
| Data-in setup time | $^{t}SU:DAT$ | 100 | – | ns | |
| Start condition setup time | $^{t}SU:STA$ | 0.6 | – | µs | 3 |
| Stop condition setup time | $^{t}SU:STO$ | 0.6 | – | µs | |
| WRITE cycle time | $^{t}WRC$ | – | 10 | ms | 4 |

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time ($^{t}WRC$) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.


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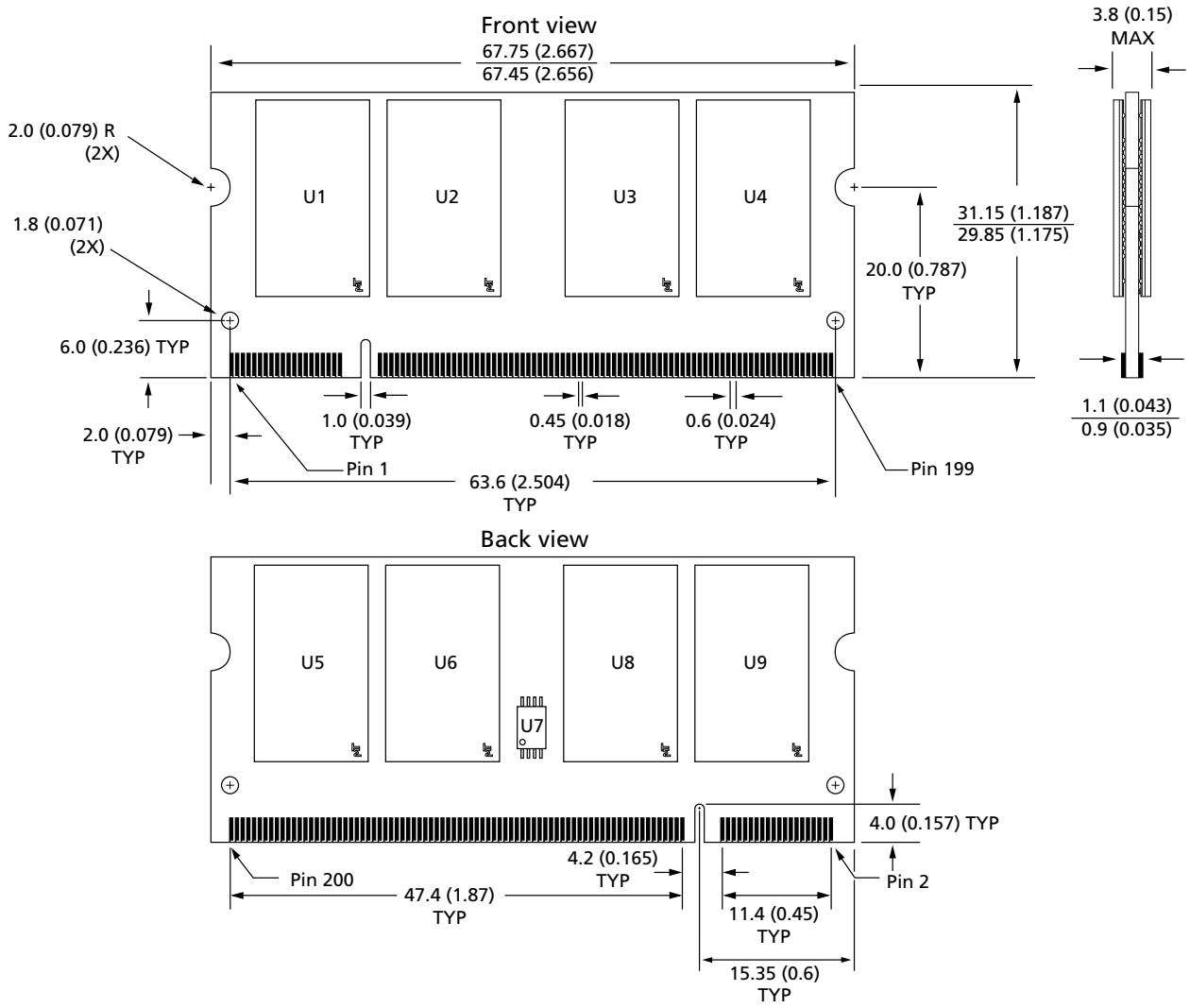
# Module Dimensions

**Figure 3: 200-Pin DDR2 SODIMM**




Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.


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