



1Mx32 SRAM 3.3V MODULE

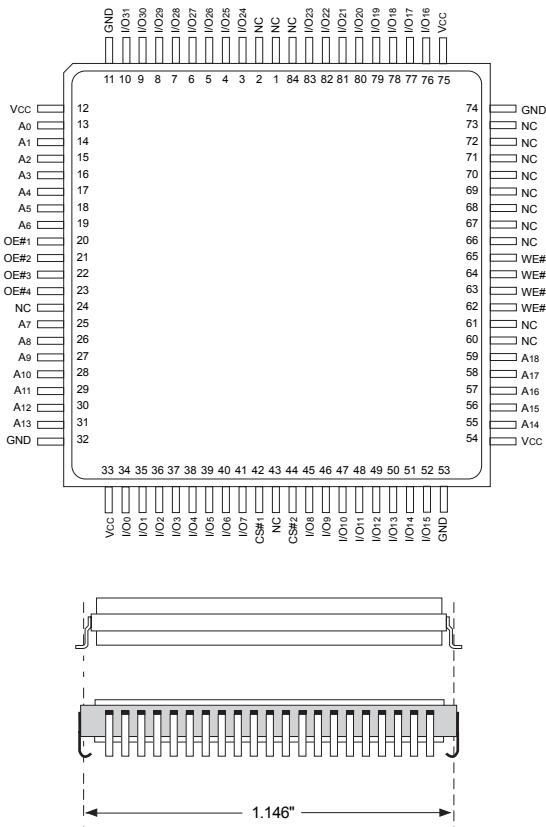
FEATURES

- Access Times of 17, 20, 25ns
- 84 lead, 28mm CQFP, (Package 511)
- Organized as two banks of 512Kx32, User Configurable as 2Mx16 or 4Mx8
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- 3.3V Power Supply
- Low Power CMOS
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight - WS1M32V-XG3X - 20 grams typical

*This product is under development, is not qualified or characterized and is subject to change without notice.

PIN CONFIGURATION FOR WS1M32V-XG3X

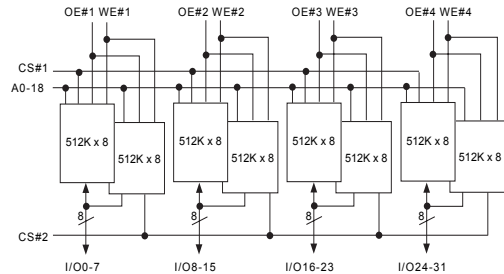
TOP VIEW



PIN DESCRIPTION

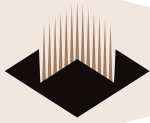
I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
WE#1-4	Write Enables
CS#1-2	Chip Selects
OE#1-4	Output Enables
Vcc	+3.3V Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



Note: CS#1 & CS#2 are used as bank select

The WEDC 84 lead G3 CQFP fills the same fit and function as the JEDEC 84 lead CQFJ or 84 PLCC. But the G3 has the TCE and lead inspection advantage of the CQFP form.



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	4.6	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	4.6	V

TRUTH TABLE

CS#	OE#	WE#	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	3.0	3.6	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE#1-4 capacitance	COE	V _{IN} = 0V, f = 1.0MHz	20	pF
WE#1-4 capacitance	CWE	V _{IN} = 0V, f = 1.0MHz	20	pF
CS#1-2 capacitance	CCS	V _{IN} = 0V, f = 1.0MHz	50	pF
Data I/O capacitance	CI/O	VI/O = 0V, f = 1.0MHz	20	pF
Address input capacitance	CAD	V _{IN} = 0V, f = 1.0MHz	70	pF

This parameter is guaranteed by design, but not tested.

DC CHARACTERISTICS

V_{CC} = 3.3V ± 0.3V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I _{LI}	V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	CS# = V _{IH} , OE# = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
Operating Supply Current (x 32 Mode)	I _{CC} x 32	CS# = V _{IL} , OE# = V _{IH} , f = 5MHz, V _{CC} = 3.6V		520	mA
Standby Current	ISB	CS# = V _{IH} , OE# = V _{IH} , f = 5MHz, V _{CC} = 3.6V		400	mA
Output Low Voltage	V _{OL}	I _{OL} = 4.0mA		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V
Contact Factory for low power option.



AC CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	-17		-20		-25		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle								
Read Cycle Time	t _{RC}	17		20		25		ns
Address Access Time	t _{AA}		17		20		25	ns
Output Hold from Address Change	t _{OH}	0		0		0		ns
Chip Select Access Time	t _{ACS}		17		20		25	ns
Output Enable to Output Valid	t _{OE}		10		10		12	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	1		1		1		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	0		0		0		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		12		12		12	ns
Output Disable to Output in High Z	t _{OHZ} ¹		12		12		12	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS

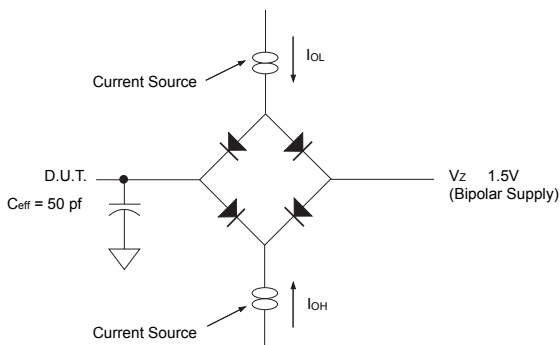
V_{CC} = 3.3V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	-17		-20		-25		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle								
Write Cycle Time	t _{WC}	17		20		25		ns
Chip Select to End of Write	t _{OW}	15		15		17		ns
Address Valid to End of Write	t _{AW}	15		15		17		ns
Data Valid to End of Write	t _{DW}	11		12		13		ns
Write Pulse Width	t _{WP}	15		15		17		ns
Address Setup Time	t _{AS}	2		2		2		ns
Address Hold Time	t _{AH}	0		0		0		ns
Output Active from End of Write	t _{OW} ¹	2		3		4		ns
Write Enable to Output in High Z	t _{WHZ} ¹		9		11		13	ns
Data Hold Time	t _{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT

AC TEST CONDITIONS

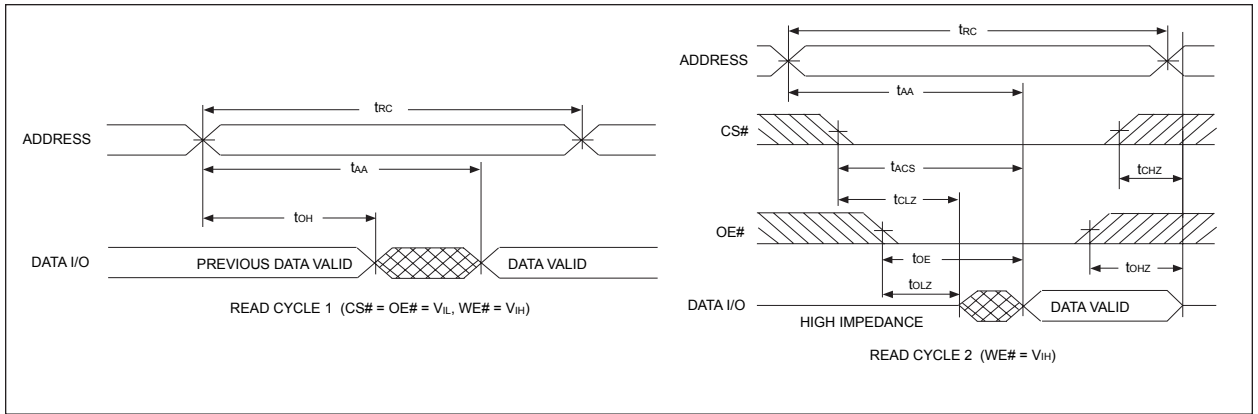


Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

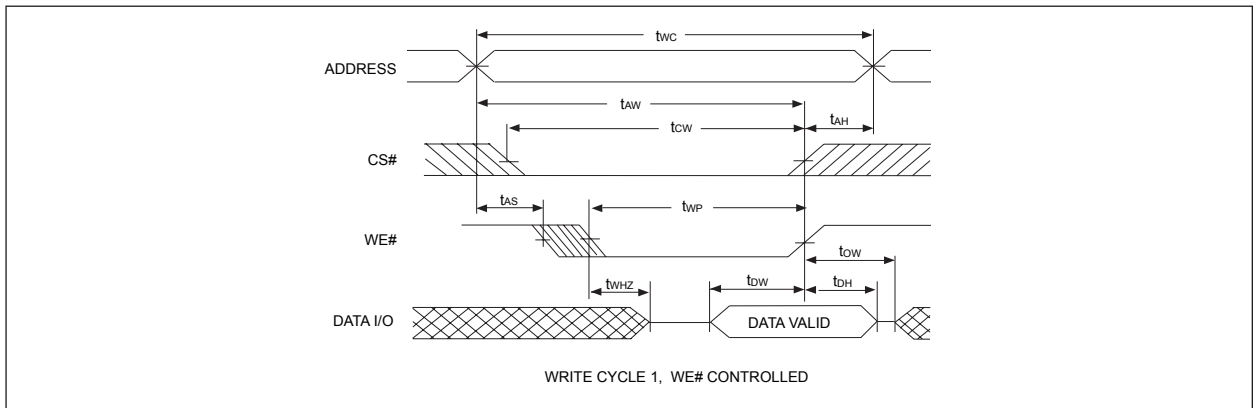
Notes:
 V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance Z₀ = 75.
 V_Z is typically the midpoint of V_{OH} and V_{OL}.
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.



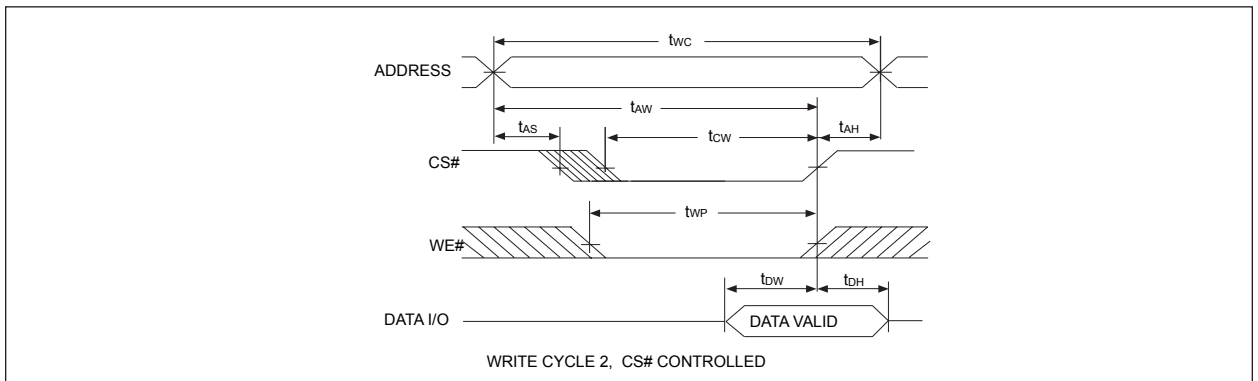
TIMING WAVEFORM - READ CYCLE



WRITE CYCLE - WE# CONTROLLED

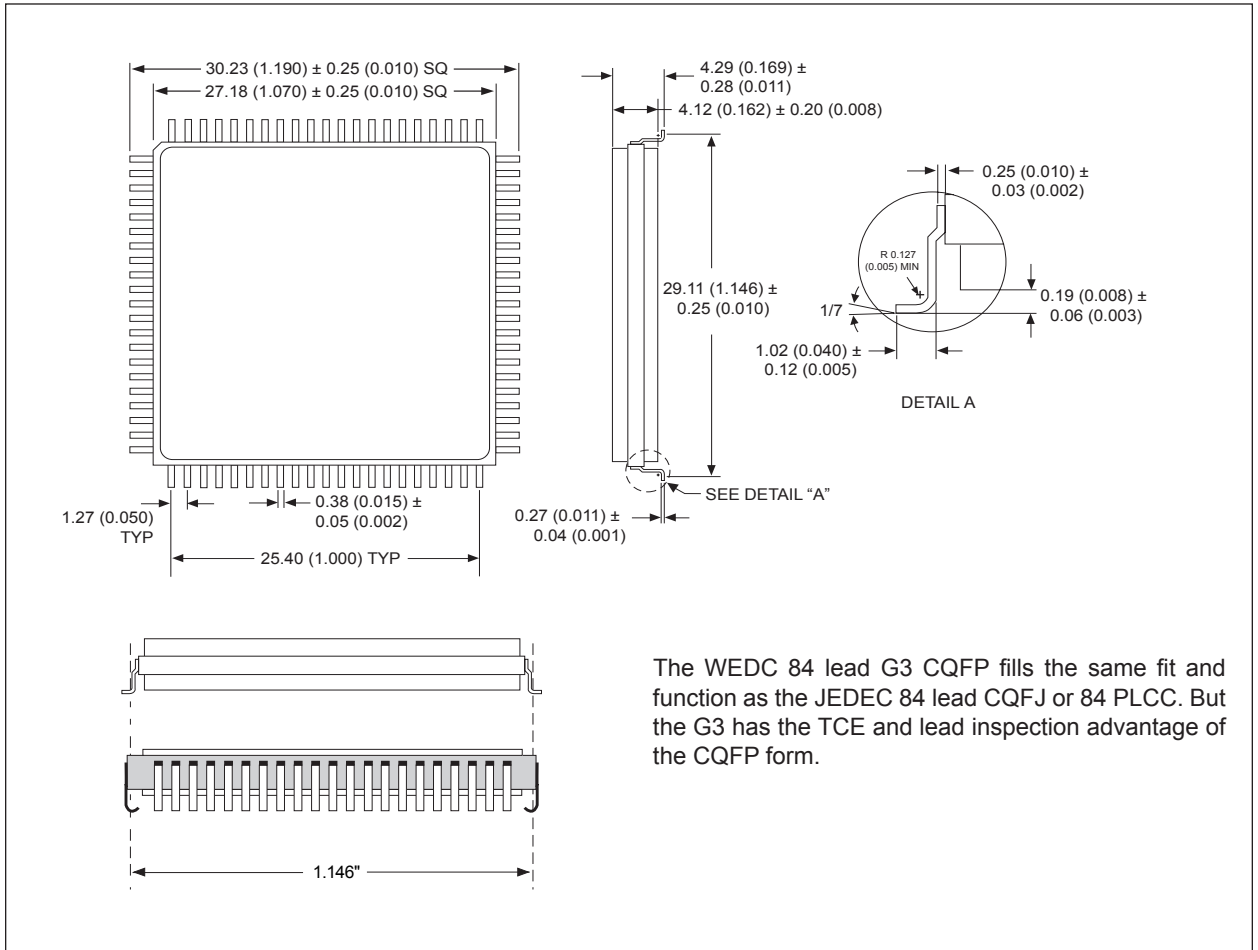


WRITE CYCLE - CS# CONTROLLED





PACKAGE 511: 84 LEAD, CERAMIC QUAD FLAT PACK (G3)



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ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

