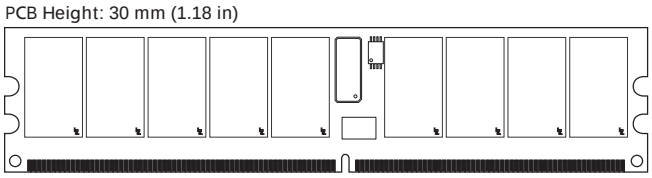
DDR2 SDRAM Registered DIMM

MT18HTF6472(P)D – 512MB
MT18HTF12872(P)D – 1GB
MT18HTF25672(P)D – 2GB

Features

- Supports 95°C with double refresh
- 240-pin, registered dual in-line memory module
- Fast data transfer rates: PC2-3200, PC2-4200, PC2-5300, or PC2-6400
- Supports ECC error detection and correction
- $V_{DD} = V_{DD}Q = +1.8V$
- $V_{DDSPD} = +1.7V$ to $+3.6V$
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Dual rank
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL)
- Posted CAS# additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts

Figure 1: 240-Pin DIMM (MO-237 R/C "B")



Options — Marking

- Parity — P
- Package
  - 240-pin DIMM (lead-free) — Y
- Frequency/CAS latency[1]
  - 2.5ns @ CL = 5 (DDR2-800)[2] — -80E
  - 2.5ns @ CL = 6 (DDR2-800)[2] — -800
  - 3.0ns @ CL = 5 (DDR2-667) — -667
  - 3.75ns @ CL = 4 (DDR2-533) — -53E
  - 5.0ns @ CL = 3 (DDR2-400) — -40E
- PCB height
  - 30mm (1.18 in)

Notes: 1. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.
2. Not available in 512MB module density.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)				^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
		CL = 6	CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	–	800	533	–	12.5	12.5	55
-800	PC2-6400	800	667	–	–	15	15	55
-667	PC2-5300	–	667	533	400	15	15	55
-53E	PC2-4200	–	–	533	400	15	15	55
-40E	PC2-3200	–	–	400	400	15	15	55

Table 2: Addressing

	512MB	1GB	2GB
Refresh count	8K	8K	8K
Row address	8K (A0–A12)	16K (A0–A13)	16K (A0–A13)
Device bank address	4 (BA0, BA1)	4 (BA0, BA1)	8 (BA0, BA1, BA2)
Device page size per bank	1KB	1KB	1KB
Device configuration	256Mb (32 Meg x 8)	512Mb (64 Meg x 8)	1Gb (128 Meg x 8)
Column address	1K (A0–A9)	1K (A0–A9)	1K (A0–A9)
Module rank address	2 (S0#, S1#)	2 (S0#, S1#)	2 (S0#, S1#)

Table 3: Part Numbers and Timing Parameters – 512MB Modules
Base device: MT47H32M8, 256Mb DDR2 SDRAM

Part Number[1]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - ^{t}RCD - ^{t}RP)
MT18HTF6472(P)D(P)Y-667__	512MB	64 Meg x72	5.3 GB/s	3.0ns/667MT/s	5-5-5
MT18HTF6472(P)D(P)Y-53E__	512MB	64 Meg x72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT18HTF6472(P)D(P)Y-40E__	512MB	64 Meg x72	3.2 GB/s	5.0ns/400MT/s	3-3-3

Table 4: Part Numbers and Timing Parameters – 1GB Modules
Base device: MT47H64M8, 512Mb DDR2 SDRAM

Part Number[1]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - ^{t}RCD - ^{t}RP)
MT18HTF12872(P)D(P)Y-80E__	1GB	128 Meg x72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT18HTF12872(P)D(P)Y-800__	1GB	128 Meg x72	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT18HTF12872(P)D(P)Y-667__	1GB	128 Meg x72	5.3 GB/s	3.0ns/667MT/s	5-5-5
MT18HTF12872(P)D(P)Y-53E__	1GB	128 Meg x72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT18HTF12872(P)D(P)Y-40E__	1GB	128 Meg x72	3.2 GB/s	5.0ns/400MT/s	3-3-3

Table 5: Part Numbers and Timing Parameters – 2GB Modules
Base device: MT47H128M8, 1Gb DDR2 SDRAM

Part Number[1]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - ^{t}RCD - ^{t}RP)
MT18HTF25672(P)D(P)Y-80E__	2GB	256 Meg x72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT18HTF25672(P)D(P)Y-800__	2GB	256 Meg x72	6.4 GB/s	2.5ns/800MT/s	6-6-6
MT18HTF25672(P)D(P)Y-667__	2GB	256 Meg x72	5.3 GB/s	3.0ns/667MT/s	5-5-5
MT18HTF25672(P)D(P)Y-53E__	2GB	256 Meg x72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT18HTF25672(P)D(P)Y-40E__	2GB	256 Meg x72	3.2 GB/s	5.0ns/400MT/s	3-3-3

Notes: 1. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT18HTF12872(P)DY-667C2.

Pin Assignments and Descriptions

Table 6: Pin Assignments

240-Pin RDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	31	DQ19	61	A4	91	VSS
2	VSS	32	VSS	62	VDDQ	92	DQS5#
3	DQ0	33	DQ24	63	A2	93	DQS5
4	DQ1	34	DQ25	64	VDD	94	VSS
5	VSS	35	VSS	65	VSS	95	DQ42
6	DQS0#	36	DQS3#	66	VSS	96	DQ43
7	DQS0	37	DQS3	67	VDD	97	VSS
8	VSS	38	VSS	68	PAR_IN	98	DQ48
9	DQ2	39	DQ26	69	VDD	99	DQ49
10	DQ3	40	DQ27	70	A10/AP	100	VSS
11	VSS	41	VSS	71	BA0	101	SA2
12	DQ8	42	CB0	72	VDDQ	102	NC
13	DQ9	43	CB1	73	WE#	103	VSS
14	VSS	44	VSS	74	CAS#	104	DQS6#
15	DQS1#	45	DQS8#	75	VDDQ	105	DQS6
16	DQS1	46	DQS8	76	S1#	106	VSS
17	VSS	47	VSS	77	ODT1	107	DQ50
18	RESET#	48	CB2	78	VDDQ	108	DQ51
19	NC	49	CB3	79	VSS	109	VSS
20	VSS	50	VSS	80	DQ32	110	DQ56
21	DQ10	51	VDDQ	81	DQ33	111	DQ57
22	DQ11	52	CKE0	82	VSS	112	VSS
23	VSS	53	VDD	83	DQS4#	113	DQS7#
24	DQ16	54	NC/BA2	84	DQS4	114	DQS7
25	DQ17	55	ERR_OUT	85	VSS	115	VSS
26	VSS	56	VDDQ	86	DQ34	116	DQ58
27	DQS2#	57	A11	87	DQ35	117	DQ59
28	DQS2	58	A7	88	VSS	118	VSS
29	VSS	59	VDD	89	DQ40	119	SDA
30	DQ18	60	A5	90	DQ41	120	SCL

240-Pin RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
121	VSS	151	VSS	181	VDDQ	211	DM5/ DQS14
122	DQ4	152	DQ28	182	A3	212	NC/ DQS14#
123	DQ5	153	DQ29	183	A1	213	VSS
124	VSS	154	VSS	184	VDD	214	DQ46
125	DM0/ DQS9	155	DM3/ DQS12	185	CK0	215	DQ47
126	NC/ DQS9#	156	NC/ DQS12#	186	CK0#	216	VSS
127	VSS	157	VSS	187	VDD	217	DQ52
128	DQ6	158	DQ30	188	A0	218	DQ53
129	DQ7	159	DQ31	189	VDD	219	VSS
130	VSS	160	VSS	190	BA1	220	RFU
131	DQ12	161	CB4	191	VDDQ	221	RFU
132	DQ13	162	CB5	192	RAS#	222	VSS
133	VSS	163	VSS	193	S0#	223	DM6/ DQS15
134	DM1/ DQS10	164	DM8/ DQS17	194	VDDQ	224	NC/ DQS15#
135	NC/ DQS10#	165	NC/ DQS17#	195	ODT0	225	VSS
136	VSS	166	VSS	196	NC/A13	226	DQ54
137	RFU	167	CB6	197	VDD	227	DQ55
138	RFU	168	CB7	198	VSS	228	VSS
139	VSS	169	VSS	199	DQ36	229	DQ60
140	DQ14	170	VDDQ	200	DQ37	230	DQ61
141	DQ15	171	CKE1	201	VSS	231	VSS
142	VSS	172	VDD	202	DM4/ DQS13	232	DM7/ DQS16
143	DQ20	173	NC	203	NC/ DQS13#	233	NC/ DQS16#
144	DQ21	174	NC	204	VSS	234	VSS
145	VSS	175	VDDQ	205	DQ38	235	DQ62
146	DM2/ DQS11	176	A12	206	DQ39	236	DQ63
147	NC/ DQS11#	177	A9	207	VSS	237	VSS
148	VSS	178	VDD	208	DQ44	238	VDDSPD
149	DQ22	179	A8	209	DQ45	239	SA0
150	DQ23	180	A6	210	VSS	240	SA1

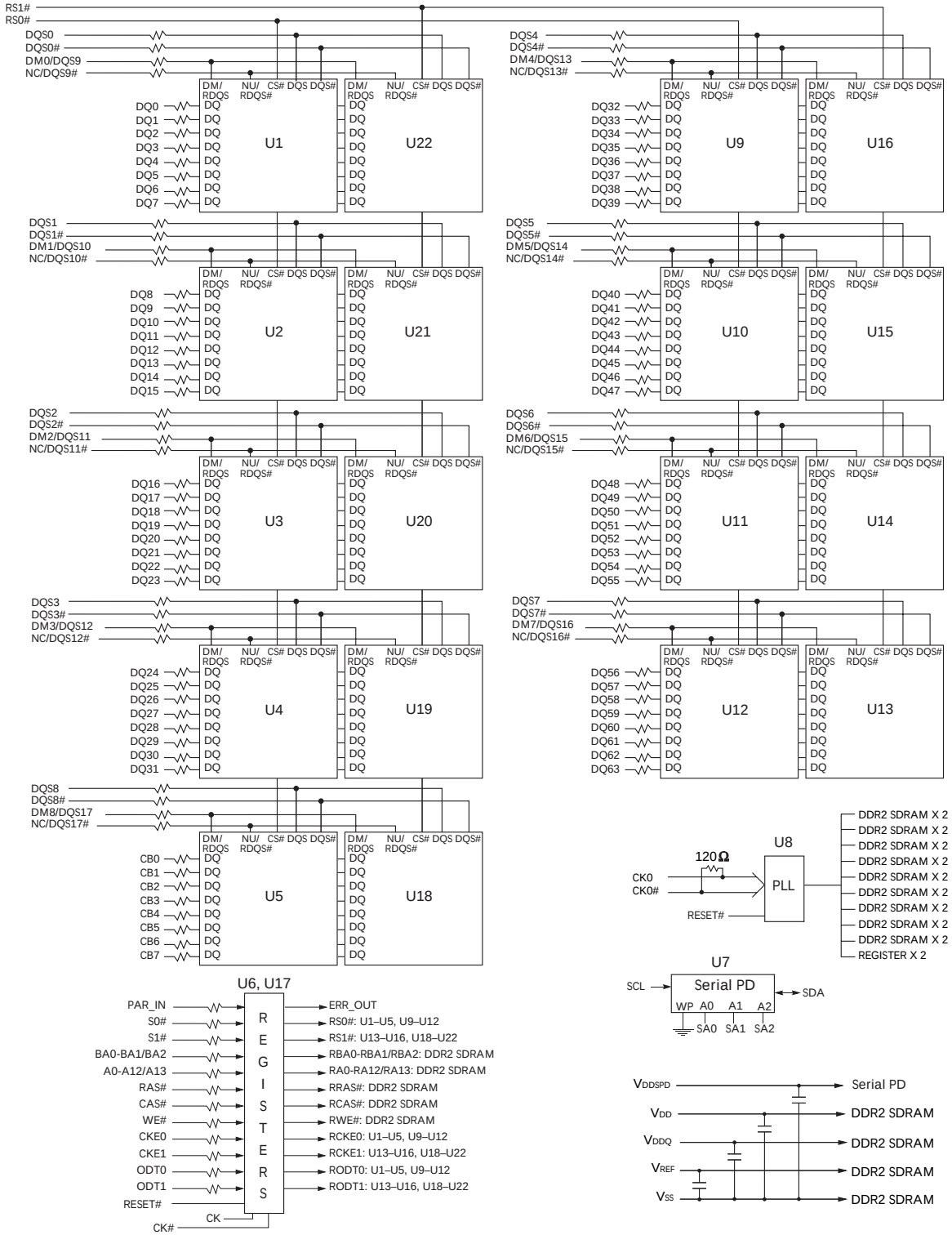
Notes: 1. Pin 196 is NC for 512MB or A13 for 1GB and 2GB.
2. Pin 54 is NC for 512MB and 1GB, or BA2 for 2GB.

Table 7: Pin Descriptions

Symbol	Type	Description
ODT0, ODT1	Input (SSTL18)	**On-die termination:** ODT1 (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to the following pins: DQ, DQS, DQS#, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
CK0, CK0#	Input (SSTL18)	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE0, CKE1	Input (SSTL18)	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.
S0#, S1#	Input (SSTL18)	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
RAS#, CAS#, WE#	Input (SSTL18)	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
BA0, BA1 (512MB, 1GB) BA0, BA1, BA2 (2GB)	Input (SSTL18)	**Bank address inputs:** BA0–BA1/BA2 define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA1/BA2 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command.
A0–A12 (512MB) A0–A13 (1GB, 2GB)	Input (SSTL18)	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA1/BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
PAR_IN	Input (SSTL18)	Parity bit for the address and control bus.
SCL	Input	**Serial clock for presence-detect:** SCL is used to synchronize the presence-detect data transfer to and from the module.
SA0–SA2	Input	**Presence-detect address inputs:** These pins are used to configure the presence-detect device.
RESET#	Input (LVCMOS)	Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQs are High-Z.
DQS0–DQS8, DQS0#–DQS17#	I/O (SSTL18)	**Data strobe:** Output with read data, input with write data for source-synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
DM0–DM8 (DQS9–DQS17)	I/O (SSTL18)	**Data input mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. If RDQS is disabled, DQS0–DQS17 become DM0–DM8 and DQS9#–DQS17# are not used.
DQ0–DQ63	I/O (SSTL18)	**Data input/output:** Bidirectional data bus.
CB0–CB7	I/O (SSTL18)	Check bits.
SDA	I/O	**Serial presence-detect data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
ERR_OUT	Output (open drain)	Parity error found on the address and control bus.
VDD	Supply	**Power supply:** 1.8V ±0.1V.
VDDQ	Supply	**DQ power supply:** 1.8V ±0.1V.
VREF	Supply	SSTL_18 reference voltage.
VSS	Supply	Ground.
VDDSPD	Supply	**Serial EEPROM positive power supply:** +1.7V to +3.6V.

Functional Block Diagram

Figure 2: Functional Block Diagram



Unless otherwise noted, resistor values are 22Ω per industry standard

General Description

The MT18HTF6472(P)D, MT18HTF12872(P)D, and MT18HTF25672(P)D DDR2 SDRAM modules are high-speed, CMOS, dynamic random-access 512MB, 1GB, and 2GB memory modules organized in a x72 configuration. These DDR2 SDRAM modules use internally configured quad-bank (256Mb, 512Mb) or eight-bank (1Gb) DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

PLL and Register Operation

DDR2 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR2 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The registers and PLL minimize system and clock loading. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 6 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 8: Absolute Maximum DC Ratings

Symbol	Parameter		Min	Max	Units
VDD	VDD supply voltage relative to VSS		–1.0	2.3	V
VDDQ	VDDQ supply voltage relative to VSS		–0.5	2.3	V
VDDL	VDDL supply voltage relative to VSS		–0.5	2.3	V
VIN, VOUT	Voltage on any pin relative to VSS		–0.5	2.3	V
T_{STG}	Storage temperature		–55	100	°C
T_{case}	DDR2 SDRAM device operating temperature (ambient)		0	85	°C
T_{OPR}	Operating temperature (ambient)		0	65	°C
I_I	Input leakage current; Any input 0V ≤ VIN ≤ VDD; VREF input 0V ≤ VIN ≤ 0.95V; (All other pins not under test = 0V)	Command/address, RAS#, CAS#, WE# S#, CKE	–5	5	µA
		CK, CK#	–10	10	
		DM	–10	10	
I_{OZ}	Output leakage current; 0V ≤ VOUT ≤ VDDQ; DQs and ODT are disabled	DQ, DQS, DQS#	–10	10	µA
I_{VREF}	VREF leakage current; VREF = valid VREF level		–36	36	µA

Capacitance

At DDR2 data rates, Micron encourages designers to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

IDD Specifications

Table 9: DDR2 IDD Specifications and Conditions – 512MB

Values shown for MT47H32M8 DDR2 SDRAM only and are computed from values specified in the 256Mb (32 Meg x 8) component data sheet

Parameter/Condition		Symbol	-667	-53E	-40E	Units
Operating one bank active-precharge current: tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0[a]	855	765	720	mA
Operating one bank active-read-precharge current: IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1[a]	945	855	810	mA
Precharge power-down current: All device banks idle; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P[b]	90	90	90	mA
Precharge quiet standby current: All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q[b]	720	630	450	mA
Precharge standby current: All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N[b]	720	630	540	mA
Active power-down current: All device banks open; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	IDD3P[b]	540	450	360	mA
	Slow PDN exit MR[12] = 1		108	108	108	mA
Active standby current: All device banks open; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N[b]	900	720	540	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W[a]	1,755	1,485	1,170	mA
Operating burst read current: All device banks open; Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R[a]	1,665	1,395	1,080	mA
Burst refresh current: tCK = tCK (IDD); REFRESH command at every tRFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5[b]	3,240	3,060	2,970	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6[b]	90	90	90	mA
Operating bank interleave read current: All device banks interleaving reads, IOUT= 0mA; BL = 4, CL = CL (IDD), AL = tRCD (IDD) -1 x tCK (IDD); tCK = tCK (IDD), tRC = tRC (IDD), tRRD = tRRD (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during DESELECTs; Data bus inputs are switching		IDD7[a]	2,295	2,205	2,115	mA

Notes:
1. a = Value calculated as one module rank in this operating condition; all other module ranks in IDD2P (CKE LOW) mode.
2. b = Value calculated reflects all module ranks in this operating condition.

Table 10: DDR2 IDD Specifications and Conditions – 1GB

Values shown for MT47H64M8 DDR2 SDRAM only and are computed from values specified in the 512Mb (64 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E	-667	-53E	-40E	Units
Operating one bank active-precharge current: tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0[a]	963	873	783	783	mA
Operating one bank active-read-precharge current: IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1[a]	1,098	1,008	918	873	mA
Precharge power-down current: All device banks idle; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P[b]	126	126	126	126	mA
Precharge quiet standby current: All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q[b]	900	810	720	630	mA
Precharge standby current: All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N[b]	990	900	810	720	mA
Active power-down current: All device banks open; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	IDD3P[b]	720	630	540	450	mA
	Slow PDN exit MR[12] = 1		216	216	216	216	mA
Active standby current: All device banks open; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N[b]	1,260	1,170	990	810	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W[a]	1,818	1,593	1,323	1,098	mA
Operating burst read current: All device banks open; Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R[a]	1,908	1,683	1,368	1,098	mA
Burst refresh current: tCK = tCK (IDD); REFRESH command at every tRFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5[b]	4,140	3,240	3,060	2,970	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6[b]	126	126	126	126	mA
Operating bank interleave read current: All device banks interleaving reads, IOUT= 0mA; BL = 4, CL = CL (IDD), AL = tRCD (IDD) -1 x tCK (IDD); tCK = tCK (IDD), tRC = tRC (IDD), tRRD = tRRD (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during DESELECTs; Data bus inputs are switching		IDD7[a]	2,763	2,223	2,088	2,043	mA

Notes:
1. a = Value calculated as one module rank in this operating condition; all other module ranks in IDD2P (CKE LOW) mode.
2. b = Value calculated reflects all module ranks in this operating condition.

Table 11: DDR2 IDD Specifications and Conditions – 2GB

Values shown for MT47H128M8 DDR2 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E	-667	-53E	-40E	Units
Operating one bank active-precharge current: tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0[a]	963	873	783	693	mA
Operating one bank active-read-precharge current: IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS MIN (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1[a]	1,053	963	918	783	mA
Precharge power-down current: All device banks idle; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P[b]	126	126	126	126	mA
Precharge quiet standby current: All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q[b]	1,170	990	738	630	mA
Precharge standby current: All device banks idle; tCK = tCK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N[b]	1,260	1,080	810	720	mA
Active power-down current: All device banks open; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	IDD3P[b]	810	720	630	630	mA
	Slow PDN exit MR[12] = 1		252	252	252	252	mA
Active standby current: All device banks open; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N[b]	1,350	1,260	990	810	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W[a]	1,728	1,503	1,233	1,053	mA
Operating burst read current; All device banks open; Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS MAX (IDD), tRP = tRP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R[a]	1,773	1,503	1,368	1,053	mA
Burst refresh current: tCK = tCK (IDD); REFRESH command at every tRFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5[b]	5,040	4,680	4,500	3,960	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6[b]	126	126	126	126	mA
Operating bank interleave read current: All device banks interleaving reads, IOUT= 0mA; BL = 4, CL = CL (IDD), AL = tRCD (IDD) -1 x tCK (IDD); tCK = tCK (IDD), tRC = tRC (IDD), tRRD = tRRD (IDD), tRCD = tRCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during DESELECTs; Data bus inputs are switching		IDD7[a]	3,078	2,763	2,673	2,403	mA

Notes:
1. a = Value calculated as one module rank in this operating condition; all other module ranks in IDD2P (CKE LOW) mode.
2. b = Value calculated reflects all module ranks in this operating condition.

AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades as shown in the following table:

Table 12: Module and Component Speed Grade Table

Module Speed Grade	Component Speed Grade
-80E	-25E
-800	-25
-667	-3
-53E	-37E
-40E	-5E

Register and PLL Specifications

Table 13: Register (SSTU32866 devices or equivalent JESD82-16)

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	$V_{IH(DC)}$	Address, control, command	SSTL_18	$V_{REF(DC)}$ +125	V_{DDQ} + 250	mV
DC low-level input voltage	$V_{IL(DC)}$	Address, control, command	SSTL_18	0	$V_{REF(DC)}$ - 125	mV
AC high-level input voltage	$V_{IH(AC)}$	Address, control, command	SSTL_18	$V_{REF(DC)}$ + 250	V_{DD}	mV
AC low-level input voltage	$V_{IL(AC)}$	Address, control, command	SSTL_18	0	$V_{REF(DC)}$ - 250	mV
Output high voltage	V_{OH}	Parity output	LVCMOS	1.2	–	mV
Output low voltage	V_{OL}	Parity output	LVCMOS	–	0.5	mV
Input current	I_I	All pins	V_I = V_{DDQ} or V_{SSQ}	–5	5	µA
Static standby	I_{DD}	All pins	RESET# = V_{SSQ} (I/O = 0)	–	100	µA
Static operating	I_{DD}	All pins	RESET# = V_{SSQ}; V_I = $V_{IH(AC)}$ or $V_{IL(DC)}$ I/O = 0	–	40mA	µA
Dynamic operating – clock tree	I_{DDD}	n/a	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, I0 = 0; CK and CK# switching 50% duty cycle	–	Varies by manufacturer	µA
Dynamic operating (per each input)	I_{DDD}	n/a	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, I0 = 0; CK and CK# switching 50% duty cycle; One data input switching at ^{t}CK/2, 50% duty cycle	–	Varies by manufacturer	µA
Input capacitance (per device, per pin)	C_I	All inputs except RESET#	V_I = V_{REF} ±250mV; V_{DDQ} = 1.8V	2.5	3.5	pF
Input capacitance (per device, per pin)		RESET#	V_I = V_{DDQ} or V_{SSQ}	–	Varies by manufacturer	pF

Notes:
1. Timing and switching specifications for the register listed above are critical for proper operation of the DDR2 SDRAM registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC Standard JESD82.
2. This parameter is not necessarily production tested.
3. Data inputs must be low a minimum time of ^{t}act (MAX), after RESET# is taken HIGH.
4. Data and clock inputs must be held at valid levels (not floating) a minimum time of ^{t}inact (MAX), after RESET# is taken LOW.
5. Total I_{DD} = I_{DDQ} = I_{ADD} = F_{CK} × C_{PD} × V_{DDQ}, solving for C_{PD} = (I_{DDQ} + I_{ADD})/(F_{CK} × V_{DDQ}) where F_{CK} is the input frequency, V_{DDQ} is the power supply and C_{PD} is the power dissipation capacitance.

PLL

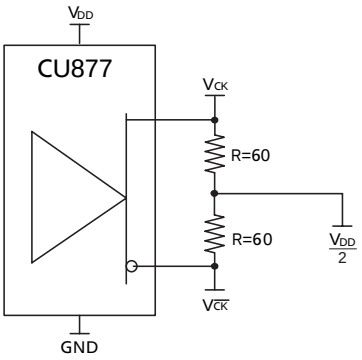
Table 14: PLL (CU877 device or equivalent JESD82-8.01)

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	V_{IH}	RESET#	LVCMOS	0.65 × V_{DD}	–	mV
DC low-level input voltage	V_{IL}	RESET#	LVCMOS	–	0.35 × V_{DD}	mV
Input voltage (limits)	V_{IN}	RESET#, CK, CK#		–0.3	$V_{DD}Q$ + 0.3	mV
DC high-level input voltage	V_{IH}	CK, CK#	Differential input	0.65 × V_{DD}	–	mV
DC low-level input voltage	V_{IL}	CK, CK#	Differential input	–	0.35 × V_{DD}	mV
Input differential-pair cross voltage	V_{IX}	CK, CK#	Differential input	($V_{DD}Q$/2) - 0.15	($V_{DD}Q$/2) + 0.15	V
Input differential voltage	$V_{ID(DC)}$	CK, CK#	Differential input	0.3	$V_{DD}Q$ + 0.4	V
Input differential voltage	$V_{ID(AC)}$	CK, CK#	Differential input	0.6	$V_{DD}Q$ + 0.4	V
Input current	I_I	RESET#	V_I = $V_{DD}Q$ or $V_{SS}Q$	–10	10	µA
		CK, CK#	V_I = $V_{DD}Q$ or $V_{SS}Q$	–250	250	µA
Output disabled current	I_{ODL}		RESET# = $V_{SS}Q$; V_I = $V_{IH(AC)}$ or $V_{IL(DC)}$	100	–	µA
Static supply current	I_{DDLD}		CK = CK# = LOW	–	500	µA
Dynamic supply	I_{DD}	n/a	CK, CK# = 270 MHz, all outputs open (not connected to PCB)	–	300	mA
Input capacitance	C_{IN}	Each input	V_I = $V_{DD}Q$ or $V_{SS}Q$	2	3	pF

Table 15: PLL Clock Driver Timing Requirements and Switching Characteristics

Parameter	Symbol	0°C ≤ T_{OPR} ≤ +55°C V_{DD} = +1.8V ±0.1V		Units
		Min	Max	
Stabilization time	^{t}L	–	15	µs
Input clock slew rate	$^{t}LS_{I}$	1.0	4	V/ns
SSC modulation frequency		30	33	kHZ
SSC clock input frequency deviation		0.0	–0.50	%
PLL loop bandwidth (-3dB from unity gain)		2.0	–	MHz

Notes:
1. PLL timing and switching specifications are critical for proper operation of the DDR2 DIMM. This is a subset of parameters for the specific PLL used. Detailed PLL information is available in JEDEC Standard JESD82.
2. Static phase offset does not include jitter.
3. Period jitter and half-period jitter specifications are separate specifications that must be met independently of each other.
4. Design target is 60ps, unless it is not achievable.
5. V_{OX} specified at the DRAM clock input or the test load.
6. The output slew rate is determined from the IBIS model:



Serial Presence-Detect

Table 16: Serial Presence-Detect EEPROM DC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	1.7	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.10	3	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3	µA
Standby current	I_{SB}	1.6	4	µA
Power supply current, READ: SCL clock frequency = 100 KHz	ICC_R	0.4	1	mA
Power supply current, WRITE: SCL clock frequency = 100 KHz	ICC_W	2	3	mA

Table 17: Serial Presence-Detect EEPROM AC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^tAA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^tBUF	1.3	–	µs	
Data-out hold time	^tDH	200	–	ns	
SDA and SCL fall time	^tF	–	300	ns	2
Data-in hold time	$^tHD:DAT$	0	–	µs	
Start condition hold time	$^tHD:STA$	0.6	–	µs	
Clock HIGH period	^tHIGH	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^tI	–	50	ns	
Clock LOW period	^tLOW	1.3	–	µs	
SDA and SCL rise time	^tR	–	0.3	µs	2
SCL clock frequency	^fSCL	–	400	KHz	
Data-in setup time	$^tSU:DAT$	100	–	ns	
Start condition setup time	$^tSU:STA$	0.6	–	µs	3
Stop condition setup time	$^tSU:STO$	0.6	–	µs	
WRITE cycle time	^tWRC	–	10	ms	4

Notes:
1. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a reSTART condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 18: Serial Presence-Detect Matrix
"1"/"0": serial data, "driven to HIGH"/"driven to LOW"

Byte	Description	Entry (Version)	MT18HTF6472(P)D	MT18HTF12872(P)D	MT18HTF25672(P)D
0	Number of SPD bytes used by Micron	128	80	80	80
1	Total number of bytes in SPD device	256	08	08	08
2	Fundamental memory type	DDR2 SDRAM	08	08	08
3	Number of row addresses on SDRAM	13, 14	0D	0E	0E
4	Number of column addresses on SDRAM	10	0A	0A	0A
5	DIMM height and module ranks	30mm, dual rank	61	61	61
6	Module data width	72	48	48	48
7	Reserved	0	00	00	00
8	Module voltage interface levels	SSTL 1.8V	05	05	05
9	SDRAM cycle time, ^{t}CK (CL = MAX value, see byte 18)	-80E -800 -667 -53E -40E	– – 30 3D 50	25 25 30 3D 50	25 25 30 3D 50
10	SDRAM access from clock, ^{t}AC (CL = MAX value, see byte 18)	-800/-80E -667 -53E -40E	– 45 50 60	40 45 50 60	40 45 50 60
11	Module configuration type	ECC ECC and parity (P)	02 06	02 06	02 06
12	Refresh rate/type	7.81µs/SELF	82	82	82
13	SDRAM device width (primary SDRAM)	8	08	08	08
14	Error-checking SDRAM data width	8	08	08	08
15	Reserved		00	00	00
16	Burst lengths supported	4, 8	0C	0C	0C
17	Number of banks on SDRAM device	4 or 8	04	04	08
18	CAS latencies supported	-80E (5, 4) -800 (6, 5) -667 (5, 4, 3) -53E/-40E (4, 3)	– – 38 18	30 60 38 18	30 60 38 18
19	Module thickness		01	01	01
20	DDR2 DIMM type	Registered DIMM	01	01	01
21	SDRAM module attributes	1 PLL, 2 Reg	05	05	05
22	SDRAM device attributes: weak driver (01), or weak driver and 50Ω ODT (03)	-800/-80E/-667 -53E/-40E	– /03 01	03 01	03 01

Table 18: Serial Presence-Detect Matrix (continued)
"1"/"0": serial data, "driven to HIGH"/"driven to LOW"

Byte	Description	Entry (Version)	MT18HTF6472(P)D	MT18HTF12872(P)D	MT18HTF25672(P)D
23	SDRAM cycle time, ^{t}CK, MAX CL - 1	-80E/-667 -800 -53E/-40E	– /3D – 50	3D 30 50	3D 30 50
24	SDRAM access from CK, ^{t}AC, MAX CL - 1	-800/-80E -667 -53E -40E	– 45 50 60	40 45 50 60	40 45 50 60
25	SDRAM cycle time, ^{t}CK, MAX CL - 2	-800/-80E(N/S) -667 -53E/-40E(N/S)	– 50 00	00 50 00	00 50 00
26	SDRAM access from CK, ^{t}AC, MAX CL - 2	-800/-80E(N/S) -667 -53E/-40E(N/S)	– 45 00	00 45 00	00 45 00
27	MIN row precharge time, ^{t}RP	-80E -800/-667/ -53E/-40E	– – /3C 3C	32 3C 3C	32 3C 3C
28	MIN row active to row active, ^{t}RRD		1E	1E	1E
29	MIN RAS# to CAS# delay, ^{t}RCD	-80E -800/-667/ -53E/-40E	– – /3C 3C	32 3C 3C	32 3C 3C
30	MIN RAS# pulse width, ^{t}RAS	-800-80E/ -667/-53E -40E	– /2D 2D 28	2D 2D 28	2D 2D 28
31	Module rank density	256MB, 512MB, 1GB	40	80	01
32	Address and command setup time, $^{t}IS_{b}$	-800/-80E -667 -53E -40E	– 20 25 35	17 20 25 35	17 20 25 35
33	Address and command hold time, $^{t}IH_{b}$	-800/-80E -667 -53E -40E	– 27 37 47	25 27 37 47	25 27 37 47
34	Data/data mask input setup time, $^{t}DS_{b}$	-800/-80E -667/-53E -40E	– 10 15	05 10 15	05 10 15
35	Data/data mask input hold time, $^{t}DH_{b}$	-800/-80E -667 -53E -40E	– 17 22 27	12 17 22 27	12 17 22 27
36	Write recovery time, ^{t}WR		3C	3C	3C
37	Write to read CMD delay, ^{t}WTR	-80E/-667/-53E -800/-40E	– /1E – /28	1E 28	1E 28
38	Read to precharge CMD delay, ^{t}RTP		1E	1E	1E
39	Memory analysis probe		00	00	00
40	Extension for bytes 41 and 42	-80E -800/-667 -53E/-40E	– 00 00	30 00 00	36 06 06

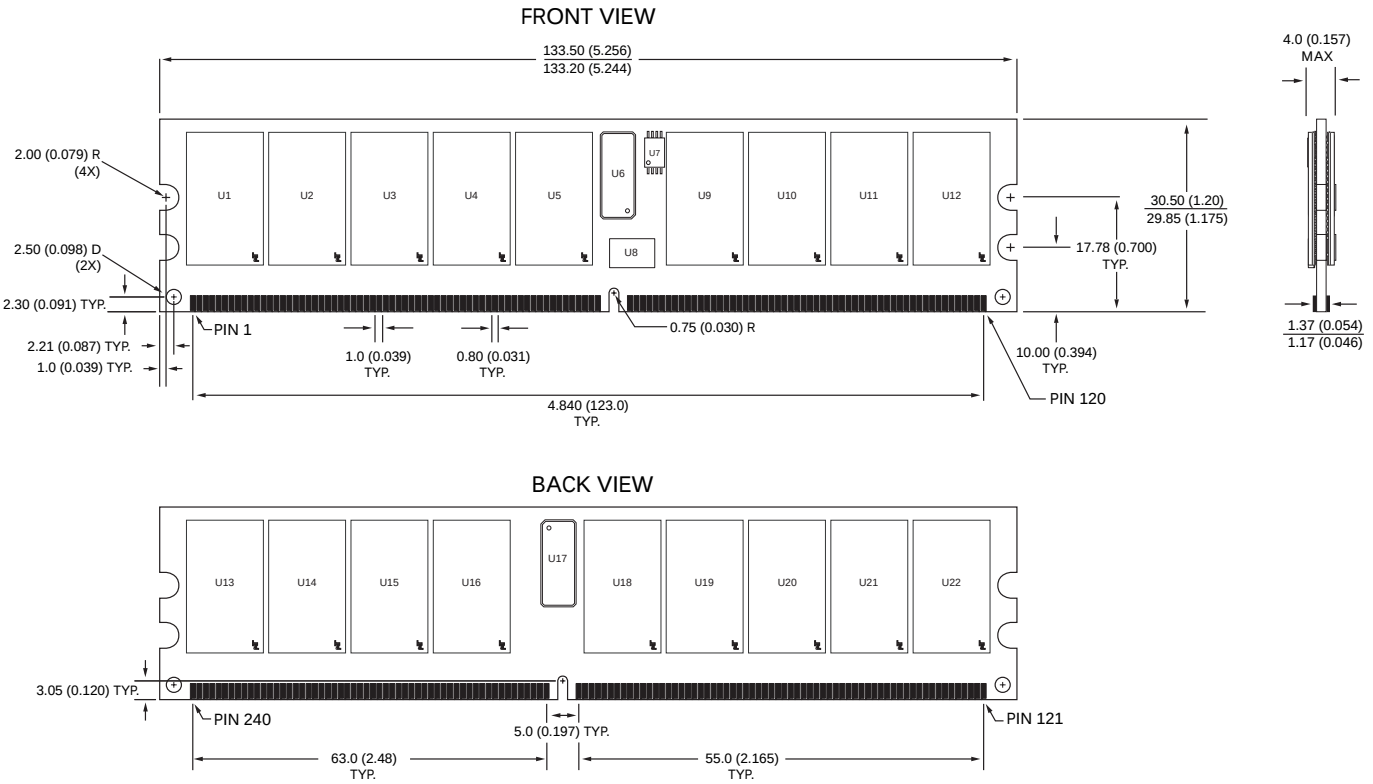
Table 18: Serial Presence-Detect Matrix (continued)
"1"/"0": serial data, "driven to HIGH"/"driven to LOW"

Byte	Description	Entry (Version)	MT18HTF6472(P)D	MT18HTF12872(P)D	MT18HTF25672(P)D
41	MIN active auto refresh time, ^{t}RC (see note 1)	-80E -800/-667/-53E -40E	– 3C 37	39 3C 37	39 3C 37
42	MIN auto refresh to active/ auto refresh command period, ^{t}RFC		4B	69	7F
43	SDRAM device MAX cycle time, ^{t}CKMAX		80	80	80
44	SDRAM device MAX DQS–DQ skew time, ^{t}DQSQ	-800/-80E -667 -53E -40E	– 18 1E 23	14 18 1E 23	14 18 1E 23
45	SDRAM device MAX read data hold skew factor, ^{t}QHS	-800/-80E -667 -53E -40E	– 22 28 2D	1E 22 28 2D	1E 22 28 2D
46	PLL relock time	15µs	0F	0F	0F
47–61	Optional features, not supported		00	00	00
62	SPD revision	Release 1.2	12	12	12
63	Checksum for bytes 0–62 ECC/ECC and parity	-80E -800 -667 -53E -40E	– – 12/16 BD/C1 24/28	B5/B9 C9/CD 71/75 1C/20 83/89	56/5A 6A/6E 12/16 BD/C1 24/28
64	Manufacturer's JEDEC ID code	MICRON	2C	2C	2C
65-71	Manufacturer's JEDEC ID code	(continued)	FF	FF	FF
72	Manufacturing location	01–12	01–0C	01–0C	01–0C
73-90	Module part number (ASCII)		Variable data	Variable data	Variable data
91	PCB identification code	1–9	01–09	01–09	01–09
92	Identification code (continued)	0	00	00	00
93	Year of manufacture in BCD		Variable data	Variable data	Variable data
94	Week of manufacture in BCD		Variable data	Variable data	Variable data
95–98	Module serial number		Variable data	Variable data	Variable data
99–127	Manufacturer-specific data (RSVD)		FF	FF	FF

Notes: 1. The ^{t}RC SPD values shown are JEDEC DDR2 device specification values. The actual Micron DDR2 device specification is ^{t}RC = 55ns for all speed grades.

Module Dimensions

Figure 3: 240-Pin DDR2 DIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for complete design dimensions.

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