

FAN8026G3

5-CH Motor Driver

Features

- 5-CH Balanced transformerless (BTL) driver
- Operating supply voltage : 4.5 V ~ 13.2V
- Built-in thermal shut down circuit (TSD)
- Built-in channel mute circuit
- Built-in 1-OP AMP

Description

The FAN8026G3 is a monolithic integrated circuit suitable for a 5-CH motor driver which drives a tracking actuator, a focus actuator, a sled motor, a spindle motor, and a tray motor of the CDP/CAR-CD/DVDP systems.

28-SSOPH-375SG3



Typical application

- Compact disk player
- Video compact disk player
- Car compact disk player
- Digital video disk player

Ordering information

Device	Package	Operating temp
FAN8026G3	28-SSOPH-375-SG2	-35°C ~ +85°C
FAN8026G3X ^{note1}	28-SSOPH-375-SG2	-35°C ~ +85°C
FAN8026G3_NL ^{note2}	28-SSOPH-375-SG2	-35°C ~ +85°C
FAN8026G3X_NL	28-SSOPH-375-SG2	-35°C ~ +85°C

Notes:

1. X : Tape&Reel
2. NL : Lead free

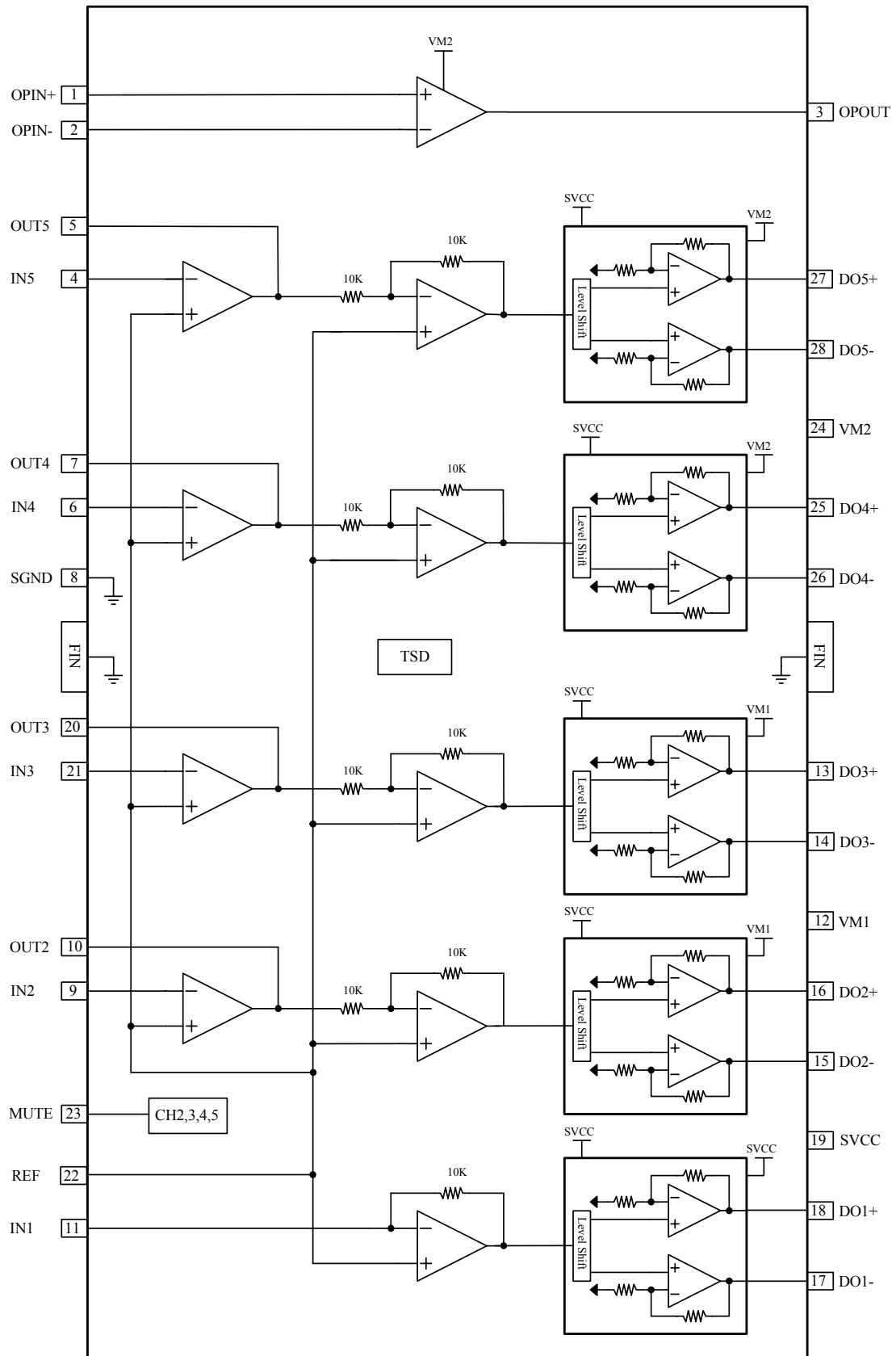
Pin Assignments



Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	OPIN+	I	OP-AMP Input(+)
2	OPIN-	I	OP-AMP Input(-)
3	OPOUT	O	OP-AMP Output
4	IN5	I	CH5 Op-amp Input(-)
5	OUT5	O	CH5 Op-amp Output
6	IN4	I	CH4 Op-amp Input(-)
7	OUT4	O	CH4 Op-amp Output
8	GND	-	Ground
9	IN2	I	CH2 Op-amp Input(-)
10	OUT2	O	CH2 Op-amp Output
11	IN1	I	CH1 Input
12	VM1	-	Power Supply Voltage(For CH2,CH3)
13	DO3+	O	CH3 Drive Output(+)
14	DO3-	O	CH3 Drive Output(-)
15	DO2-	O	CH2 Drive Output(-)
16	DO2+	O	CH2 Drive Output(+)
17	DO1-	O	CH1 Drive Output(-)
18	DO1+	O	CH1 Drive Output(+)
19	SVCC	-	Power Supply Voltage(For Signal,CH1)
20	OUT3	O	CH3 Op-amp Output
21	IN3	I	CH3 Op-amp Input(-)
22	REF	I	CH1,2,3,4,5 Input Reference
23	MUTE	I	MUTE(CH2,3,4,5)
24	VM2	-	Power Supply Voltage(For CH4,CH5,Normal Op-amp)
25	DO4+	O	CH4 Drive Output(+)
26	DO4-	O	CH4 Drive Output(-)
27	DO5+	O	CH5 Drive Output(+)
28	DO5-	O	CH5 Drive Output(-)

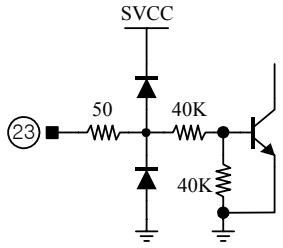
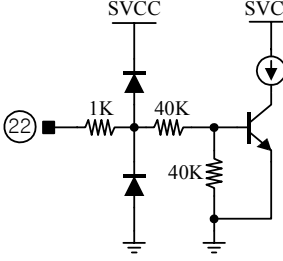
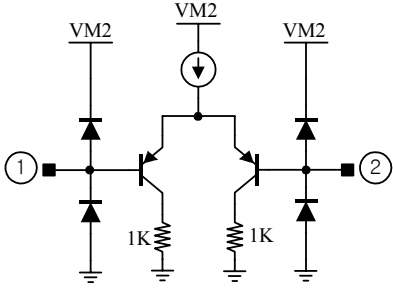
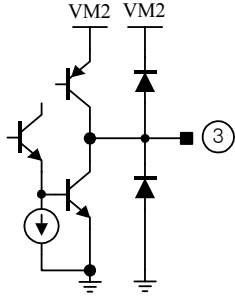
Internal Block Diagram



Equivalent Circuits

<p style="text-align: center;">BTL CH1 Input</p>	<p style="text-align: center;">BTL CH2,3,4,5 Op-amp Input</p>
<p style="text-align: center;">BTL CH2,3,4,5 Op-amp Output</p>	<p style="text-align: center;">BTL CH1 Driver Output</p>
<p style="text-align: center;">BTL CH2,3 Driver Output</p>	<p style="text-align: center;">BTL CH4,5 Driver Output</p>

Equivalent Circuits (Continued)

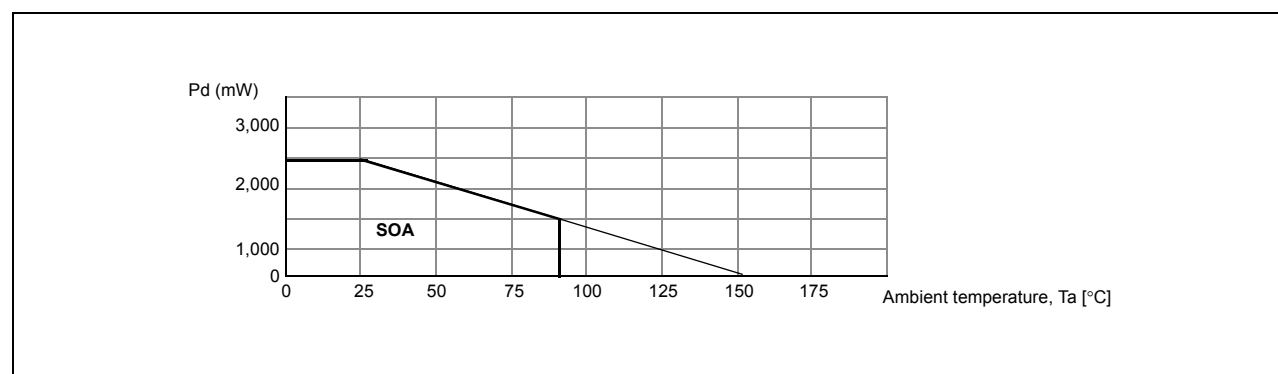
Mute	REF
	
Op-amp Input	Op-amp Output
	

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Value	Unit
Maximum supply voltage	SVCC	15	V
	VM1	15	V
	VM2	15	V
Power dissipation	P _D	2.5 ^{note1,2,3}	W
Operating temperature	T _{OPR}	-35 ~ +85	°C
Storage temperature	T _{STG}	-55 ~ +150	°C

Notes:

1. When mounted on glass epoxy PCB (76 × 114 × 1.6mm)
2. Power dissipation is reduced at the rate of -20mW/°C for TA≥25°C.
3. Do not exceed Pd and SOA(Safe Operating Area).



Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage1	SVCC	4.5	-	13.2	V
Supply voltage2	VM1	4.5	-	SVCC	V
Supply voltage3	VM2	4.5	-	SVCC	V

Electrical Characteristics

(Unless otherwise specified, Ta=25°C, SVCC=8V, VM1=5V, VM2=5V, Vref=1.65V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Quiescent current 1*note1	ICC1	MUTE Off	-	21	-	mA
Quiescent current 2*note1	ICC2	MUTE On	-	12	-	mA
MUTE on voltage	Vmon	Pin23=Variation	2.0	-	-	V
MUTE off voltage	Vmoff	Pin23=Variation	-	-	0.5	V
Reference MUTE on voltage	Vrmon	Pin22=Variation	-	-	0.4	V
Reference MUTE off voltage	Vrmoff	Pin22=Variation	1.0	-	-	V
REF Input voltage range	Vrefin1	-	1.0	-	3.3	V
CH1 LOADING DRIVER CIRCUIT (RL=12Ω)						
Output offset voltage1	VOF1	VIN=1.65V	-50	-	+50	mV
Maximum output voltage1	Vom1	-	6	6.5	-	V
Close-loop voltage gain1	Gvf1	VIN=100mVpp, f=1kHz	10	12	14	dB
CH2,3 BTL DRIVER CIRCUIT (RL=8Ω)						
Output offset voltage2,3,4,5	VOF2,3,4,5	VIN=1.65V	-50	-	+50	mV
Maximum output voltage2,3,4,5	Vom2,3,4,5	-	3.6	4.0	-	V
Close-loop voltage gain2,3,5	Gvf2,3,5	VIN=100mVpp, f=1kHz	10.5	12.5	14.5	dB
Close-loop voltage gain4	Gvf4	VIN=100mVpp, f=1kHz	11.5	13.5	15.5	dB
INPUT OP-AMP CIRCUIT						
Input offset voltage1	VOF1	-	-10	-	+10	mV
Input bias current1	IB1	-	-	-	300	nA
High level output voltage1	VOH1	SVCC=8V	7	-	-	V
Low level output voltage1	VOL1	-	-	-	0.5	V
Output sink current1	ISINK1	-	1	-	-	mA
Output source current1	ISOU1	-	0.5	-	-	mA
Common mode input range1*note1	Vicm1	-	-0.3	-	7.0	V
Open loop voltage gain1*note1	GVO1	f=1kHz, VIN= -75dB	-	75	-	dB
Ripple rejection ratio1*note1	RR1	f=120Hz, VIN= -20dB	-	65	-	dB
Slew rate1*note1	SR1	f=120Hz, 2Vp-p	-	1	-	V/us

Note:

1. Guaranteed field. (No EDS/ Final test .)

Electrical characteristics (Continued)

(Unless otherwise specified, Ta=25°C, SVCC=8V, VM1=5V, VM2=5V, Vref=1.65V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
NORMAL OP-AMP CIRCUIT						
Input offset voltage	VOF2	-	-10	-	+10	mV
Input bias current	IB2	-	-	-	300	nA
High level output voltage	VOH2	VM2=5V	4.5	-	-	V
Low level output voltage	VOL2	-	-	-	0.5	V
Output sink current	ISINK2	-	1	-	-	mA
Output source current	ISOU2	-	0.5	-	-	mA
Common mode input range ^{1*note1}	Vicm1	-	-0.3	-	4.0	V
Open loop voltage gain ^{*note1}	GVO2	f=1kHz, VIN= -75dB	-	75	-	dB
Ripple rejection ratio ^{*note1}	RR2	f=120Hz, VIN= -20dB	-	65	-	dB
Slew rate ^{*note1}	SR2	f=120Hz, 2Vp-p	-	1	-	V/us

Note:

1.Guaranteed field. (No EDS/ Final test .)

Application information

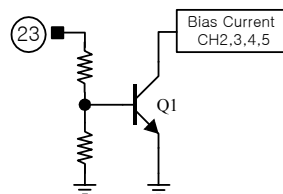
1. MUTE Function

When the mute pin is low(GND), the TR Q1 is turned on and the bias circuit is enabled. On the other hand, when the mute pin is high, the TR Q1 is turned off and the bias circuit is disabled.

It will make all the circuit blocks except CH1 off, so low power quiescent state can be established.

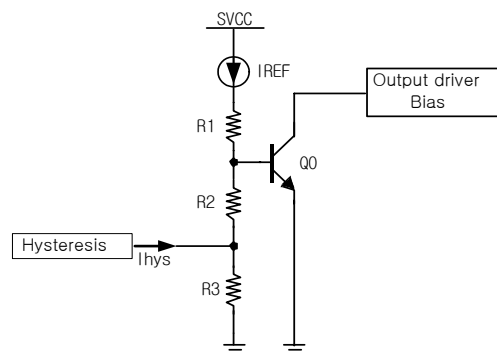
- Truth table is as follows

Pin 23	FAN8026
High	Mute-On
Low	Mute-Off



2. TSD Function

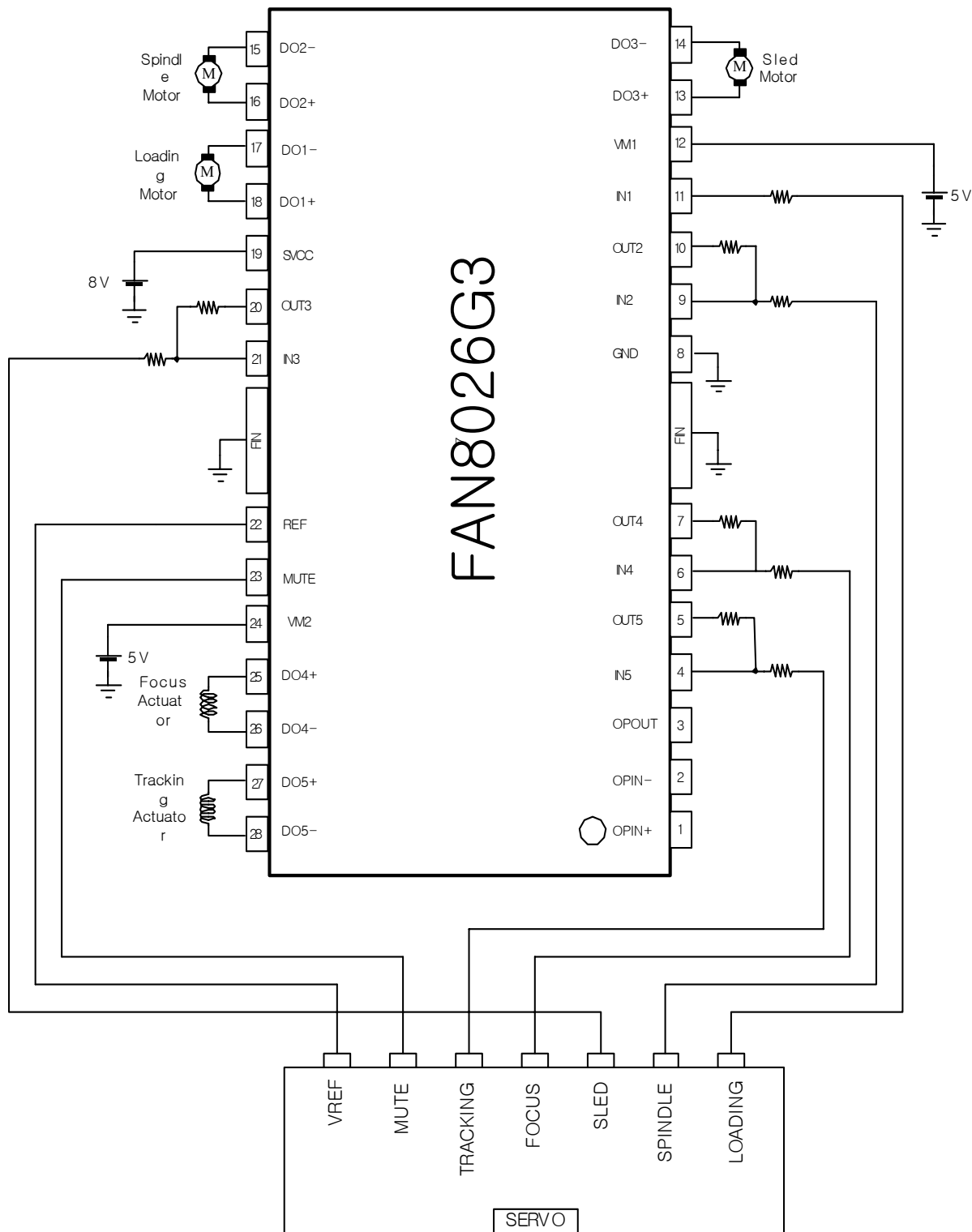
- When the chip temperature reaches to 175°C by abnormal condition, the TSD circuit is activated
- This makes the bias current of the output drivers shut down, and all the output drivers are on cut-off state. Therefore the chip temperature begins to decrease.
- When the chip temperature falls to 155°C, the TSD circuit is deactivated and the output drivers start to operate normally.



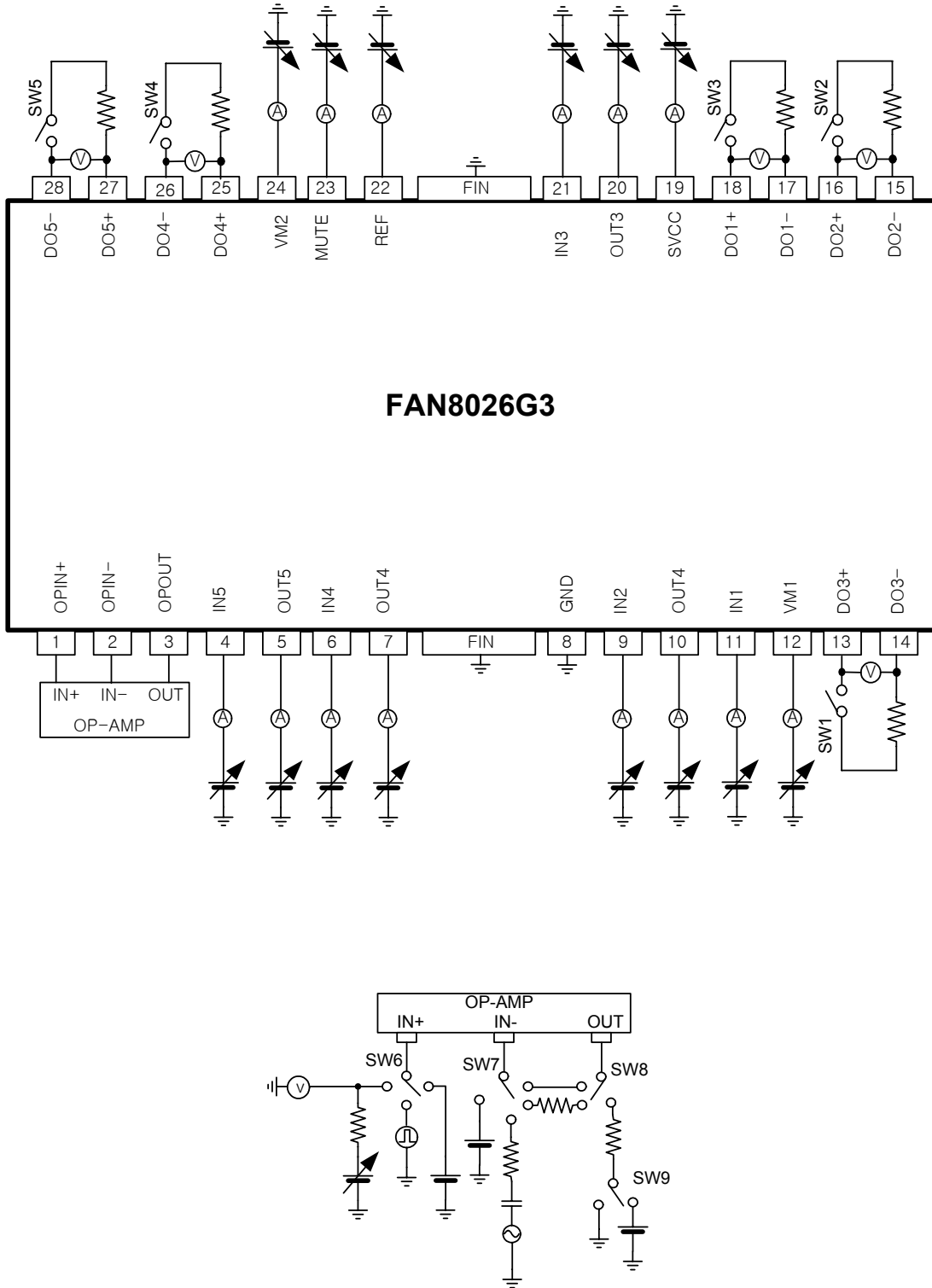
3. Notice

- If REF(pin23) is lower than 0.7V, BTL output is off.
- Under voltage protection function. (If SVcc is lower than 3.8V, Chip is disable. Hysteresis is 0.2V)
- Mute on BTL output voltage is as followed:
 - Mute on BTL output(CH2,3,4,5) = $V_M / 2$
 - Mute on BTL output CH1 = $((PV_{cc2} - 0.6) / 2)$
- Each output to output and output to GND short should be kept away.

Typical Application Circuit

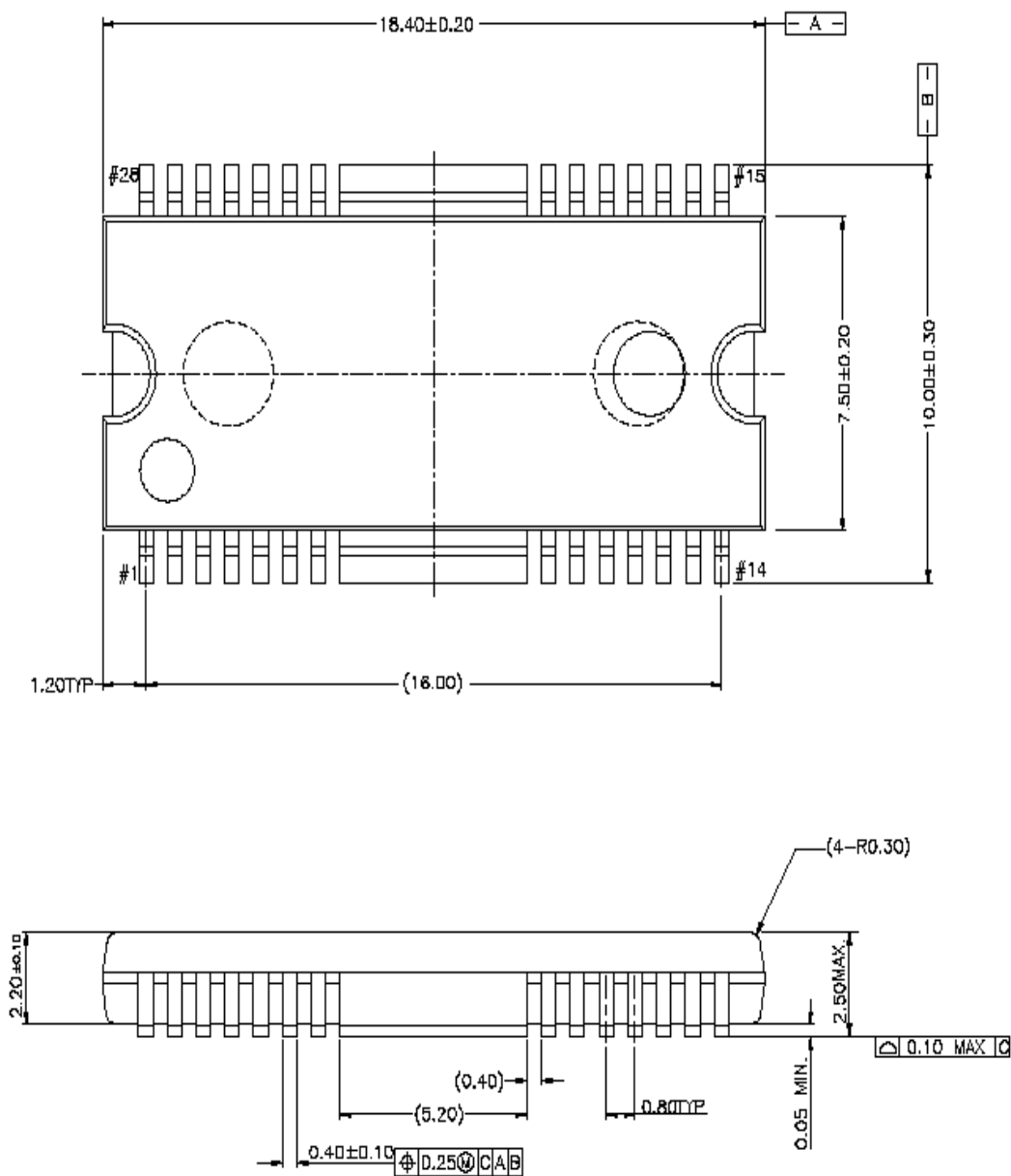


Test Circuits



Package Dimension

28-SSOPH-375-SG2



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