

0.4 A Dual H-Bridge Motor Driver IC

The 17C724 is a compact monolithic dual channel H-Bridge power IC, ideal for portable electronic applications containing bipolar stepper motors or brush DC motors such as those used in camera lenses and shutters.

The 17C724 can operate efficiently with supply voltages from 2.7 V to 5.5 V and can provide continuous motor drive currents of 0.4 A with low $R_{DS(ON)}$ of 1.0 Ω . It is easily interfaced to low-cost MCUs via parallel 3.0 V- or 5.0 V-compatible logic and has built-in shoot-through current protection circuit and undervoltage detector to avoid malfunction.

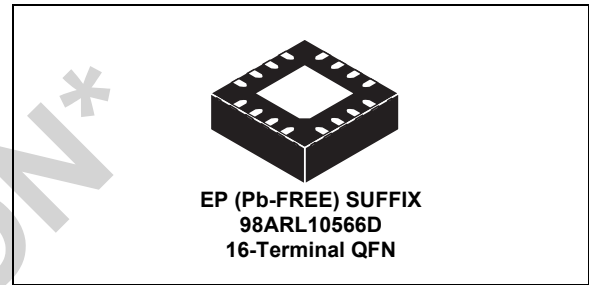
The 17C724 has four output control modes: Forward, Reverse, Brake, and Tri-State (High Impedance). The H-bridge outputs are designed to be independently PWM'ed at up to 200 kHz for speed/torque and current control.

Features

- Manufactured in SMOS7 Process Technology
- Built-In 2-Channel H-Bridge Driver
- Provides 4 Driving Modes (Forward, Reverse, Break, High Impedance)
- Direct Interface to MCU
- Low ON-Resistance, $R_{DS(ON)} = 1.0 \Omega$ (Typical)
- Dual Channel Parallel Drive, $R_{DS(ON)} = 0.5 \Omega$ (Typical)
- Output Current Driver (IDR) is 400 mA (Continuous)
- Low Power Consumption
- Built-In Shoot-Through Current Prevention Circuit
- Built-In Low-Voltage Shutdown Circuit
- PWM Control Frequency 200 kHz (Max)
- Very Compact Size, Comes in 16-Terminal QFN Package (3x3 mm Terminal Pitch: 0.5 mm)
- Pb-Free Packaging Designated by Suffix Code EP

17C724

MOTOR DRIVER



ORDERING INFORMATION		
Device	Temperature Range (T _A)	Package
MPC17C724EP/R2	-20°C to 85°C	16 QFN

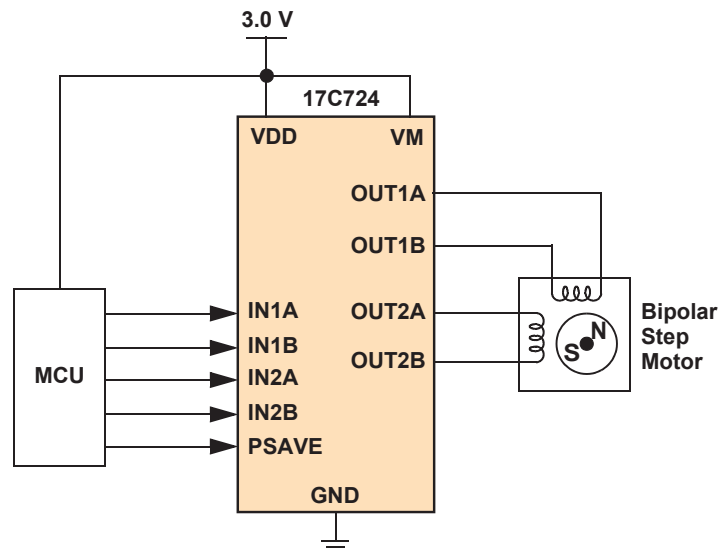


Figure 1. 17C724 Simplified Application Diagram

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INTERNAL BLOCK DIAGRAM

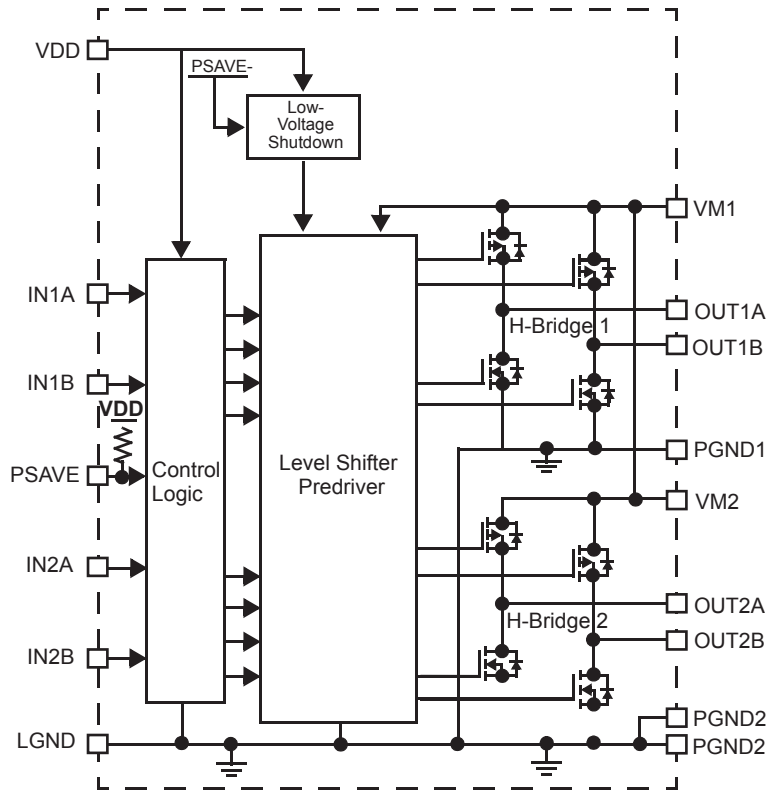


Figure 2. 17C724 Simplified Internal Block Diagram

TERMINAL CONNECTIONS

Transparent Top View of Package

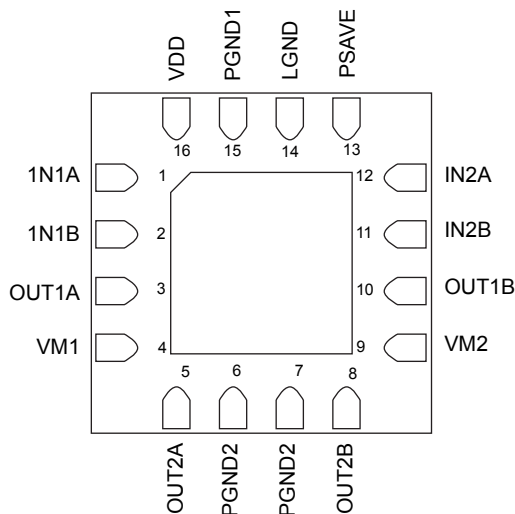


Figure 3. 17C724 Terminal Connections

Table 1. 17C724 Terminal Definitions

A functional description of each terminal can be found in the Functional Terminal Description section beginning on [page 8](#).

Terminal Number	Terminal Name	Terminal Function	Formal Name	Definition
1	IN1A	Logic	Logic Input Control 1A	Logic input control of OUT1A (refer to Table 5. Truth Table , page Z).
2	IN1B	Logic	Logic Input Control 1B	Logic input control of OUT1B (refer to Table 5. Truth Table , page Z).
3	OUT1A	Output	H-Bridge Output 1A	Output A of H-Bridge channel 1.
4	VM1	Power	Motor Driver Power Supply 1	Positive power source connection for H-Bridge 1 (Motor Driver Power Supply) ⁽¹⁾ .
5	OUT2A	Output	H-Bridge Output 2A	Output A of H-Bridge channel 2.
6, 7	PGND2	Ground	Power Ground 2	High-current power ground 2 ⁽²⁾ .
8	OUT2B	Output	H-Bridge Output 2B	Output B of H-Bridge channel 2.
9	VM2	Power	Motor Driver Power Supply 2	Positive power source connection for H-Bridge 2 (Motor Driver Power Supply) ⁽¹⁾ .
10	OUT1B	Output	H-Bridge Output 1B	Output B of H-Bridge channel 1.
11	IN2B	Input	Logic Input Control 2B	Logic input control of OUT2B (refer to Table 5. Truth Table , page Z).
12	IN2A	Input	Logic Input Control 2A	Logic input control of OUT2A (refer to Table 5. Truth Table , page Z).
13	PSAVE	Input	Input Enable Control	Logic input enable control of H-Bridges to save power.
14	LGND	Ground	Logic Ground	Low-current logic signal ground ⁽²⁾ .
15	PGND1	Ground	Power Ground 1	High-current power ground 1 ⁽²⁾ .
16	VDD	Logic	Logic Circuit Power Supply	Positive power source connection for logic circuit.

Notes

1. VM1 and VM2 are internally connected.
2. LGND, PGND1, and PGND2 are internally connected.

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Power Supply Voltage (Motor Driver) Normal Operation (Steady-State) Transient Conditions ⁽³⁾	$V_{M(SS)}$ $V_{M(PK)}$	-0.3 to 6.0 -0.3 to 6.5	V
Logic Supply Voltage	V_{DD}	6.0	V
Input Terminal Voltage	V_{IN}	-0.3 to $V_{DD} + 0.3$	V
Driver Output Current (Continuous) ⁽⁴⁾	I_O	400	mA
Driver Output Current (Peak) ⁽⁵⁾	I_{OPK}	800	mA
ESD Voltage ⁽⁶⁾ Human Body Model Machine Model	V_{ESD1} V_{ESD2}	± 2000 ± 200	V
TEMPERATURE RATINGS			
Storage Temperature	T_{STG}	-40 to 150	°C
Operating Temperature Ambient	T_A	-20 to 85	°C
Operating Junction Temperature	T_J	150 maximum	°C
Thermal Resistance (Junction-to-Ambient) Single-Layer PCB Mounting ⁽⁸⁾ Multi-Layer PCB (2S2P) Mounting ⁽⁹⁾	$R_{\theta JA}$ $R_{\theta JMA}$	169 47	°C/W
Terminal Soldering Temperature ⁽⁷⁾	T_{SOLDER}	260	°C

Notes

3. Transient condition within 500 ms.
4. Continuous output current must not be exceeded and at operating junction temperature below 150°C.
5. Peak time is for 10 ms pulse width at 200 ms intervals.
6. ESD testing is performed in accordance with the Human Body Model ($C_{ZAP}=100$ pF, $R_{ZAP}=1500$ Ω), **and** the Machine Model ($C_{ZAP}=200$ pF, $R_{ZAP}=0$ Ω).
7. Terminal soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
8. For cases using SEMI G38-87, JEDEC JESD51-2, JESD51-3, JESD51-5, single layer PCB mounting without thermal vias.
9. For cases using SEMI JEDEC JESD51-6, JESD51-5, JESD51-7, 2S2P PCB mounting with 4 thermal vias.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions $T_A = 25^\circ\text{C}$, $V_{DD} = V_M = 3.0\text{V}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^\circ\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT (VDD, PSAVE)					
Supply Voltage Range					V
Motor Driver Supply Voltage	V_M	2.7	3.0	5.5	
Logic Supply Voltage	V_{DD}	2.7	3.0	5.5	
Standby Power Supply Current ⁽¹⁰⁾					μA
$V_M = 3.0\text{V}$	$I_{V_{MSTBY}}$	–	–	1.0	
$V_{DD} = 3.0\text{V}$	$I_{V_{DDSTBY}}$	–	–	1.0	
Operating Power Supply Current ⁽¹¹⁾	I_C	–	40	100	μA
$V_{DD} = 3.0\text{V}$					
Logic Input Function					
High-Level Input Voltage	V_{IH}	$V_{DD} 0.7$	–	–	V
Low-Level Input Voltage	V_{IL}	–	–	$V_{DD} 0.3$	V
High-Level Input Current	I_{IH}	–	–	1.0	μA
Low-Level Input Current	I_{IL}	-1.0	–	–	μA
PSAVE Terminal Low Level Input Current ⁽¹²⁾	I_{IL}	–	-30	-60	μA
Driver Output ON Resistance ⁽¹³⁾	$R_{DS(ON)}$	–	1.0	1.5	Ω
Low-Voltage Shutdown Detection Voltage ⁽¹⁴⁾	V_{DDDET}	1.5	2.0	2.5	V

Notes

10. Power SAVE mode.
11. I_C is the sum of the current of V_{DD} monitor block “Low Voltage Detection Module” and the PSAVE pull-up resistor at $f_{IN} = 200\text{ kHz}$.
12. $V_{DD} = 3.0\text{ V}$.
13. $I_O = 375\text{ mA}$. $R_{DS(ON)} = R_{SOURCE} + R_{SINK}$. $R_L = 6.8\ \Omega$.
14. Detection voltage is defined as when the output becomes high impedance after V_{DD} voltage falls and when $V_M = 5.5\text{ V}$.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions $T_A = 25^\circ\text{C}$, $V_{DD} = V_M = 3.0\text{V}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^\circ\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT					
Pulse Input Frequency	f_{IN}	–	–	200	kHz
Input Pulse Rise Time ⁽¹⁵⁾	t_R	–	–	1.0 (16)	μs
Input Pulse Fall Time ⁽¹⁷⁾	t_F	–	–	1.0 (16)	μs
OUTPUT					
Output Propagation Delay Time ⁽¹⁸⁾					μs
Turn-ON Time	t_{PLH}	–	0.2	0.5	
Turn-OFF Time	t_{PHL}	–	0.1	0.5	
Low-Voltage Detection Time	$t_{V_{DD}DET}$	–	0.02	1.0	ms

Notes

15. Time is defined between 10% and 90%.
16. That is, the input waveform slope must be steeper than this.
17. Time is defined between 90% and 10%.
18. $R_L = 6.8 \Omega$. Slew time, rise time, and fall times are between 10% and 90% of output low and high levels with respect to the 50% level of the input.

TIMING DIAGRAMS

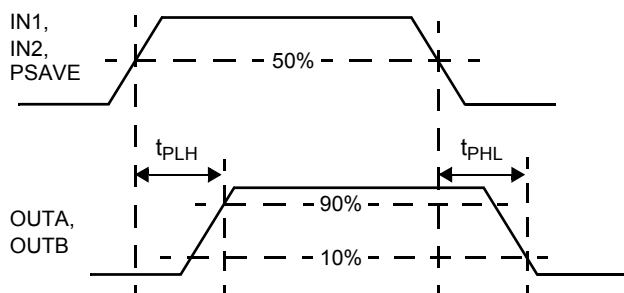
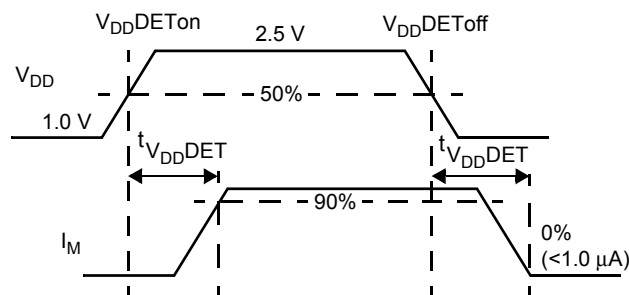
Figure 4. t_{PLH} and t_{PHL} Timing

Figure 5. Low-Voltage Detection Timing

Table 5. Truth Table

INPUT			OUTPUT		$V_{DDDET}^{(20)}$
PSAVE ⁽¹⁹⁾	IN1A IN2A	IN1B IN2B	OUT1A OUT2A	OUT1B OUT2B	
L	L	L	L	L	Enabled
L	H	L	H	L	Enabled
L	L	H	L	H	Enabled
L	H	H	Z	Z	Enabled
H	X	X	Z	Z	Disabled

H : High
 L : Low
 Z : High impedance
 X : Don't care

Notes

- Terminal 13 (PSAVE) is pulled up by an internal resistor.
- When V_{DD} is lower than V_{DDDET} while V_M is applied, output becomes "Z" (high impedance); however, when PSAVE = "H", the low-voltage shutdown detection circuit is disabled.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 17C724 is a monolithic dual H-Bridge that is ideal in portable electronic applications to control bipolar step motors and brush DC motors such as those used in camera lens and shutters. The 17C724 can operate efficiently with supply voltages as low as 2.7 V to as high as 5.5 V, and provide continuous motor drive currents of 0.4 A while handling peak currents up to 0.8 A. It is easily interfaced to low-cost MCUs via parallel 3.0 V- or 5.0 V-compatible logic. The device can be pulse width modulated (PWM'ed) at up to 200 kHz.

The 17C724 can drive two motors simultaneously (see [Figure 6](#)), or it can drive one bipolar step motor as shown in the simplified application diagram on [page 1](#). Dual channel

parallel drive is also possible if higher current drive is desired (0.8 A). Two-motor operation is accomplished by hooking one motor between OUT1A and OUT1B, and the other motor between OUT2A and OUT2B.

This IC has a built-in shoot-through current protection circuit and undervoltage detector to avoid malfunction. It also allows for power-conserving Sleep mode by the setting of the PSAVE terminal (refer to [Table 5, Truth Table](#), page 7).

The device features four operating modes: Forward, Reverse, Brake, and Tri-States (High Impedance).

FUNCTIONAL TERMINAL DESCRIPTION

LOGIC CIRCUIT POWER SUPPLY (VDD)

The VDD terminal carries the power source connection to the control (logic) circuit, and its input range is between 2.7 V to 5.5 V (3.0 V and 5.0 V compatible). V_{DD} has an undervoltage threshold. If the supply voltage to V_{DD} drops below 2.0 V (typical), then all the output of H-Bridges (OUT1A, OUT1B, OUT2A, OUT2B) will become open (high impedance = Z). When the supply voltage returns to a level that is above the threshold voltage the H-Bridge outputs automatically resume normal operation according to the established condition of the input terminals.

LOGIC INPUT CONTROL (IN1A, IN1B, IN2A, AND IN2B)

These logic input terminals control each H-Bridge output. For example, IN1A logic HIGH = OUT1A HIGH; likewise, IN1B logic HIGH = OUT1B HIGH. If both A and B inputs are HIGH, then both A and B outputs are Z (refer to [Table 5, Truth Table](#), page 7).

INPUT ENABLE CONTROL (PSAVE)

The PSAVE input controls the functioning of the power output stages (the H-Bridges). When it is set logic LOW, the output stages are enabled and the H-Bridges function normally. When it is set logic HIGH, the output stages are disabled and all the outputs are opened (high impedance). In

this mode, the built-in low-voltage detection circuit is disabled.

H-BRIDGE OUTPUT (OUT1A, OUT1B, OUT2A, AND OUT2B)

These terminals are the outputs of the power MOSFET H-Bridges. OUT1 is from H-Bridge Channel 1, and OUT2 from H-Bridge Channel 2. These terminals will typically connect to an external load (step motor or brush DC motors).

MOTOR DRIVER POWER SUPPLY (VM1 AND VM2)

VM1 and VM2 carries the main supply voltage and current into the power sections (the H-Bridges) of the IC. Both of these terminals are connected internally but they must be connected together on the printed circuit board with as short as possible traces. The input range is 2.7 V to 5.5 V.

POWER GROUND (PGND1 AND PGND2)

These two are the power ground terminals that connect to the power ground of the H-Bridges. The power grounds are for higher current handling capability from loads and they must be connected together on the PCB.

LOGIC GROUND (LGND)

LGND is the logic ground terminal and its current handling level is lower than the PGND.

TYPICAL APPLICATIONS

Figure 6 shows a typical application for the 17C724.

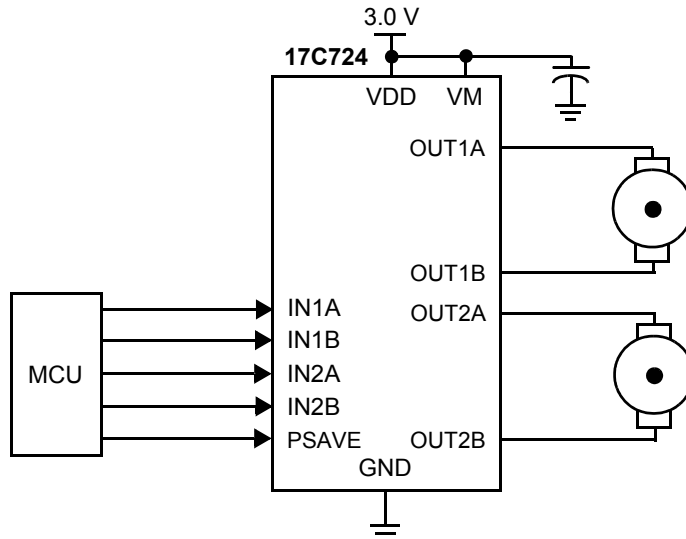


Figure 6. 17C724 Typical Application Diagram

CEMF SNUBBING TECHNIQUES

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commutating currents in inductive loads. Typical practice is to provide snubbing of voltage transients by placing a zener or capacitor at the supply terminal (VM) (see Figure 7).

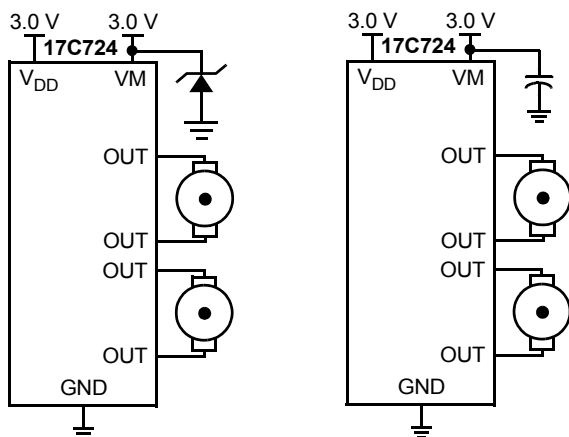


Figure 7. CEMF Snubbing Techniques

PCB LAYOUT

When designing the printed circuit board (PCB), connect sufficient capacitance between power supply and ground terminals to ensure proper filtering from transients. For all high-current paths, use wide copper traces and shortest possible distance.

APPLICATION NOTES

Although VM1 and VM2 are connected internally, they must be connected externally to attain sufficient power distribution.

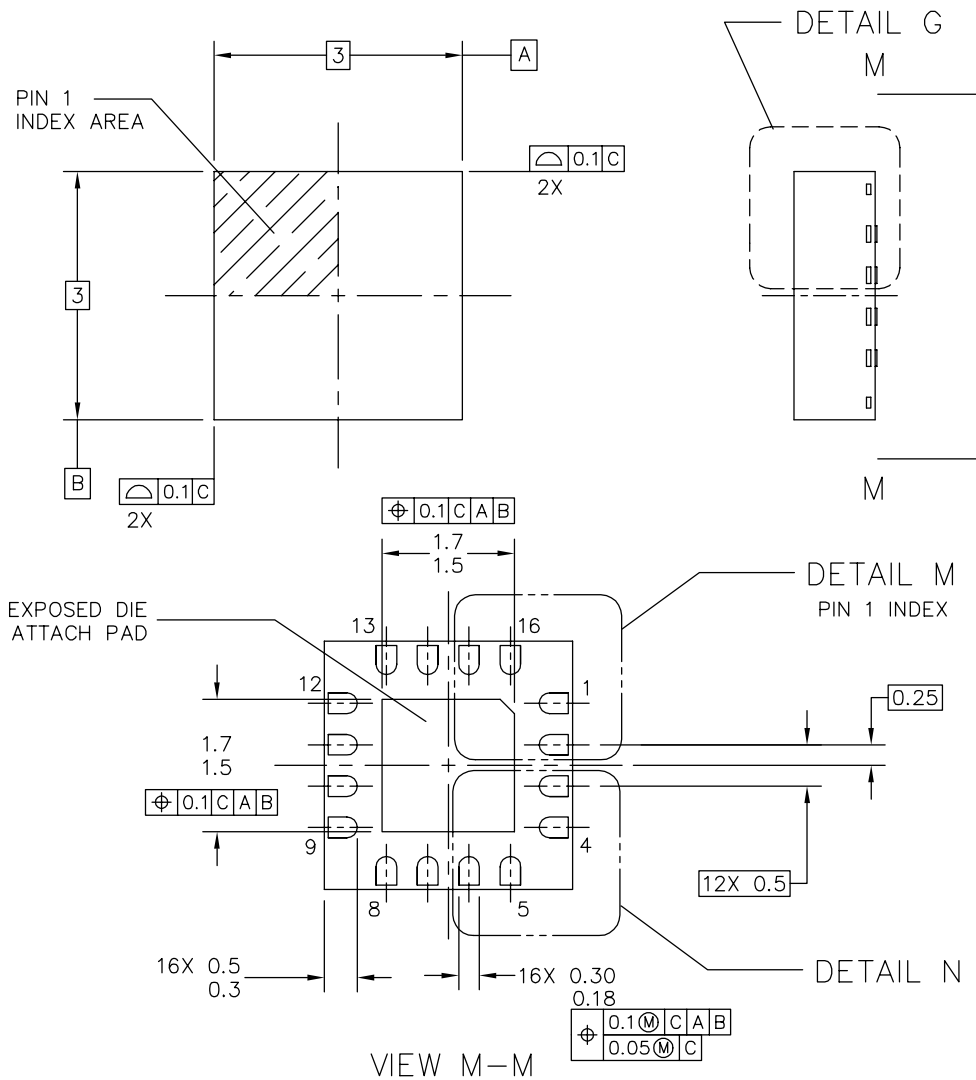
Take precautions to guard against electrostatic discharge when handling the device, especially when mounting and demounting the device to a PCB.

PACKAGING

PACKAGE DIMENSIONS

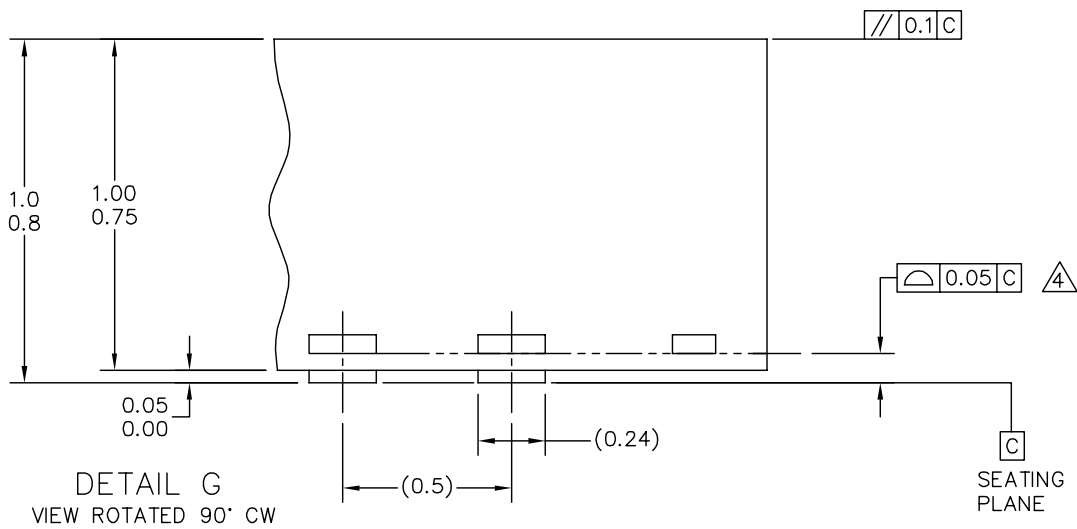
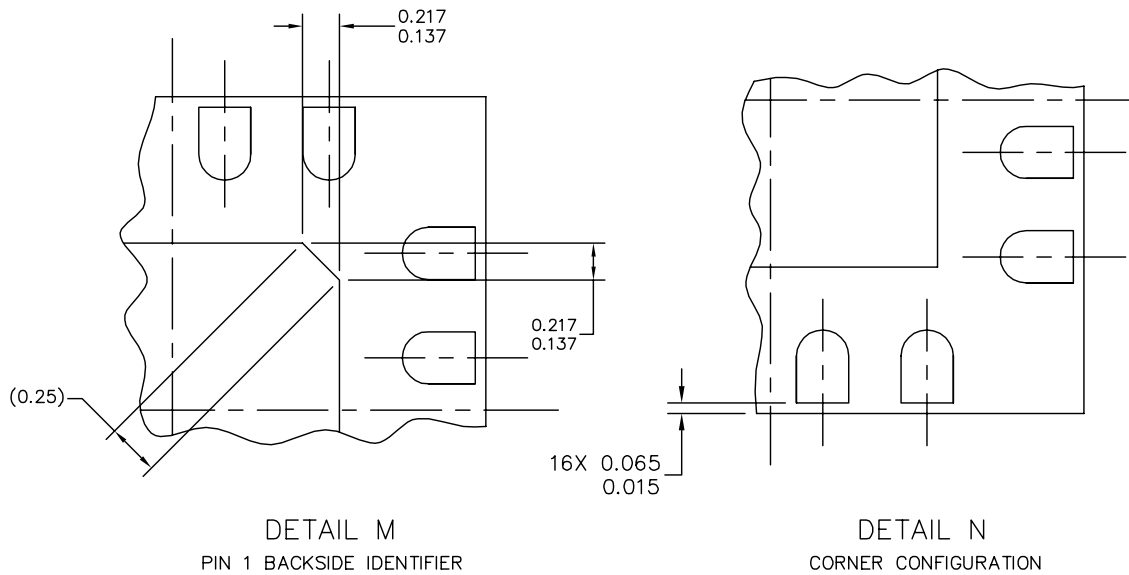
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16-TERMINAL QFN
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REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
2.0	2005	<ul style="list-style-type: none">Initial Release

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